Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines

Susann Rothe
susann.rothe@mailbox.tu-dresden.de
Dresden University of Technology, Institute of Electromechanical and Electronic Design (IFTE)
Dresden, Germany

Jens Lienig
jens@ieee.org
Dresden University of Technology, Institute of Electromechanical and Electronic Design (IFTE)
Dresden, Germany

ABSTRACT

The migration of atoms in metal interconnects in integrated circuits (ICs) increasingly endangers chip reliability. The susceptibility of DC interconnects to electromigration has been extensively studied. A few works on thermal migration and AC electromigration are also available. Yet, the combined effect of both on chip reliability has been neglected thus far. This paper provides both FEM and analytical models for atomic migration and steady-state stress profiles in AC interconnects considering electromigration, thermal and stress migration combined. For this we expand existing models by the impact of self-healing, temperature-dependent resistivity, and short wire length. We conclude by analyzing the impact of thermal migration on interconnect robustness and show that it cannot be neglected any longer in migration robustness verification.

CCS CONCEPTS

• **Hardware → Aging of circuits and systems**; *Metallic interconnect*; Wire routing.

KEYWORDS

Electromigration, Thermal Migration, Physical Design, Reliability, AC Interconnects

ACM Reference Format:
Susann Rothe and Jens Lienig. 2023. Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines. In *Proceedings of the 2023 International Symposium on Physical Design (ISPD '23), March 26–29, 2023, Virtual Event, USA.* ACM, New York, NY, USA, 8 pages. https://doi.org/10.1145/3569052.3571880

1 INTRODUCTION

The miniaturization of integrated circuit (IC) structure sizes exacerbates the challenges of designing reliable chips [13]. One of the constraints on IC lifetimes are metal interconnects that are degraded by atomic migration.

There are three major migration mechanisms (also shown in Fig. 1): The best known mechanism is *electromigration* (EM) which is driven by an electric current. Temperature gradients within a wire cause *thermal migration* (TM). Both EM and TM are increasing in severity as current densities rise in advanced semiconductor technologies accompanied by a tightening of migration robustness constraints (Fig. 2) [2, 13, 21]. The third mechanism is *stress migration* (SM), which arises from hydrostatic stress gradients and can thus partly reverse the atom dislocation caused by EM and TM.

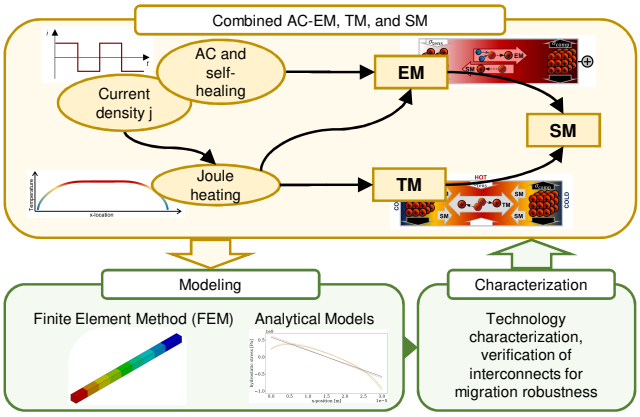

Figure 1: Illustration of the interactions of EM, TM, and SM (top) and the contribution of this paper (bottom). As shown on the lower left, we provide both FEM and analytical models in order (1) to identify core parameters and (2) to show the need to consider Joule heating and TM in migration robustness verification. Our models can be the basis for experimental technology characterization, migration robustness verification, and novel design strategies to mitigate migration-induced failures (lower right).

Atom dislocation within an interconnect can cause (1) voids (which lead to opens) as a consequence of tensile stress and (2) hillocks (which can form shorts to other nets) resulting from compressive stress. Both cases are critical in terms of reliability [20].

Technological modifications, introduced in the metal stack, are increasingly used to counter these migration issues in leading-edge technologies. For example, the scaling of conventional copper lines is more and more constrained by rising resistivity and EM risk. Thus, novel materials (e. g., cobalt liners [28]) are applied in the lower metal layers which are most susceptible to EM.

In addition to technological changes, migration has been also addressed within the design flow. Here, EM verification has been focused mostly on DC nets (e. g., power delivery networks, PDNs), thereby relying on boundaries for current density [5, 6, 27]. Yet, recent studies show that also AC lines, like signal and clock nets, suffer from migration-induced failure [4, 11]. (AC lines have been

ISPD '23, March 26–29, 2023, Virtual Event, USA

ACM ISBN 978-1-4503-9978-4/23/03.
https://doi.org/10.1145/3569052.3571880

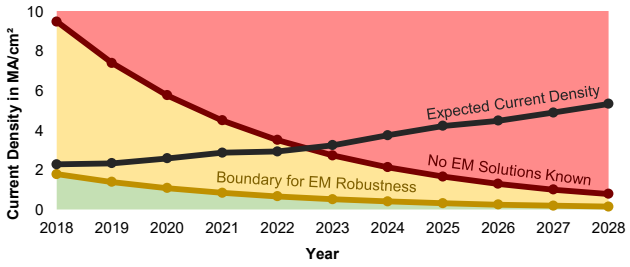

Figure 2: Prognosis for current densities and EM boundary values in [14]. There is no risk of EM-induced failures in the green area, while in the yellow area, EM degradation occurs but can be handled by design and verification measures. There are no known solutions for EM-robust layout design in the red area [13, 20, 27] which motivates the presented work in this paper.

widely considered as EM robust up to now because of their inherent self-healing effects.) In addition, the EM robustness of both DC and AC lines is highly dependent on their topology (e. g., length) [18]. Hence, it is getting more and more obvious that current density boundaries alone are not sufficient to capture EM robustness. Moreover, TM is gaining in significance and cannot be neglected anymore [2].

As a consequence of these developments, novel design and verification methodologies that combine (better) EM and TM modeling are required to maintain migration robustness in IC design [27]. This task is challenging as EM, TM, and SM are closely coupled. Hence, combined models to capture the total atomic flux and stress evolution are urgently needed.

In order to achieve this, we propose both FEM and analytical models in this paper that allow us to calculate the steady-state stress distribution in AC interconnect lines. We derive the exact equation to calculate the location and value of the stress maximum to estimate the risk of voiding. Moreover, we investigate the effect of short wire length and temperature-dependent resistivity on the stress distribution.

Thus, the contribution of this paper (also illustrated in Fig. 1) are novel models that enable a thorough analysis of the parameters impacting the migration robustness of signal lines. These models can then be used for experimental technology characterization and migration robustness verification in state-of-the-art design flows where conventional EM verification (see above) increasingly fails.

We aim to establish a basis for future work on migration assessment in clock and signal nets by thoroughly investigating migration mechanisms and key parameters in AC interconnects. To support this goal, our FEM models are available online [26].

The remainder of this paper is organized as follows: Section 2 introduces the basics of today's methodologies in migration modeling. In Section 3, we present our novel FEM and analytical models for combined EM, TM, and SM simulation. Section 4 shows results w.r.t. the main material parameters and the significance of TM. We conclude our paper in Section 5 with a summary and outlook.

2 FUNDAMENTALS AND RELATED WORK

2.1 Migration Mechanisms

EM (Fig. 3) is driven by an electric current. The momentum transfer from the conduction electrons to the metal atoms causes the atoms to move from the cathode to the anode. TM (Fig. 4) arises from temperature gradients in interconnects. Reasons for temperature gradients are (1) Joule heating and (2) external heat sources (e. g., transistors with high power dissipation). Atoms move from hot to cold regions of a wire. SM is caused by stress gradients that can have their origins in the fabrication process and thermal expansion. Both effects are significant and can be considered as initial stress conditions. However, their investigation is beyond the scope of this paper as they are caused by external conditions and not by processes within the wire. In this work, we limit our consideration to wire-internal SM, which is caused by the other migration mechanisms (EM, TM). Here, SM is a counteracting force to the atomic motion induced by EM and TM [20].

The atomic fluxes driven by SM, EM, and TM add up to a total atomic flux causing stress to build up in the interconnect. This process is called *stress evolution*. For a straight interconnect line stress evolution can be expressed by

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB\Omega}{k_\mathrm{B}T}\left(\frac{\partial \sigma}{\partial x} - \frac{e\rho Z j}{\Omega} - \frac{Q}{\Omega T}\frac{\partial T}{\partial x}\right)\right] \tag{1}$$

which is based on Korhonen's equation for EM and SM [18] and was expanded by the impact of TM in [7]. The term σ is the hydrostatic stress, t the time, x the location on the wire, D the diffusion coefficient with $D = D_0 \cdot \exp\left(-E_\mathrm{a}/(k_\mathrm{B}T)\right)$ (where D_0 is the diffusion constant), B the Bulk's modulus, Ω the atom volume, k_B Boltzmann's constant, T the temperature, e the elementary charge, ρ the specific resistivity, Z the effective charge number, j the current density, and Q the specific heat of transport.

Stress evolution is always calculated for wire segments that are bordered by diffusion barriers. In modern dual-damascene technologies, these barriers are located below the vias (i. e., on top of the metal layers). If both current and temperature profile remain constant over time, the stress distribution will eventually reach a steady state where the total atomic flux is zero.

Positive (tensile) stress is a sign for material depletion. If the stress is too high, a void can nucleate and grow. Negative (compressive) stress occurs when material accumulates. In rare cases, this can lead to the formation of hillocks. The stress maximum within an interconnect usually occurs near its cathode. The stress minimum is located at the anode. [20]

2.2 Thermal Characterization of Interconnects

To calculate TM-induced stress it is crucial to know the exact temperature profile along the wire. This is a challenging task as the temperature in an interconnect depends on numerous factors such as current load, interconnect geometry, surrounding material and external heat sources. In this paper, we apply the model presented in [8] which is commonly used for TM simulation. It captures the most important effects (ambient temperature of the wire, Joule heating, heat conduction along the wire, and heat dissipation toward the surroundings) but neglects other factors such as chip surroundings, temperature-dependent resistivity, and external heat sources

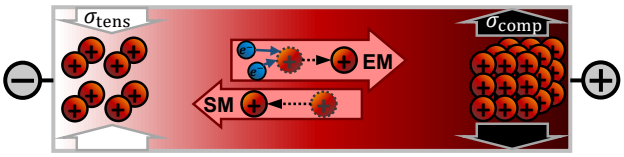

Figure 3: Electromigration is driven by an electric field. Atoms move from the cathode toward the anode. This creates a stress gradient which leads to stress migration partly reversing the effect of EM [27].

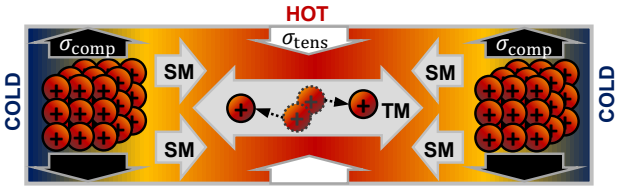

Figure 4: Thermal migration arises from temperature gradients. Atoms move from hot toward cold locations in a wire. Also in this case, the effect of TM is partly reversed by stress migration [27].

that locally impact the wire temperature. This model describes the temperature T along a straight wire with the length L and $T_i = T_j$ as the temperatures at the wire's ends as

$$T(x) = \left[\overline{T} - (T_0 + T_m)\right]\left[\cosh\left(\frac{x}{\Gamma}\right)\operatorname{sech}\left(\frac{L}{2\Gamma}\right)\right] + (T_0 + T_m) \quad (2)$$

with $\overline{T} = (T_i + T_j)/2$, the temperature of the surroundings T_0, the maximum temperature rise $T_m = \rho j^2 \Gamma^2 / k_{Cu}$, and the thermal length $\Gamma \approx \sqrt{t_{Cu} t_{ILD} k_{Cu}/k_{ILD}}$. Terms t_{Cu} and t_{ILD} stand for the thickness and k_{Cu} and k_{ILD} for the thermal conductivity of the metal layer and the interlayer dielectric, respectively. The model is based on the equation for Joule heating in metal interconnects that describes the heat produced by a current flow:

$$\phi_{th} = j^2 \rho \quad (3)$$

where ϕ_{th} is the thermal power density.

2.3 Migration Robustness Assessment of DC Networks

The focus of migration robustness verification is on EM in DC networks (mainly PDNs) that carry high currents and do not benefit from changing current direction (cf. Sec. 2.4). PDNs usually consist of large interconnect trees that are composed of a high number of branches. This makes accurate and time-efficient stress calculation difficult. Approaches to solve this issue are, for example, the use of equivalent RC-networks [24], voltage-based EM assessment (VBEM method) [29, 30] and machine-learning-based methods [15, 16].

There are also a few works investigating the influence of time-varying current density and self-healing in DC networks [12, 30].

Recent studies [2, 7, 17] have already proposed combined EM and TM assessment of DC networks. They observed that the impact of TM cannot be neglected any longer as it can be in the same order of magnitude like EM.

2.4 Migration Susceptibility of AC Lines

AC lines (such as signal and clock nets) are stressed with changing current directions as the parasitic capacitances of the transistors and interconnects have to be charged and discharged when switching the state of the gate (Fig. 5) [3]. Due to the changing current direction, the EM-induced atom dislocation is partly reversed. Hence, EM in AC lines is characterized by the so-called *effect of self-healing*.

For perfectly symmetric switching profiles one would expect complete self-healing. However, self-healing is imperfect due to multiple factors such as leakage currents, dissimilar capacitances of PMOS and NMOS transistors and grain boundary effects. This imperfection is captured by the self-healing factor r [31] which is a widely recognized simplification to model the complex mechanisms of self-healing (that are only partly understood to this day) [19, 31]. The self-healing factor r usually ranges from 0.7 to 0.9 [19, 31].

Migration-induced AC interconnect failures could be prevented by self-healing in the past. Yet, this is not true anymore [9–11, 25] because migration robustness constraints are tightening due to miniaturization. Nevertheless, as migration robustness verification for AC lines has been widely neglected, models to simulate migration processes in these nets have remained rudimentary.

There are only a few experimental studies on EM in AC lines, such as [22, 23, 32, 33], that have attempted to quantify the effect of self-healing. However, to our best knowledge, there are no published results on AC migration in leading-edge technology nodes which are characterized by both high current densities and low migration robustness boundaries.

It should also be noted that self-healing does not apply to TM-induced atom dislocation. Joule heating and temperature gradients are independent of the current direction. Hence, the growing significance of TM not only affects DC lines but also (and even worse) AC interconnects.

3 NOVEL MIGRATION MODELING IN AC LINES

3.1 FEM Models for Combined EM, TM, and SM Analysis of AC Lines

We have developed new FEM models (available at [26]) that can be applied to simulate EM, TM, and SM in AC interconnect lines. They are based on the models described in [2, 4, 7], using the Ansys® Parametric Design Language (APDL). While we will subsequently focus on the simple case of straight interconnect lines, note that our models can also be applied to more complex interconnect trees, as shown in Fig. 6[1].

Self-healing should be considered for EM in AC lines, as described in Sec. 2.4. In FEM simulations, it can be modeled by reducing the current density j by the factor $(1 - r)$. However, for TM simulation, Joule heating which is also dependent of j has to be

[1]To be more specific, wire geometry, boundary conditions, loads and material parameters can easily be edited in the APDL scripts publicly provided in [26] which then allows to simulate any interconnect structure.

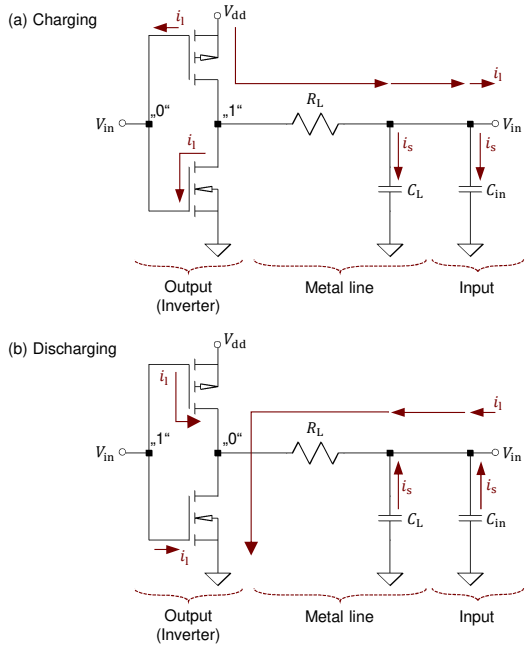

Figure 5: Illustration of the changing current direction in AC lines. A metal line connecting an inverter output to another gate (capacitance C_{in}) can be modeled as a first-order low pass (R_L, C_L). The schematics (a) and (b) show the direction of the leakage currents i_l and the switching currents i_s for the two inverter states. The self-healing effect observed in AC nets can be attributed to these alternating currents. [3]

.

modeled as well. Consequently, the self-healing effect needs to be considered differently.

In our model, we resolve this issue by including the self-healing factor r in the effective charge number Z. This material parameter only appears in the EM diffusion equation and does not affect TM or SM. Thus, Z_{AC} can be calculated as $Z_{AC} = (1 - r) \cdot Z$.

To model TM, knowing the temperature profile along the wire is crucial. Thermal modeling is challenging for single interconnect trees because of the (unknown) impact of the surroundings. However, we can assume that high temperature gradients within an interconnect are mainly caused by Joule heating and that the temperature of the interconnect's surroundings is fairly constant (compared to the temperature differences due to Joule heating) [8]. For heat dissipation, we chose a simplistic approach to model heat flux along the wire and toward the surrounding dielectric by applying a constant temperature to the wire ends and the surroundings (Fig. 7, top). Heat dissipation from the wire to the dielectric is modeled by convection [7] with:

$$q_{ILD} = \frac{k_{ILD}}{t_{ILD}} (T(x) - T_0). \tag{4}$$

Consequently, our results show a symmetric temperature profile along the wire and correspond to the temperature model described in Sec. 2.2. If the wire is long, the temperature will remain relatively

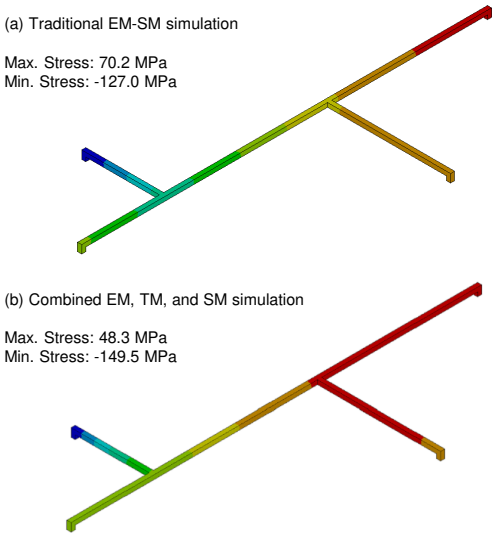

Figure 6: FEM results for (a) traditional EM and SM simulation and (b) combined EM, TM, and SM simulation for a more complex interconnect geometry, publicly available in [26]. Setting Z=5 and Q=0.5 eV, the stress maximum is located at the cathode both for EM-SM and combined EM, TM, and SM consideration. When Q is increased (or Z decreased), the location of the stress maximum shifts toward the middle of the interconnect due to stronger TM effect.

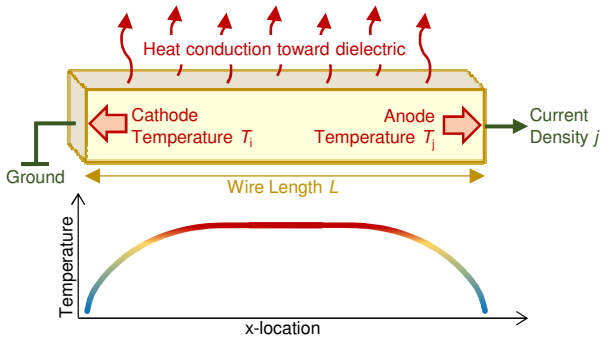

Figure 7: FEM loads and constraints for combined EM, TM, and SM simulation in a straight interconnect line and the typical temperature profile caused by Joule heating.

constant in the middle of the wire while dropping off at the wire ends (Fig. 7, bottom).

Joule heating, and thus the resulting TM, can be disabled in the FEM models. Hence, they can be used to compare the standard EM and SM simulation at a constant temperature with the combined EM, TM and SM consideration presented in this paper. Moreover, they include the option to incorporate the temperature dependency of the specific resistivity into the calculation (cf. Sec. 3.3). Both options are given as examples in [26].

3.2 Analytical Description of Migration-Induced Stress in AC Lines

The steady-state stress distribution caused by EM, TM, and SM in AC lines can be calculated with our novel analytical models.

We assume the simple case from Fig. 7. That is, a straight wire from $x_i = -L/2$ to $x_j = +L/2$: with width w equal to height h; a constant current density j; and with the wire ends and surroundings at the same temperature $T_\mathrm{i} = T_\mathrm{j} = T_0$. The temperature along this wire can be calculated using (2).

The stress distribution along a wire [7] is described by

$$\sigma(x) = \frac{eZ_\mathrm{AC}\rho}{\Omega} jx + \frac{Q}{\Omega}\ln(T(x)) + \sigma_0 \tag{5}$$

and the stress difference between two points on the wire is represented by

$$\sigma(x_1) - \sigma(x_2) = \frac{eZ_\mathrm{AC}\rho j}{\Omega} L_{12} + \frac{Q}{\Omega}\Big[\ln(T(x_1)) - \ln(T(x_2))\Big]. \tag{6}$$

We have already included self-healing here. The sum of two stress values was derived in [7] and can be obtained by

$$\sigma(x_1) + \sigma(x_2) = -\frac{2}{L_{12}}\frac{Q}{\Omega}\left[\ln\left(\frac{T_0 + T_\mathrm{m}}{\sqrt{T_1 T_2}}\right) L_{12} + \frac{T_1 + T_2 - 2(T_0 + T_\mathrm{m})\Gamma}{(T_0 + T_\mathrm{m})}\tanh\left(\frac{L_{12}}{2\Gamma}\right)\right]. \tag{7}$$

The derivation of (7) includes the integral over (2) given in [1] which was only solved for the special case of $T_0 >> T_\mathrm{m}$ and $L >> \Gamma$. Thus, our analytical solution for the calculation of stress values is limited to this assumption.

In contrast to EM, for TM consideration it is not sufficient to know the stress at the wire terminals and junctions for migration-robustness assessment. This is because the maximum stress can be located elsewhere in the wire rather than at the cathode. Consequently, we need to calculate its location x_s and stress value $\sigma(x_\mathrm{s})$.

The formula for x_s given in [1] relies on the same assumptions as the temperature integral mentioned above and, thus, lacks precision. Neither does it provide valid solutions in some cases due to the self-healing effect in AC lines and, thus, a stronger TM effect.

We found the exact equation for the location of the stress maximum (which can be solved also for all cases, including those with high TM impact) by setting the derivation of the steady-state stress profile (5) along a wire to zero (8) and solving for x_s:

$$\sigma'(x_\mathrm{s}) = \frac{eZ_\mathrm{AC}\rho}{\Omega} j + \frac{Q}{\Omega T(x_\mathrm{s})} T'(x_\mathrm{s}) \stackrel{!}{=} 0 \tag{8}$$

$$x_\mathrm{s} = \Gamma \cdot \ln\left[\frac{A\Gamma\left(\frac{T_0}{T_\mathrm{m}} + 1\right)}{\Gamma - C} + \sqrt{\left(\frac{A\Gamma\left(\frac{T_0}{T_\mathrm{m}} + 1\right)}{\Gamma - C}\right)^2 - \frac{\Gamma + C}{\Gamma - C}}\right] \tag{9}$$

where $A = \cosh\left(\frac{L}{2\Gamma}\right)$ and $C = -\frac{Q}{eZ_\mathrm{AC}\rho j}$.

To calculate the stress $\sigma(x_\mathrm{s})$ we adapt the voltage-based stress analysis proposed in [2] by considering self-healing on the one hand, and introducing a new point for the calculation at x_s on the other. The fundamental equation for the voltage-based approach is derived from (6) by replacing $\rho j L_{12}$ with ΔV:

$$\sigma(x_2) - \sigma(x_1) = \frac{Z_\mathrm{AC} e}{\Omega}(V(x_1) - V(x_2)) + \frac{Q}{\Omega}\left[\ln(T(x_2)) - \ln(T(x_1))\right]. \tag{10}$$

Consequently, we can calculate $\sigma(x_\mathrm{s})$ as

$$\sigma(x_\mathrm{s}) = \frac{Z_\mathrm{AC} e}{\Omega}(V(x_1) - V(x_\mathrm{s})) + \frac{Q}{\Omega}\left[\ln(T(x_\mathrm{s})) - \ln(T(x_1))\right] + \sigma(x_1) \tag{11}$$

where $\sigma(x_1)$ can be determined using (6) and (7).

Our FEM models agree with the analytical solution given in this section under the conditions stated above: $T_0 >> T_\mathrm{m}$ and $L >> \Gamma$. Our calculation of x_s corresponds with the FEM results also for shorter wires and high T_m (cf. Sec. 4).

3.3 Considering Temperature-Dependent Resistivity and Short Wires

As already mentioned in Sec. 3.2, analytical solutions are only known for simplistic cases and under certain conditions. We can capture more realistic migration profiles in FEM models, however. Specifically, we improved our models by considering temperature-dependent resistivity ρ. Moreover, our FEM models do not rely on approximations that are only valid for long wires with a small temperature rise. We can also model cases for which the assumptions made in Sec. 3.2 are not valid.

The temperature dependency of ρ is usually approximated by

$$\rho(T_0 + \Delta T) = \rho_0(1 + \alpha\Delta T) \tag{12}$$

where α is the linear temperature coefficient and ρ_0 is the specific resistivity at $T = T_0$. Consequently, the specific resistivity along a wire varies with temperature and is a function of x. This also impacts the temperature along the wire itself as Joule heating depends on ρ. As a result, our FEM simulations show higher temperature differences along the wire and, thus, enhanced EM and TM which leads to more severe stress differences.

We also expand the equation for the temperature profile along the wire (2) by considering $\rho(T, x)$ in order to verify our FEM results. The equation for the temperature profile can be written as

$$T(x) = T_0 + \Delta T(x) \tag{13}$$

where

$$\Delta T(x) = T_\mathrm{m}\left[1 - \cosh\left(\frac{x}{\Gamma}\right)\mathrm{sech}\left(\frac{L}{2\Gamma}\right)\right]. \tag{14}$$

We expand the expression for temperature T_m, which is a function of ρ, to consider the location along the wire:

$$T_\mathrm{m} = \frac{\rho(x) j^2 \Gamma^2}{k_\mathrm{Cu}} = \frac{\rho_0(1 + \alpha\Delta T(x)) j^2 \Gamma^2}{k_\mathrm{Cu}} = T_\mathrm{m0}(1 + \alpha\Delta T(x)). \tag{15}$$

We then get

$$\Delta T(x) = T_\mathrm{m0}(1 + \alpha\Delta T(x))\left[1 - \cosh\left(\frac{x}{\Gamma}\right)\mathrm{sech}\left(\frac{L}{2\Gamma}\right)\right]. \tag{16}$$

Solving for $\Delta T(x)$ yields the final solution for the temperature profile:

$$T(x) = T_0 + \frac{T_\mathrm{m0}\left[1 - \cosh\left(\frac{x}{\Gamma}\right)\mathrm{sech}\left(\frac{L}{2\Gamma}\right)\right]}{1 - \alpha T_\mathrm{m0}\left[1 - \cosh\left(\frac{x}{\Gamma}\right)\mathrm{sech}\left(\frac{L}{2\Gamma}\right)\right]}. \tag{17}$$

This temperature profile is in excellent agreement with our FEM models that consider temperature-dependent ρ.

4 SIMULATION RESULTS

4.1 Growing Impact of TM and Temperature-Dependent Resistivity

Recent studies [2, 7] have indicated that TM significantly impacts migration robustness. Investigating this further, we have so far shown that the migration-robustness assessment of AC interconnects is even more affected by TM consideration as EM is reduced by self-healing. Figure 8 depicts the simulation results for a single 30 µm line – indicating clearly the differences between the EM-induced stress profile and the combined EM and TM simulation. It becomes obvious that TM can mitigate the danger of migration-induced wire degradation by decreasing the maximum occurring tensile stress. Thereby, the risk of voiding is reduced. Hence, EM verification without considering TM can be pessimistic and may result in overdesign. On the other hand, the compressive stress is increased and should be considered. However, it is not as critical as tensile stress because voiding is the most common EM failure mechanism.

In Fig. 8 we also see that the location of the stress maximum is shifted toward the middle of the wire. Consequently, migration verification cannot just be based on the stress occurring at the wire's ends as the risk of voiding could be underestimated based on the stress at the cathode. Hence, we need methods to calculate the stress profile along the wire or to directly derive the location of the stress maximum, as described in Sec. 3.2.

The influence of TM is especially significant for AC lines as in these nets EM is reduced by self-healing. Consequently, the shifted stress maximum is likely to be observed in AC lines, not DC nets. Therefore, more precise stress modeling is required for AC lines, while monitoring the tensile stress at the cathode is often all that is required for DC lines.

Furthermore, the dotted lines in Fig. 8 represent the stress profiles obtained by FEM simulation when temperature-dependent resistivity is considered. The relative error caused by ignoring $\rho(T)$ depends on the material parameters, wire geometry and current load. However, we have found that if $\rho(T)$ is not considered the hydrostatic stress is always underestimated and there is a need for safety margins in the design flow.

4.2 Impact of Material Properties on EM and TM

The quantitative effect of TM on overall migration robustness depends to a large extent on the material parameters (such as specific resistivity ρ, heat of transport Q, effective charge number Z, and thermal conductivity k), wire geometry and current load. Especially the material parameters are hard to measure and differ in every technology. Consequently, a wide range of values can be found in literature. This is particularly true for the effective charge number Z and the heat of transport Q in the calculations for the steady-state stress profile (5). Hence, we conducted FEM simulations on the 30 µm line cited earlier and varied these two parameters across their respective permissible ranges. We considered both EM and TM in the first run and neglected TM in the second run by applying a constant temperature to the entire wire.

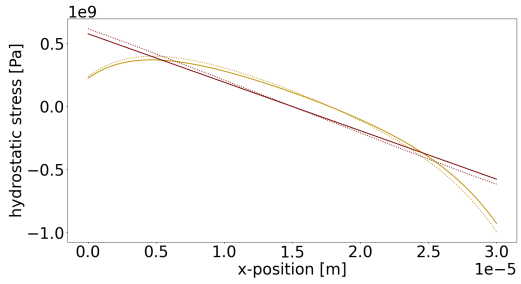

Figure 8: Comparison of the stress profile for EM (red lines) and combined EM-TM simulation (yellow lines) in a straight interconnect line with L=30 µm, w=h=0.1 µm, j=10 MA/cm^2, Z=5, r=0.9 and Q=0.5 eV. The dotted lines show the impact of temperature-dependent resistivity.

The results are shown in Fig. 9. First, we compared the maximum occurring stress in both cases. We can conclude that the relative stress reduction caused by TM grows as Q increases (i. e., stronger TM) and Z decreases (i. e., weaker EM). The maximum value for the stress reduction in our simulations was 26.7 %. On the other hand, the minimum occurring stress can be more than 2.6× greater than we would expect it to be when only EM is considered. Even though compressive stress is considered less critical, this phenomenon should be investigated in order to prevent failures due to hillocks.

Consequently, technologies should be carefully characterized to obtain the material parameters relevant for migration robustness assessment. They are the prerequisites for precise chip modeling and migration verification. Please note, that Z and Q are only two of the parameters with a bearing on the steady-state stress profile. Other material properties, such as the specific resistivity, are also highly relevant – especially, as they vary with shrinking technology sizes. The specific resistivity, for example, increases in small technologies and thus affects EM and Joule heating (and, thus, TM) [1].

Unfortunately, information on these material properties is sparse in today's process design kits (PDKs). Our models are a foundation for technology characterization based on germane parameters that directly impact the steady-state stress distribution and, thus, migration robustness. Knowledge of these parameters is in our opinion crucial for future migration-robust IC design.

Our FEM models, including all material parameters used for simulations, are available online [26].

4.3 Stress Results for Short Wires

Finally, we compare our analytical model presented in Sec. 3.2 with the FEM simulations described in Sec. 3.1. Specifically, our goal is to estimate the error introduced by the assumptions made in [1] considering wire length. We found, that the results are in excellent agreement as long as $T_0 >> T_\mathrm{m}$ and $L >> \Gamma$. We improve the model from [1] by deriving the exact equation for the location of the stress maximum. Thus, we can precisely locate the point where the risk of voiding is greatest and calculate the stress. However, the shorter the wire length, the greater the calculation error than in the FEM simulation. Our model still accurately locates the maximum stress

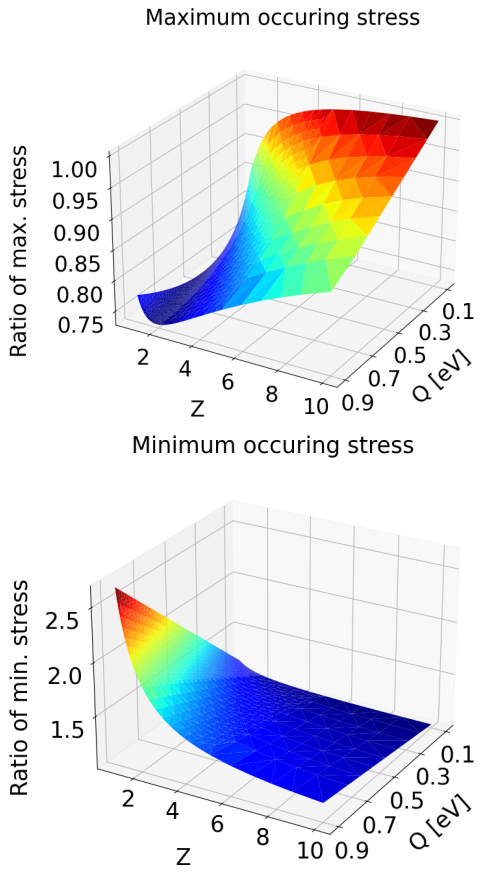

Figure 9: Stress extrema caused by combined EM and TM simulation normalized to the values that are found for EM simulation without considering TM for Z=[1,10] and Q=[0.1,0.9] eV (these are typical parameter ranges reported in literature). We simulated the same wire as in Fig. 8. It is obvious that knowing Z and Q is essential to perform migration robustness verification in a given technology.

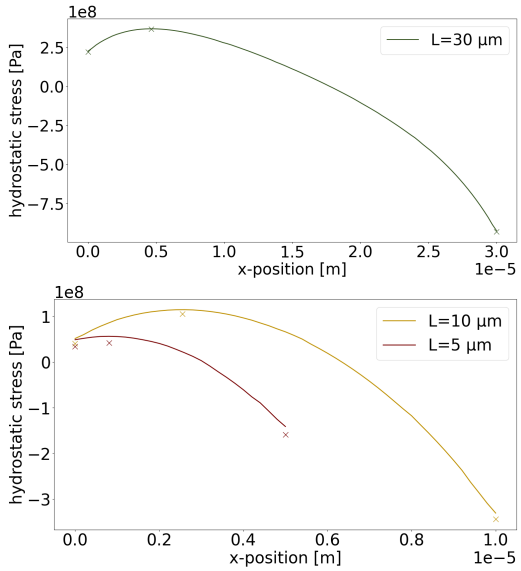

Figure 10: Comparison of our FEM results (solid lines, for constant specific resistivity) and the stress values calculated with the analytical model presented in Sec. 3.2 (marked with X) for wires with L=30 µm (green, upper diagram), 10 µm (yellow, lower diagram), and 5 µm (red, lower diagram). Our results show that the analytical solution underestimates the (positive) tensile stress and overestimates the (negative) compressive stress in shorter wires.

for shorter wires but underestimates tensile and overestimates compressive stress.

To illustrate this error, we plotted the stress profiles obtained by FEM simulation and the stress points calculated with the analytical method in Fig. 10. The green line (L=30 µm) represents the setup we used in Figs. 8 and 9. In this case, analytical and FEM solutions show excellent agreement. When the wire length is reduced, however, errors occur as in the simulations with L=10 µm and L=5 µm.

It is worth noting that the tensile stress error is even greater when using the FEM models with temperature-dependent resistivity and the danger of underestimating the risk of voiding is exacerbated (cf. Sec. 4.1).

Our results show that the available analytical models have reached their limitations for the simple case of straight wires. The stress profile in more complex (and thus, realistic) interconnect structures can only be estimated by analytical methods or by laborious simulation with FEM. This is especially true for AC lines where TM plays are greater role in the migration robustness assessment of these lines due to self-healing.

5 SUMMARY AND CONCLUSION

This work aims to close the gap in combined EM, TM, and SM simulation in AC lines. To this end, we introduce new models and utilize them, among other things, to characterize TM in AC lines (a factor that has been ignored up to now). We also revisit available models for combined EM, TM, and SM calculations and improve their precision. It should thus be possible to apply these models in the assessment of AC migration robustness – a measure that has been neglected so far but is fast becoming a hot topic in advanced technology nodes.

More specifically, we propose a novel methodology for combined EM, TM, and SM simulation in AC interconnects using FEM. Our models consider self-healing by integrating the self-healing factor into the diffusion equation for EM. Moreover, we supplement existing models for DC lines by taking into account the temperature dependency of the specific resistivity. Thus, our FEM models (publicly available [26]) can precisely calculate the temperature profile along a wire and the stress arising from TM.

In addition, we adapt existing analytical models for AC migration and improve their precision: We transfer the method for considering self-healing in the EM diffusion equation to the analytical solutions introduced in recent works. Furthermore, the equation for the exact location of the stress maximum on a straight wire is derived in this

paper. The equation for the temperature profile along the wire is also enhanced by considering temperature-dependent resistivity.

We can conclude from our results that TM indeed has significant impact on migration robustness – especially in AC lines where the EM effect is moderated by self-healing. Here, TM can potentially diminish the risk of voiding by reducing the tensile stress in a wire. However, it increases the compressive stress and, thus, the danger of hillock formation. What is more, AC lines cannot be assessed for their migration robustness with traditional models only, as they are unable to find the location of the stress maximum.

Sound knowledge about material parameters is mandatory for meticulous migration modeling. The steady-state stress profile is especially dependent on the specific resistivity, the effective charge number and the heat of transport – all of which must be determined for every technology. The temperature profile along the interconnect needs to be known for considering TM. However, calculating such a temperature profile remains a key challenge that has to be solved for more complex (and thus, realistic) interconnect structures and when taking the environment into consideration.

Finally, we note that our publicly available models [26] can be used for technology characterization. Subsequently, the obtained material parameters can be fed back into the models in order to use them for the verification of migration robustness of IC layouts.

ACKNOWLEDGMENTS

We would like to thank Dr. Steve Bigalke, on whose FEM models for EM [3, 4] we based our FEM models [26] presented in this paper.

REFERENCES

[1] Ali Abbasinasab. 2018. *Interconnect Aging – Physics to Software.* Ph. D. Dissertation. UC Santa Barbara. https://escholarship.org/uc/item/9t34j0zw.

[2] Ali Abbasinasab and Malgorzata Marek-Sadowska. 2018. RAIN: A tool for reliability assessment of interconnect networks—physics to software. In *2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC).* 1–6. https://doi.org/10.1109/DAC.2018.8465800.

[3] Steve Bigalke. 2020. *Erhöhung der Elektromigrationsrobustheit in der Verdrahtung digitaler Schaltungen.* VDI-Verlag GmbH, Düsseldorf. ISBN: 978-3-18-347220-8.

[4] Steve Bigalke and Jens Lienig. 2020. Avoidance vs. repair: New approaches to increasing electromigration robustness in VLSI routing. *Integration* 75 (2020), 189–198. https://doi.org/10.1016/j.vlsi.2020.04.009.

[5] James R. Black. 1969. Electromigration—A brief survey and some recent results. *IEEE Transactions on Electron Devices* 16, 4 (1969), 338–347. https://doi.org/10.1109/T-ED.1969.16754.

[6] Ilan A. Blech. 1976. Electromigration in thin aluminum films on titanium nitride. *Journal of Applied Physics* 47, 4 (1976), 1203–1208. https://doi.org/10.1063/1.322842.

[7] Liang Chen, Sheldon X.-D. Tan, Zeyu Sun, Shaoyi Peng, Min Tang, and Junfa Mao. 2020. A fast semi-analytic approach for combined electromigration and thermomigration analysis for general multi-segment interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2020), 1–1. https://doi.org/https://doi.org/10.1109/TCAD.2020.2994271.

[8] Ting-Yen Chiang, Kaustav Banerjee, and Krishna C. Saraswat. 2001. Compact modeling and SPICE-based simulation for electrothermal analysis of multilevel ULSI interconnects. In *IEEE/ACM International Conference on Computer Aided Design. ICCAD 2001. IEEE/ACM Digest of Technical Papers.* 165–172. https://doi.org/10.1109/ICCAD.2001.968613.

[9] Lucas de Paris, Gracieli Posser, and Ricardo Reis. 2016. Electromigration aware circuits by using special signal non-default routing rules. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS).* 2795–2798. https://doi.org/10.1109/ISCAS.2016.7539173.

[10] Lucas de Paris and Ricardo Reis. 2018. An automated methodology to fix electromigration violations on a customized design flow. In *2018 IEEE 9th Latin American Symposium on Circuits and Systems (LASCAS).* 1–4. https://doi.org/10.1109/LASCAS.2018.8399939.

[11] Zhong Guan and Malgorzata Marek-Sadowska. 2015. Atomic flux divergence-based AC electromigration model for signal line reliability assessment. In *2015 IEEE 65th Electronic Components and Technology Conference (ECTC).* 2155–2161. https://doi.org/10.1109/ECTC.2015.7159901.

[12] Xin Huang, Valeriy Sukharev, Taeyoung Kim, Haibao Chen, and Sheldon X.-D. Tan. 2016. Electromigration recovery modeling and analysis under time-dependent current and temperature stressing. In *2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC).* 244–249. https://doi.org/10.1109/ASPDAC.2016.7428018.

[13] IRDS. 2021. *IEEE International Roadmap for Devices and Systems (More Moore).* https://irds.ieee.org/editions/2021/more-moore

[14] ITRS. 2015. *International Technology Roadmap for Semiconductors 2.0 (ITRS 2.0).* http://www.itrs2.net/itrs-reports.html

[15] Wentian Jin, Liang Chen, Sheriff Sadiqbatcha, Shaoyi Peng, and Sheldon X.-D. Tan. 2021. EMGraph: fast learning-based electromigration analysis for multi-segment interconnect using graph convolution networks. In *2021 58th ACM/IEEE Design Automation Conference (DAC).* 919–924. https://doi.org/10.1109/DAC18074.2021.9586239.

[16] Wentian Jin, Sheriff Sadiqbatcha, Zeyu Sun, Han Zhou, and Sheldon X.-D. Tan. 2020. EM-GAN: data-driven fast stress analysis for multi-segment interconnects. In *2020 IEEE 38th International Conference on Computer Design (ICCD).* 296–303. https://doi.org/10.1109/ICCD50377.2020.00057.

[17] Mohammadamir Kavousi, Liang Chen, and Sheldon X.-D. Tan. 2022. Fast electromigration stress analysis considering spatial joule heating effects. In *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC).* 208–213. https://doi.org/10.1109/ASP-DAC52403.2022.9712535.

[18] Matt A. Korhonen, Peter Børgesen, King-Ning Tu, and Che-Yu Li. 1993. Stress evolution due to electromigration in confined metal lines. *Journal of Applied Physics* 73, 8 (1993), 3790–3799. https://doi.org/10.1063/1.354073.

[19] Ki-Don Lee. 2012. Electromigration recovery and short lead effect under bipolar- and unipolar-pulse current. In *2012 IEEE International Reliability Physics Symposium (IRPS).* 6B.3.1–6B.3.4. https://doi.org/10.1109/IRPS.2012.6241869.

[20] Jens Lienig and Matthias Thiele. 2018. *Fundamentals of Electromigration-Aware Integrated Circuit Design.* Springer, Cham. https://link.springer.com/book/10.1007/978-3-319-73558-0.

[21] Jens Lienig and Matthias Thiele. 2018. The pressing need for electromigration-aware physical design. In *Proceedings of the 2018 International Symposium on Physical Design.* 144–151. https://doi.org/10.1145/3177540.3177560.

[22] M. H. Lin and A. S. Oates. 2013. AC and pulsed-DC stress electromigration failure mechanisms in Cu interconnects. In *2013 IEEE International Interconnect Technology Conference - IITC.* 1–3. https://doi.org/10.1109/IITC.2013.6615556.

[23] M. H. Lin and A. S. Oates. 2015. Mechanisms of electromigration under AC and pulsed-DC stress in Cu/low-k dual damascene interconnects. In *2015 IEEE International Reliability Physics Symposium.* 2D.2.1–2D.2.6. https://doi.org/10.1109/IRPS.2015.7112681.

[24] Farid N. Najm. 2021. Equivalent circuits for electromigration. *Microelectronics Reliability* 123 (2021), 114200. https://doi.org/10.1016/j.microrel.2021.114200.

[25] Gracieli Posser, Sachin S. Sapatnekar, and Ricardo Reis. 2017. *Electromigration Inside Logic Cells.* Springer. https://link.springer.com/book/10.1007/978-3-319-48899-8.

[26] Susann Rothe. 2023. *FEM Models (APDL Scripts) developed an presented in this work.* https://github.com/IFTE-EDA/MigrationFEM

[27] Susann Rothe and Jens Lienig. 2022. Reliability by design: avoiding migration-induced failure in IC interconnects. In *2022 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI).* 1–6. https://doi.org/10.1109/SBCCI55532.2022.9893237.

[28] Bernhard Sell et al. 2022. Intel 4 CMOS technology featuring advanced FinFET transistors optimized for high density and high-performance computing. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits).* 282–283. https://doi.org/10.1109/VLSITechnologyandCir46769.2022.9830194

[29] Zeyu Sun, Ertugrul Demircan, Mehul D. Shroff, Taeyoung Kim, Xin Huang, and Sheldon X.-D. Tan. 2016. Voltage-based electromigration immortality check for general multi-branch interconnects. In *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD).* 1–7. https://doi.org/10.1145/2966986.2967083.

[30] Sheldon X.-D. Tan, Mehdi Tahoori, Taeyoung Kim, Shengcheng Wang, Zeyu Sun, and Saman Kiamehr. 2019. *Long-Term Reliability of Nanometer VLSI Systems.* Springer, Cham. https://doi.org/10.1007/978-3-030-26172-6.

[31] L. M. Ting, J. S. May, W. R. Hunter, and J. W. McPherson. 1993. AC electromigration characterization and modeling of multilayered interconnects. In *31st Annual Proceedings Reliability Physics 1993.* 311–316. https://doi.org/10.1109/RELPHY.1993.283282.

[32] Chen Zhou, Xiaofei Wang, Rita Fung, Shi-Jie Wen, Rick Wong, and Chris H. Kim. 2015. High frequency AC electromigration lifetime measurements from a 32nm test chip. In *2015 Symposium on VLSI Technology (VLSI Technology).* T42–T43. https://doi.org/10.1109/VLSIT.2015.7223696.

[33] Chen Zhou, Xiaofei Wang, Rita Fung, Shi-Jie Wen, Richard Wong, and Chris H. Kim. 2017. A circuit-based approach for characterizing high frequency electromigration effects. *IEEE Transactions on Device and Materials Reliability* 17, 4 (2017), 763–772. https://doi.org/10.1109/TDMR.2017.2772193.