Embedded Tutorial:
Electromigration-Aware Physical Design of Integrated Circuits

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Abstract

The electromigration effect within current-density-stressed signal and power lines is an ubiquitous and increasingly important reliability and design problem in sub-micron IC designs. It is therefore necessary to consider electromigration-related design parameters as early as possible in the physical design flow. In this tutorial, we first give an introduction into the electromigration problem and its relationship to current density and temperature. Physical design parameters that affect current density are presented next. We then focus on various distinctive methodologies that allow the electromigration problem to be addressed directly during physical design and verification of both analog and digital circuits. We also present and discuss commercial applications of these electromigration-aware methodologies.

1. Introduction

The term "electromigration" is applied to mass transport in solid state metals when the metals are stressed at high current densities. This might result in a steady change of conductor dimensions, thereby causing the creation of either voids or the creation of hillocks and whiskers in the affected regions. Both can eventually lead to the failure of the circuit.

The ongoing reduction of circuit feature sizes has aggravated the problem of electromigration in integrated circuits to a level where this problem cannot be ignored any longer. Since manual current-density considerations within complex circuits are extremely time-consuming and error-prone, automatic methodologies for current-dependent routing, verification and post-route layout modifications are urgently needed.

This tutorial addresses electromigration-related problems and solutions as seen from both a designer's as well as a tool developer's point of view. While most solutions presented are for analog and mixed-signal designs, electromigration is also increasing as a factor in sub-micron digital designs.

Firstly, we give an introduction into the physical background of electromigration.

Secondly, we discuss electromigration-related design parameters. We show that current density and temperature are the main parameters circuit designers must consider when addressing the electromigration problem during layout generation. We present solutions to the problem of obtaining realistic current values. We also elaborate on effective calculation methods of wire widths and the number of required vias with respect to current density, temperature, etc.

Thirdly, three distinctive methodologies will be presented that allow an automatic consideration of current densities within the automatic design flow of integrated circuits. Each of these methodologies can either be applied separately or they can be combined within the design flow in order to increase the design efficiency.

2. The Electromigration Problem

The physics of electromigration and its effect on interconnect lifetime have been studied extensively over the last decades [2]-[4][25]-[31][36][37]. Despite the fact that the overall understanding of the effect already improved dramatically, many problems are still to be addressed.

The copper or aluminum interconnects of a chip are polycrystalline, i.e., they consists of grains of lattice. While conducting a current through an interconnect, the electrons interact with atoms in the metal lattice, causing them to migrate in the direction of the electron flow [3][29]. This material transport mainly occurs at the metal-dielectric interface (surface diffusion) and at the boundaries between the grains (grain boundary diffusion) [3][4][25][26].

In the direction of the electron flow, copper or aluminum atoms will be deposited over time. This results in the generation of hillocks and the buildup of mechanical stress around the hillock area. While hillocks might cause shorts with neighboring interconnects, the buildup of mechanical stress can lead to cracks in the surrounding insulation layers. Subsequently, material migration towards these cracks can generate so-called whiskers which might also introduce shorts to neighboring wires. In the opposite direction, voids will grow between the metal-dielectric interface and at grain boundaries. Voids reduce the conductivity of the affected interconnects over time, which can eventually lead to interconnect failures. It should be noted that the generation of hillocks and voids represents a self-accelerating effect cycle [3][29].

The growth of voids and hillocks within the metallization often starts at so-called "triple points". A triple point represents the location where grain boundaries belonging to at least three grains meet (Fig. 1). Most triple point configurations are characterized by a divergence in the material flux caused by a difference in the number of inbound and outbound transport paths. In case there are one inbound and two outbound transport paths at the triple point, a void creation will occur, otherwise (two inbound and one outbound paths), a hillock will be formed.

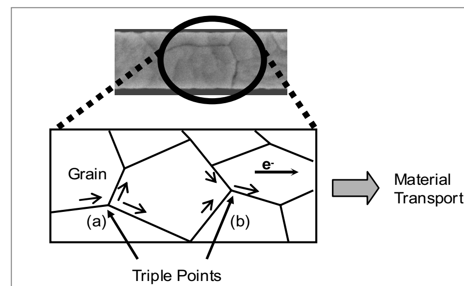

Fig. 1. Diffusion paths at triple points leading to the creation of voids (a) and hillocks (b).

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An interesting effect occurs with so-called "bamboo wires" where the grain diameter exceeds the wire width. In this case, most grain boundaries are perpendicularly located with regard to the electron flow. Thus, there are almost no grain boundary transport paths available. This leads to an increased resistance against electromigration despite the fact that these wires are very narrow [3].

It is known that pure copper used for Cu-metallization offers a much better resistance against electromigration than aluminum. This is mainly due to its higher electromigration activation energy levels caused by its superior electrical and thermal conductivity as well as its higher melting point [4][26]. Alternatively, the Al-metallization material can be alloyed with small amounts of copper and silicon (AlSiCu) in order to reduce the migration effect by increasing its electromigration activation energy as well [3][25].

Grain boundary diffusion is prevalent for Al-metallization [3] [25] while surface diffusion prevails for Cu-metallization [4][26]-[28]. Grain boundary diffusion leads to the growth of voids and hillocks at the grain boundary. Examples for surface diffusion in copper metallization are line and via depletion observed at the copper-to-trench interface (liner) and at the copper-to-inter-level-diffusion-barrier interface (cap) [4] (Fig. 2).

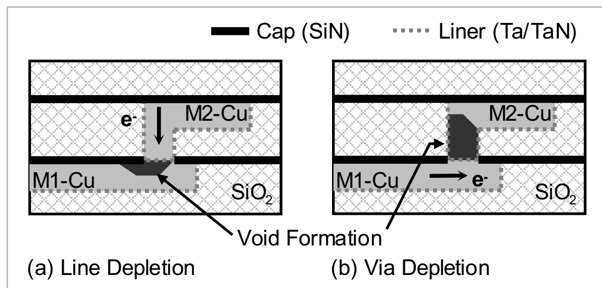

Fig. 2. Line and via depletion in a copper metallization.

It should be noted that the mechanical stress built up in the hillock area also causes a reversed migration process which can reduce or even compensate the effective material flow towards the anode. I. A. Blech stated in [1] that a conductor line is not susceptible to electromigration if the product of current density j within the wire and its length l is smaller than a process-technology-dependent threshold value $(jl)_{Threshold}$. Exploiting this compensation effect enables the design of so-called "immortal wires" that are not susceptible to the above-mentioned electromigration failure mechanisms [5][28][36].

3. Physical Design and Electromigration

3.1. Wire Lifetime and Current Density

All chip interconnects must guarantee a predefined mean time to failure (*MTTF*). Failure due to electromigration for a single wire is usually expressed by the empirical equation of Black ("Black's law") [2]:

$$MTTF = \frac{A}{j^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \tag{1}$$

where A is a cross-section-area-dependent constant, j is the current density, E_a is the effective activation energy of the electromigration failure process, k is the Boltzmann constant, T is the temperature and n a scaling factor (usually set to $n \approx 2.0$ according to Black [2] and experiments reviewed in [3]).

As is obvious from Eq. (1), the *MTTF* due to electromigration depends on two factors that can be influenced by the chip designer: current density j and temperature T. Hence, any algorithmic approach for electromigration-aware physical design must ensure that the maximum actual current density j within the interconnects does not exceed a temperature-dependent maximum permitted current-density limit.

3.2. Obtaining Realistic Current Values

There exist three relevant models of current values for electromigration-aware design: (1) root-mean-square currents (RMS), (2) average currents and (3) peak currents.

The **RMS-current**-based model is most exact for current frequencies below 1 Hz. It does not consider the so-called self-healing effect. (Self healing represents the reduction of the overall material migration due to reversed material flows caused by alternating current directions [34].) This model represents a more conservative approach and, hence, it is suitable for all analog DC nets and reliability-critical applications in general.

The **average-current**-based model considers the self healing effect of alternating current directions. It is suitable for analog AC and digital nets with current frequencies greater than 1 Hz [34].

A **peak-current** flow (such as short-time current flows due to an ESD event) has to be considered separately from RMS- or average-current-based model. This is due to different damaging effects within the metallization resulting in different design rules for conductor dimensioning [37].

A problem for any current-driven design methodology is the determination of realistic current values for each net terminal. Extensive studies have been conducted by various authors to address this issue [33]-[35][37]. Most of these presented approaches use a *single* so-called "equivalent current value" (by considering the current waveform, duty cycle and frequency) which is attached to the net terminal. However, single current values are not sufficient in order to calculate currents in various Steiner point connections. For example, the current within a Steiner point connection is underestimated in case of directly connected net terminals with reversed and compensating worst case currents flows.

In this tutorial, we present three current value models that are capable of resolving the above mentioned current value propagation problem by utilizing either a single current value pair or a vector of current value pairs. Within each value pair, the first entry represents the most negative current value, i.e. the lower bound i_{min} of the current value range. The second entry of a current value pair represents the most positive current value, i.e. the upper bound i_{max} of the current value range.

In our *first* current value model, all results from one or more simulations are post-processed by calculating a set of **current vectors** satisfying Kirchhoff's current law [11]. They represent a snapshot of the circuits operation at the time of minimum and maximum currents at each terminal. This reduces the simulation results to a vector of "worst case" current value ranges. For a net with m terminals, this may lead to up to m current value pairs attached to each terminal $i_{terminal}$:

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$i_{terminal} = [[i_{i_min(terminal_1)}, i_{i_max(terminal_1)}],$
$[i_{i_min(terminal_2)}, i_{i_max(terminal_2)}],$
$\ldots$
$[i_{i_min(terminal_m)}, i_{i_max(terminal_m)}]],$

(e.g., $i_{terminal} = [[-2mA, -1mA], [0, +1\text{mA}], \ldots, [-2\text{mA}, 0]]$).

The *second* approach uses one **time-*independent* current value pair** (i.e., a minimum and a maximum current value) per net terminal. This current pair is obtained either by circuit simulation, by manual attachment to the net terminal in the schematic, or derived from a device library. This model offers a very simple, fast and worst case solution to the current value problem but (due to its time independency) "over-designs" wires since it cannot relate worst case currents to their time of appearance.

$i_{terminal} = [i_{min}, i_{max}]$, (e.g., $i_{terminal} = [-1mA, +3mA]$).

A *third* approach extends the second model by introducing a time-slot dependency of the current flow. Hence, this model utilizes **a vector with one current value pair for each of *n* time-slots S_x** ($x = 1 \ldots n$) to account for independent current flow events originated by multiple net terminals. The minimum and maximum current values of a current value pair are determined between the start and end time of the particular time-slot:

$i_{terminal} = [[S_1, i_{min_1}, i_{max_1}], [S_2, i_{min_2}, i_{max_2}], \ldots, [S_n, i_{min_n}, i_{max_n}]]$

(e.g., $i_{terminal} = [[S_1, -1mA, +3mA], [S_2, +2mA, +3mA], \ldots]$).

Due to our experience, we recommend that tools within an electromigration-aware design flow are "open" to all three approaches in order to utilize their widely varying characteristics with regard to different applications.

3.3. Wire and Via Sizes and Temperature Consideration

Eqs. (2)-(4) have been shown to be most accurate for calculating the **wire width** $w_{nom}(T_{ref})$ derived from maximum permitted current-density limits $j_{max,eq}$ and $j_{max,peak}$ determined for a specific reference temperature T_{ref}. These equations also include the nominal layer height h_{nom}, a process-dependent minimal wire width $w_{min_process}$, and the equivalent RMS- or average- and peak-currents $i_{s,eq}$ and $i_{s,peak}$. These currents represent the worst case current values or propagated current value sums from the current vectors $i_{terminal}$ (Section 3.2.):

$$w_{nom}(T_{ref}) = \max \begin{cases} \dfrac{i_{s,eq}}{j_{max,eq}(T_{ref}) \cdot h_{nom}}, & (2) \\ \dfrac{i_{s,peak}}{j_{max,peak}(T_{ref}) \cdot h_{nom}}, & (3) \\ w_{min_process}. & (4) \end{cases}$$

According to Eq. (1), an increase in temperature reduces the maximum permissible current density in order to maintain a specific *MTTF* of the interconnect. Hence, a temperature scaling factor $f(T)$ can be derived from Eq. (1) which takes this current-density reduction into account. Please note that $f(T)$ is only of importance if the actual working temperature T is different to the reference temperature T_{ref} that has been used to determine the maximum current-density limits in Eqs. (2)-(3):

$$f(T) = \exp\left(-\frac{E_a}{n \cdot k \cdot T_{ref}} \left(1 - \frac{T_{ref}}{T} \right) \right) \quad (5)$$

where E_a, n and k denote parameters already defined in Eq. (1).

In addition to temperature scaling if $T \neq T_{ref}$, the determination of the final wire width $w(T)$ must also consider technology characteristics, such as the ratio between nominal and minimum layer height (h_{nom} / h_{min}), wire width variation Δw, and the etch loss w_{etch}:

$$w(T) = \left(w_{nom}(T_{ref}) \cdot \frac{h_{nom}}{h_{\min}} + \Delta w \right) \cdot f(T) + w_{etch} \quad (6)$$

The **adjustment of vias** to current density is usually performed by replacing a single via with a via array and/or adjusting the number of vias in a via array. The temperature-dependent number of single vias $n_{via}(T)$ required within a via array is determined by Eq. (7):

$$n_{via}(T) = \text{ceil}\left(\frac{i_{s,eq}}{i_{single_via}(T_{ref})} \cdot f(T) \cdot g(H) \right) \quad (7)$$

where $i_{s,eq}$ represents the worst case equivalent current the via array must sustain, i_{single_via} characterizes the maximum permissible current value of a single via at reference temperature T_{ref}, and $f(T)$ is obtained as in Eq. (5). The factor $g(H)$ accounts for the inhomogeneity of the current flow. According to our FEM simulations, it is set to $g(H) = 1.0$ in case of an homogeneous current flow, otherwise, $g(H)$ is set to $g(H) > 1.0$ to account for an inhomogeneous current flow.

Jeon et al. [30] and Nguyen et al. [39] studied the so-called reservoir effect. Both conclude that the MTTF with regard to electromigration of a via array depends not only on the current density but also on the available via-metal overlap. A larger metal overlap prolongs the via lifetime due to its larger available "reservoir" of migration-capable material.

4. Physical Design Methodologies Addressing Electromigration

4.1. Overview

As any extensive literature survey reveals, there exist various methodologies to address the problem of designing reliable interconnect systems with regard to electromigration.

Firstly, while using standard routing tools, a critical net is assigned to an "assumed save" net class with predefined and fixed routing widths. Despite its widespread application within many design flows, this approach cannot *guarantee* current-density correctness in every case. For example, any inauspicious net topology can lead to current-density-overstressed net segments due to the prior determination of fixed routing widths of these segments. Hence, this approach is not further considered in this paper.

Secondly, the routing is performed with a current-flow-aware and, hence, current-density-driven wire planning and routing tool (e.g., [6][7][11][12]). We elaborate on this approach in Section 4.2.

A third methodology performs a current-density verification of any routing structure and, thus, enables an automatic current-density DRC (e.g., [8][9][21]-[24]). The details of these

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methodologies are presented in Section 4.3.

A fourth approach, discussed in Section 4.4., performs a post-route cross-section area adjustment of critical interconnect structures [10]. This approach requires a sophisticated current-density-calculation tool in order to utilize layout-based current-density data for correct wire and via array sizing.

4.2. Current-Driven Wire Planning and Routing

Most current-driven routing strategies have been applied so far to layout generation of **power and ground nets in digital circuits**. In these cases, the generation of power supply interconnects is usually done prior to signal routing in order to achieve a planar (i.e., single layer) implementation.

The first automatic approaches to power and ground routing were presented in the 1980's [13]-[20] and usually involve three steps: interconnection topology construction, wire width determination, and layout generation. The interconnection topology is determined by using a standard wire width, and then based on that topology, branch currents are calculated. Afterwards, all wires are widened with respect to their current flow. This might result in DRC errors that must be resolved in a separate post-processing step which may require modifications of the cell placement.

A floorplan-based planning methodology for power connections has been presented in [19]. Here, a global power trunk and a block-level local power network are first generated from the floorplan, and then optimized regarding their widths. An alternative approach to optimize power and ground networks is described in [20], where the authors present a fast linear programming method that optimizes the power and ground area subject to current density and IR-drop.

Recently, Magma Inc. introduced Blast Fusion® and Blast Noise® in order to achieve a current-density-correct routing of **digital signal nets** [38]. The problem of obtaining correct values of net segment currents is circumvented by considering only *one* single current from *one* driving gate output and distributing it to the inputs of multiple receiving gates.

Pulsic Ltd. offers an integrated routing solution Lyric AMS™ for **analog and mixed-signal IC designs** with the consideration of pin currents for current-density-correct routing [32]. Detailed information about their approach has not been published yet.

The major challenge facing any current-driven signal routing is the inherent feature that segment currents are only known *after* the entire topology of the net has been laid out. A current-driven signal router must therefore solve the problem of altering current strengths in a prior routed sub-net whenever a new terminal is linked to the net. In other words, the sequence of *all* terminals to be connected must be known in order to allow for a current calculation based on Kirchhoff's current law even when routing only the first segments of a net.

In order to address this issue, the approaches of current-driven signal routing in [6][7][11][12] are focused on generating current-correct Steiner/routing trees *prior* to detailed routing. Of special interest here are the approaches published in [7][11]. Both consist of current characterization, current-driven wire planning and a conventional detailed routing with *variable* wire widths.

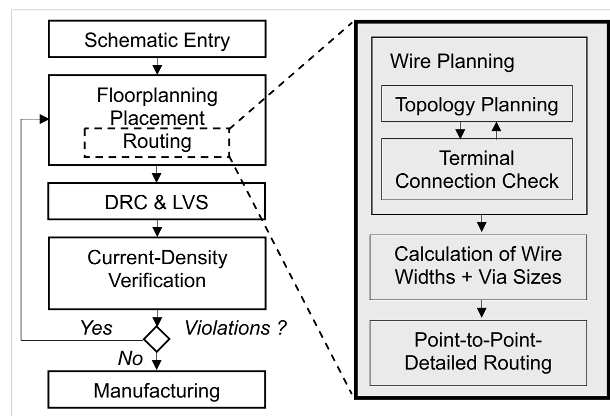

Fig. 3. Current-density-driven routing flow.

An overview of a current-density-driven routing flow is given in Fig. 3. The routing stage is divided into three individual steps: (1) wire planning consisting of net topology planning and terminal connection checking, (2) calculation of required wire and via array dimensions and (3) the final routing of the planned point-to-point-connections utilizing a detailed router.

During wire planning, a current-driven net topology is determined by calculating an optimized routing tree. Its major characteristic is *concurrent* wire planning and segment current calculation.

A specific problem arises with the required current-density-correct connection to arbitrarily shaped net terminals, e.g., pins of DMOS transistors (Fig. 4). The layout of these terminals is an integral part of the interconnect system and, hence, the current-strength capabilities of net terminals to be connected have to be verified during wire planning.

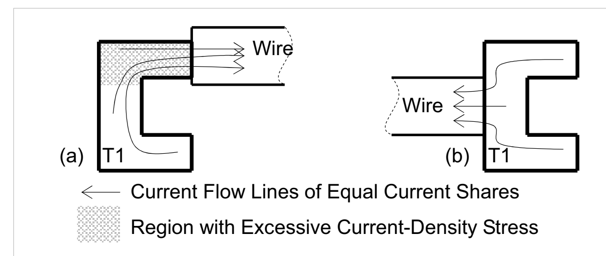

Fig. 4. The problem of current-density-correct connections to net terminals. Incorrect connection to an U-shaped terminal T1 (a) and a current-density-correct terminal connection (b).

After the net topology is defined, the obtained net segment currents are used to calculate the correct layout sizes for wires and via arrays utilizing Eqs. (6) and (7).

Since currents have already been taken into account during this planning phase, the detailed routing is then considered to be a point-to-point routing with known wire and via array sizes.

An example of the final routing result obtained with the described methodology is depicted in Fig. 5.

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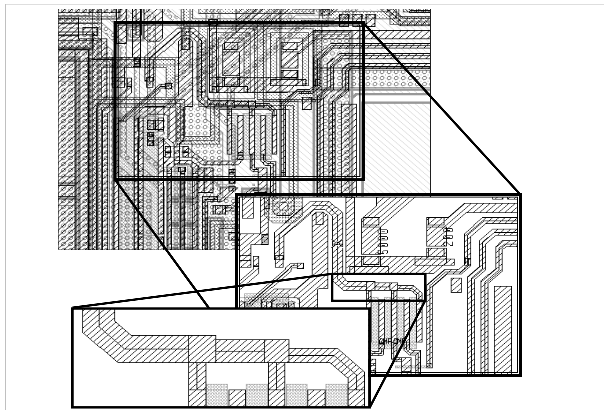

Fig. 5. Excerpt of an analog circuit routed with a current-driven router [7] with adjusted routing widths between layout Steiner points.

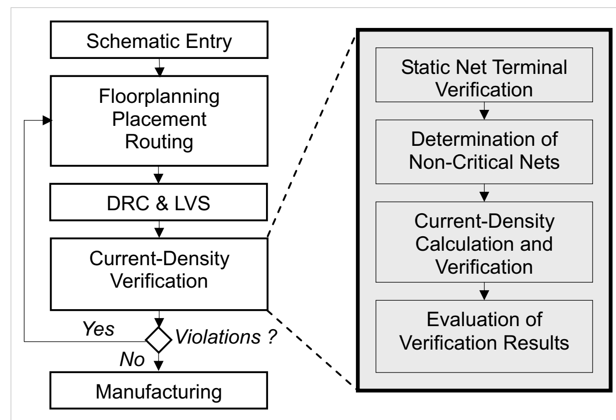

Fig. 6. Current-density verification flow.

4.3. Verification of Current Densities

The task of current-density verification is to validate that the maximum current densities occurring within the metallization will not exceed the maximum permitted current density for the predefined working temperature of the chip.

Several electromigration analysis systems, which are limited to the verification of **digital designs**, have been presented [21]-[24]. Hajj et al. [21] reported a CAD system for electromigration analysis based on current-density investigation for relatively simply shaped layout patterns in CMOS circuits. The approach divides the layout structure into several simple shapes that are combined in an RC network. Each element of the network is then simulated independently. Simplex Solutions [22] introduced "Thunder&Lightning™," a commercial tool set for electromigration analysis of power and ground networks as well as for digital signal nets. OEA International Inc. [23] with "P-Plan™" and Cadence Inc. [24] with "ElectronStorm™" also provide commercial verification systems for electromigration and Joule heating in power and signal nets in digital applications.

The current-density simulator for **analog applications** published in [6] decomposes all wires into rectangles and irregularities. The resistance of the rectangles is calculated and then used to extract a netlist that incorporates references to the corresponding geometrical dimensions. Irregularities with inhomogeneous current distribution, such as wire bends, pins and vias, cannot be validated with this approach.

To the best of our knowledge, only one approach has been published so far that verifies current densities in arbitrarily shaped layout structures as commonly used in analog circuits and analog blocks of mixed-signal designs [8]. This approach includes a quasi-3D model to verify irregularities such as vias and incorporates thermal simulation data to account for the temperature dependency of the electrical field configuration and the electromigration process. It consists of four steps: (1) the static current-density verification of net terminals, (2) the determination and de-selection of non-critical nets, (3) the calculation of current densities within the given metallization layout, and (4) the evaluation of the obtained violations (Fig. 6).

First, a static current-density verification of net terminals is performed to ensure that the metallization of the net terminals sustain the assigned current values.

Non-critical nets are excluded from further checking. The criticality of a net is determined using the sum of the worst case current values of each terminal. If this sum is smaller than the maximum permitted current on the minimum sized and most electromigration-endangered metallization layer, then this net is excluded.

The current density within the metallization can either be calculated directly (e.g., using the FEM method as in [8]) or it can be derived from a prior determination of net segment currents [6][23][24]. The latter method is very fast but it is only applicable to Manhattan-style layouts (i.e., for digital designs) with a fixed path width since it cannot consider inhomogeneous layout regions.

After determining the violating layout regions, the verification results must be evaluated to separate "dummy errors" (e.g., current-density spots at corner coordinates) from real violations.

An example of a verification result is depicted in Fig. 7.

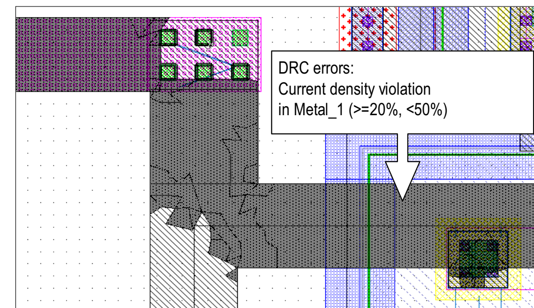

Fig. 7. Excerpt of a current-density verification layout with a flagged violation area marked in dark grey [8].

4.4. Current-Driven Decompaction of the Interconnect

In order to avoid a repeated place and route cycle when addressing current-density verification errors, current-driven decompaction has been shown to be an effective point tool. Its major goals are the post-route adjustment of layout segments according to their actual current density and a homogenization of the current flow.

Only one such decompaction approach which is applicable to *arbitrary* tree-based nets has been published so far [10]. It utilizes a current-density verification tool (Section 4.3.) to identify regions with excessive current-density stress. Using these provided cur-

rent-density data, this methodology performs four steps: (1) layout decomposition, (2) wire and via array sizing, (3) addition of support polygons, and (4) layout decompaction (Fig. 8).

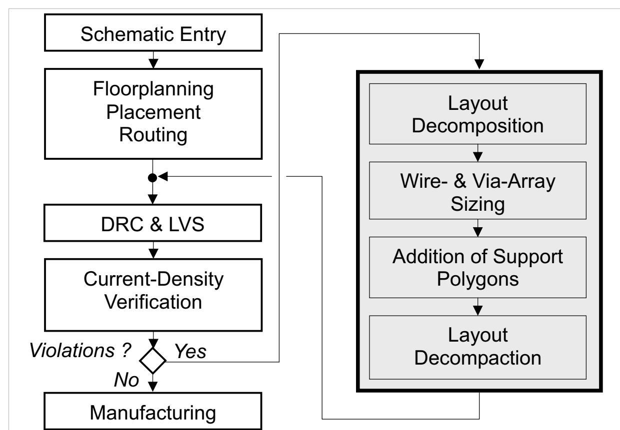

Fig. 8. Current-driven layout decompaction flow.

During layout decomposition, all net segments will be retrieved from the given net layout. The end points of each segment (i.e., net terminals or layout Steiner points) then represent either (artificial) current sources or current sinks.

The current within a net segment is retrieved from the location-dependent current-density data obtained from the prior current-density calculation. This current value is then used to calculate the appropriate cross-section areas of critical wires and via arrays according to Eqs. (6) and (7).

The addition of so called "support polygons" to critical layout corners (e.g., wire bends) and around net terminals is required to reduce the local current-density stress if wire widening is not applicable or sufficient.

The final layout decompaction with cross-section area adjustment can be performed with any layout decompaction tool capable of (1) simultaneous compaction and decompaction of layout structures, and (2) preserving the net topology [10].

An example of a current-driven layout decompaction is depicted in Fig. 9.

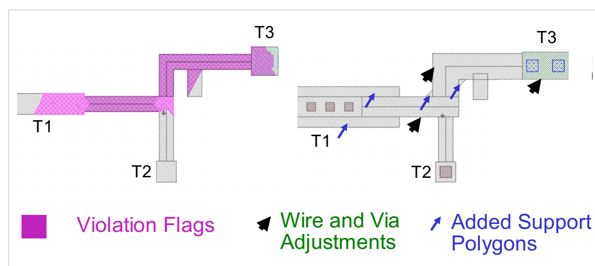

Fig. 9. Net with current-density violation flags (left) and net and via layout after current-driven layout decompaction (right) [10].

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