Early-Stage Determination of Current-Density Criticality in Interconnects

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***Abstract*—Excessive current density within interconnects is a major concern for IC designers, which if not effectively mitigated leads to electromigration and electrical overstress. This is increasingly a problem in modern ICs due to smaller feature sizes and higher currents associated with lower supply voltages. Detailed analysis of all interconnect nets is both time-consuming and cannot be done until physical design is complete, when it is too late for easy fixes. To address these problems, we introduce (i) a powerful terminal current model and (ii) an efficient methodology to determine the worst-case bounds on segment currents of the interconnect. This early-stage calculation enables nets to be separated into critical and non-critical sets; only the set of critical nets, which is typically considerably smaller, requires subsequent special consideration during physical design and layout verification due to current density design limits. The presented algorithms are fast enough to run on every net, and work with known and unknown net topology, leading to several practical uses, such as (i) the pre-layout identification of nets that are potentially troublesome and may need sizing, (ii) as filter to avoid time-consuming detailed current-density analysis of net layouts, and (iii) to evaluate the effect of interconnect temperature and process changes on the number and distribution of current-density-critical nets.**

I. Introduction

Electromigration is a mid- and long-term reliability issue that can cause opens and shorts in IC interconnect structures. Electromigration is primarily caused by high current densities in interconnect structures in combination with high ambient temperatures [1]. Failures due to electromigration are avoided by obeying current-density design rules.

Electrical overstress is a short-term reliability issue that, among others, causes opens in interconnect structures due to a continuous interconnect material degradation or due to a sudden material melt or evaporation [2], [3]. Failures due to electrical overstress are primarily caused by over-current conditions such as current flows that cause excessive Joule heating in interconnects or high-energy pulses of electrical discharge current flows that may occur during the assembly of a chip or chip-package. These interconnect failures are also addressed by current-density design rules that are dependent on the specific failure mode and the utilized technology.

The ongoing reduction of on-chip feature dimensions is generally not accompanied by a similar reduction of the current flow in interconnects. Among several reasons, this is due to high leakage currents, the high currents associated with low voltage operation and large currents that cannot be down-scaled due to their intended function. This leads to an increasing percentage of interconnects with a potential susceptibility to electromigration and electrical overstress failures caused by excessive current density.

Current density must hence be considered as a relevant design constraint by physical design and verification tools in order to guarantee an adequate interconnect failure robustness within any analog, smart-power, mixed-signal and digital IC. This is achieved by sizing each interconnect wire, via and contact array (via array) such that it complies with current-density design rules.

The impact of current flow on the design of today's deep sub-micron analog, smart-power and mixed-signal ICs is comparable to the impact of timing in digital IC applications. Seen from a design perspective, the design problems for electromigration and electrical overstress failure avoidance are identical as current-density limits in interconnects must be considered in both cases. It is of great interest to identify all nets that are susceptible to current-density-related failures as early as possible in the design process to avoid late layout changes.

To address these problems, we introduce an efficient methodology to compute bounds on worst-case segment currents in the interconnect. These bounds allow the determination of *critical nets* that are susceptible to either electromigration or electrical overstress failures or both. Critical nets do require interconnect sizing and detailed current-density verification. *Non-critical* nets are considered to be neither susceptible to electromigration nor to electrical overstress failures. Reducing the problem size in this way significantly speeds up the layout generation and design verification without compromising design reliability.

The determination whether a net is critical or not is subsequently denoted as the "Net Current-Density Criticality Problem (NCP)". This design problem is introduced and analyzed in this paper for the first time. Based on the theoretical analysis of this problem, we have developed several complementary algorithms to address the NCP for nets with known and unknown net topology. (The term "net topology" hereby refers to the topology of the layout connection graph. Each net segment represents an edge in this graph.)

We prove that the topology-unknown problem is $\mathcal{NP}$-complete under certain conditions and that the topology-known problem can always be solved in polynomial time. The algorithms are fast enough to run on every net, leading to several practical uses that we describe.

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The provided algorithms utilize a new model for electromigration and electrical overstress relevant equivalent currents at net terminals (Static Terminal Current Model, TCM-S) which is introduced in this paper. This simple, yet powerful and safe model facilitates the reduction of lengthy terminal current vectors derived from one or more transient circuit simulations to a small number of failure relevant equivalent currents, such as average, root-mean-square and peak currents. This data reduction enables for the first time an efficient and thorough consideration of terminal currents (rather than large current vectors) for current-density-aware physical design tools (e.g., current-driven floorplanners, PCell generators, placers, routers, compaction tools) as well as for electromigration and electrical overstress verification tools [4]–[7].

Since the presented algorithms work with unknown net topology, they can be used for a pre-layout design analysis in order to recognize critical nets that would need wire and via array sizing. Furthermore, our algorithms also identify critical nets after layout generation, thereby limiting the time-consuming current-density verification and adjustment effort only to those nets. Finally, our approach is utilized to study the impact of temperature changes or technology variants on the number of potentially critical nets throughout the IC design hierarchy.

The paper is structured as follows. The previous work is discussed in Section II. In Section III, we present the new model for terminal current values. The net criticality problem is formally introduced and analyzed in Section IV. Section V introduces and discusses several complementary algorithms to identify critical and non-critical nets based on either known or unknown net topology. We present application aspects and experimental results in Section VI. Finally, we summarize our contributions in Section VII.

II. Previous Work

Electromigration (EM) has been extensively studied over the last decades due to its substantial impact on IC reliability. In 1969, Black [1] introduced the so-called "Black's Law" which empirically correlates the interconnect current density with the mean-time-to-failure of interconnects while considering several material properties of the IC metallization system and the ambient temperature. The primary physical processes that lead to EM-related interconnect failures are different for aluminum and copper metallization systems as discussed in [1], [8] and [9]–[12]. An overview on electromigration is given in [13]–[15].

Electrical overstress (EOS) is a short-term reliability issue either caused by high-energy pulses of electrostatic discharge current flows that may occur during the chip and chip-package assembly [2], [16]–[18] or other over-current conditions [3]. Electrostatic-discharge-aware IC design issues have been discussed in [19] and [20].

The shape of the transient current waveform has a direct impact on the EM and the EOS failure effect as shown in [17], [18], [21]–[24]. It was found by these authors that the electromigration failure effect is almost reversed due to a self-healing mechanism in case the interconnects conduct only bi-directional currents.

The exclusive use of only one equivalent current value per current source or sink, as implied by [17], [18], [21]–[23], limits the correct worst-case current calculation to nets with pure DC current flow only. In case of non-DC current flows, it is provably not possible to determine the worst-case equivalent currents between layout Steiner points with just single equivalent currents as can be seen in Section III. Our presented terminal current model addresses this problem by introducing lower- and upper-bounds on the utilized equivalent currents.

To the best of our knowledge, neither the net criticality problem and its solution nor a safe terminal current model without large transient vectors have previously been published in the literature. A design analysis based on the net criticality status (Section VI) is firstly introduced in this paper as well.

III. The Static Terminal Current Model

In general, a terminal current model represents a model to describe the current flow at each net terminal. This section introduces a Static Terminal Current Model (TCM-S) that is used to model the current flow relevant for EM and EOS failure avoidance. The presented model stores the current information as a terminal-specific set of annotated equivalent currents. This set contains the average, the root-mean-square and the peak currents that were derived from transient current waveforms. The TCM-S represents a static model due to its exclusive use of annotated and constant equivalent currents.

An EM- and EOS-robust layout design is achieved by simultaneously taking the average (AVG), the root-mean-square (RMS), the peak (PEAK) equivalent currents (current types) and their corresponding current-density limits into account. Each equivalent current type is linked to a corresponding current-density design rule to account for the individual EM and EOS failure mechanism.

The complex topic of deriving terminal currents is beyond the scope of this paper and hence omitted here. It is subsequently assumed that (i) a set of transient circuit simulations has been previously performed covering all relevant operating phases of the design sub-circuits and (ii) that transient current waveforms or equivalent currents are available for each instance terminal and circuit operating phase.

When using only *one* maximum absolute equivalent current value at a net terminal, one *cannot* safely calculate the worst-case current flow in topological connections between layout Steiner points. This somewhat unexpected statement can easily be explained with Fig. 1. Suppose we would perform interconnect wire and via array sizing taking only maximum absolute equivalent current values at each terminal into account (Fig. 1a). We could then eventually obtain a current-density violation in the Steiner point connecting net segment due to cross-current flows when at least one equivalent current value at a net terminal is subject to change (Fig. 1b).

To overcome this problem, we propose to use the lower (AVG_-, RMS_-, $PEAK_-$) and upper (AVG_+, RMS_+, $PEAK_+$) boundaries of the AVG, RMS and PEAK equivalent currents at any time during physical design and verification. These boundaries are derived from the positive and negative shares

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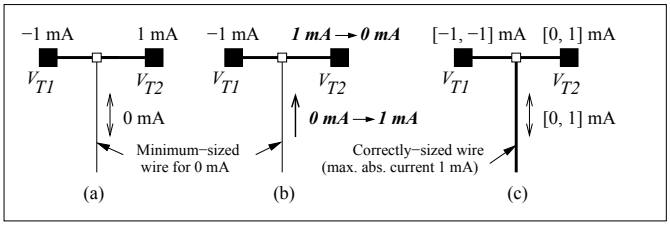

Fig. 1: Topology of a net section with AVG currents. A minimum-sized wire is shown in (a) due to a cross-current of 0 mA. Any *change* of the terminal current in V_{T1} or V_{T2} leads to an *increase* of the cross-current that eventually results in a current-density rule violation in the layout of the net segment (b). Replacing single terminal currents with current bounds delivers the correct bounds for each net segment (c).

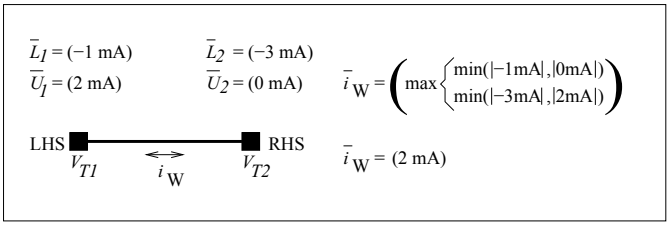

Fig. 2: Determination of the worst-case current vector $\bar{i}_{\mathrm{W}}$ in a net segment according to (2). A net segment between two instance terminals ($V_{T1} - V_{T2}$) and TCM-S (1×1) terminal current matrices with $\overline{L}_l = \overline{L}_1$, $\overline{U}_l = \overline{U}_1$ and $\overline{L}_r = \overline{L}_2$, $\overline{U}_r = \overline{U}_2$ is depicted.

of the current waveform [21], [23], [24]. As an exception, the equivalent value for RMS$_-$, which is calculated from the zero and negative shares of the current waveform, must be multiplied with a factor of -1.0 to guarantee a lower boundary (RMS$_-$ $\leq$0). Using equivalent current bounds (Fig. 1c), we can now calculate the cross-currents correctly in any segment of an arbitrary tree-shaped net layout.

The approach to use equivalent current bounds is in contrary to conventional simulation-based EM and EOS verif cation tools, such as Apache Redhawk-SEM [25], Cadence Virtuoso ElectronStorm [26], Synopsys HSIM$^{\mathrm{plus}}$-SIGRA [27] and others. The mentioned tools require vectors of transient terminal current values to allow the correct calculation of the worst-case current bounds in net segments.

A circuit may have several operating phases accounting for different operational modes and chip temperatures (e.g., normal operation mode, sleep mode, high-temperature operation mode). The current bounds of a net terminal are specif c to an operating phase and must thus be determined by post-processing the obtained current waveforms of each operating phase. The annotated terminal current bounds must also incorporate non-intended currents that may arise to device aging or leakage currents etc. in case they are signif cant.

The TCM-S comprises two equally-sized current matrices $\overline{L}_n$ and $\overline{U}_n$ holding the equivalent currents of an instance terminal n at each circuit operating phase p. The matrix for lower-bound equivalent currents $\overline{L}_n$ is def ned as:

$$\overline{L}_n = \begin{pmatrix} i_{\mathrm{L}n,11} & i_{\mathrm{L}n,12} & \cdots & i_{\mathrm{L}n,1P} \\ i_{\mathrm{L}n,21} & i_{\mathrm{L}n,22} & \cdots & i_{\mathrm{L}n,2P} \\ \vdots & \vdots & \ddots & \vdots \\ i_{\mathrm{L}n,O1} & i_{\mathrm{L}n,O2} & \cdots & i_{\mathrm{L}n,OP} \end{pmatrix}. \quad (1)$$

Each row in $\overline{L}_n$ hereby represents a P-sized sub-vector containing the equivalent currents of a specif c current type o and P operating phases. Each O-sized column sub-vector in $\overline{L}_n$ corresponds to O current types def ned for a specif c operating phase p. The current matrices of all N instance terminals must have the same dimension. A matrix for upper-bound currents $\overline{U}_n$ is similarly def ned for each instance terminal n. A set I_n of terminal current matrices with $I_n = \{\overline{L}_n, \overline{U}_n\}$ is then assigned to each instance terminal of the considered net.

The number of current values that have to be stored and handled in $\overline{L}_n$ and $\overline{U}_n$ for a net with N instance terminals is $(2 \cdot N \cdot O \cdot P)$ regardless of its number of layout Steiner points and regardless of its layout topology. For example, considering a net with a pure DC current f ow ($O = 3$, $P = 1$), this would result in only $2 \cdot N \cdot 3 \cdot 1 = 6N$ current values to account for AVG, RMS and PEAK equivalent currents. For real-world applications, sparse storage techniques applied to $\overline{L}_n$ and $\overline{U}_n$ further reduce the computational requirements.

By using the def nition of $\overline{L}_n$ and $\overline{U}_n$ in (1), we can now calculate the worst-case current vector $\bar{i}_{\mathrm{W}}$ for each net segment (Fig. 2). Hereby, each net segment is f rst partitioned into two sets of left-hand-side (LHS) and right-hand-side (RHS) terminals which contain the corresponding LHS and RHS connection terminals V_l and V_r. (Please refer to (10) and (11) on the calculation of the LHS and RHS sets' current sum.) For each specif c operating phase we may safely imply that terminals will never draw or deliver larger equivalent currents than def ned by their current bounds. The entries of the worst-case current vector $\bar{i}_{\mathrm{W}}$ are thus determined for each current type o and operating phase p as:

$$i_{\mathrm{W},op} = \max \begin{cases} \min\left(|i_{\mathrm{L}l,op}|, |i_{\mathrm{U}r,op}|\right) \\ \\ \min\left(|i_{\mathrm{L}r,op}|, |i_{\mathrm{U}l,op}|\right) \end{cases}. \quad (2)$$

These entries are then used to determine the current-type-specif c worst-case currents that are used for wire and via array sizing of the net segment between V_l and V_r:

$$i_{\mathrm{W},o} = \max\left(i_{\mathrm{W},op}\right) \quad (3)$$

with $o = 1 \ldots O, p = 1 \ldots P$ and instance terminal indices $1 \leq \{l, r\} \leq N$, $l \neq r$. A more complex example of the worst-case current calculation within nets with known topology is depicted in Fig. 3. In this example, the worst-case currents in each net segment are determined by (2) and (3) (Section V, Alg. 2), and they are shown for a set of four terminals connected with three different net topologies.

It can be shown that all annotated equivalent currents of a def ned operating phase and current type can be added up safely. The sum of the annotated equivalent currents of a specif c current type is always equal to or greater than its equivalent value derived directly from the vector sum of transient current values. The formal proof has been omitted here due to space limitations.

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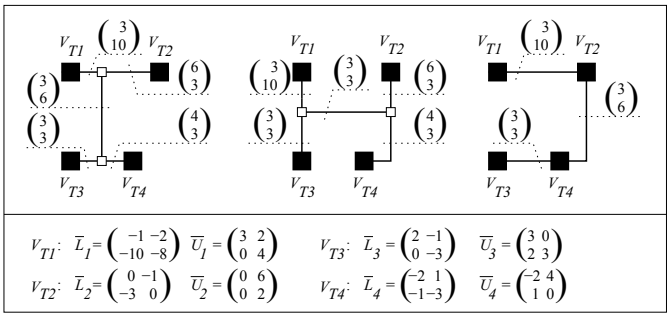

Fig. 3: Three layout topologies of the same net with instance terminals ($V_{T1}, \ldots, V_{T4}$). In each topology, the net segments are labeled with the worst-case current vector $\overline{i}_{\mathrm{W}}$ as calculated using (2) and (3).

IV. The Net Criticality Problem

We now formally introduce the net criticality problem. First, we def ne three types of current-density criticality with respect to a given interconnect temperature and given current-density limits:

1) A net is provably current-density-critical (*critical*) if at least one of its layout structures requires a cross-section adjustment due to current-density limits.
2) A net is not current-density-critical (*non-critical*) if under any circumstances all current-density limits are always ful lled by minimum-sized layout structures.
3) A net is potentially current-density-critical (*potentially critical*) if the non-criticality cannot be suff ciently proven due to the lack of relevant layout information.

Terminal currents are either dependent or independent from the net layout. In analog and power-oriented IC designs, electrical currents are directly related to the function of the involved electrical circuits. The absolute value of the current f ow in these designs primarily depends on the function of the involved electrical circuits rather than on the layout. Hence, their terminal currents are here considered as layout-independent. However, the terminal currents in digital designs are layout-dependent due to interconnect parasitics and cannot be determined unless the net layout is either fully known or the parasitic values were suff ciently estimated [28]–[30].

A. Relevant Design and Technology Parameters

In order to determine the criticality status of a net, one must consider the current f ow at each instance terminal as well as the design constraints for the current f ow within the physical layout of net terminals and within net segments. The current-density limits used for layout dimensioning are technology-specif c and depend on the metallization layer q ($q = 1 \ldots Q$), the temperature T and the current type o ($o = 1 \ldots O$).

An $(O \times Q)$-sized current-limit matrix $\overline{R}$ is def ned for a temperature T that contains the current-type-dependent current limits of a minimum-sized layout structure in each metallization layer. The temperature T typically represents an equivalent temperature that is calculated based on the mission prof le of the IC application and the EM failure mechanism of the interconnect material compound. Each row in $\overline{R}$ contains the maximum permitted equivalent currents r_{oq} for a minimum-sized wire or via array in metallization layer q, an equivalent current type o for a temperature T. Each entry r_{oq} is calculated using the general form of Black's law [1] for EM current-density limits in (4):

$$r_{oq} = j_{\max}\left(T_{\mathrm{ref}}, o, q\right) \cdot c(T) \cdot a_{\min}(q) \tag{4}$$

with

$$c(T) = \exp\left(\frac{E_A(q)}{s\ k\ T} \cdot \left(1 - \frac{T}{T_{\mathrm{ref}}}\right)\right) \tag{5}$$

and for EOS and peak current-density limits [2] in (6):

$$r_{oq} = j_{\max}\left(o, q\right) \cdot a_{\min}(q) \tag{6}$$

with $j_{\max}$ denoting the current-density limit for current type o at a reference temperature T_{ref} and for a specif c layer q, $E_A(q)$ as effective EM activation energy of layer q, k as Boltzmann's constant, s as scaling factor ($s = 1 \ldots 2$ [1], [12]), T as temperature and $a_{\min}(q)$ as minimum cross-section area of metal wires and vias in layer q.

Finally, the maximum permitted current $r_{\max,o}$ of a current type o is def ned as the equivalent current a minimum-sized layout structure in the "weakest" interconnect layer can sustain reliably according to the given current-density limits. Hence, $r_{\max,o}$ is def ned in (7) as the minimum of the matrix sub-vector entries in a specif c row o of $\overline{R}$:

$$r_{\max,o} \ = \ \min\left(r_{oq}\right) \ \text{with} \ (q = 1 \ldots Q) \ . \tag{7}$$

B. Problem Formulation

For the subsequent problem formulation and analysis, we assign each instance terminal and each layout Steiner point terminal (virtual terminal) of the considered net to one of two disjunct terminal sets A and B. We now formally def ne the Net Current Density Criticality Problem (NCP) for nets of arbitrary topology and arbitrary internal current f ow within an operating phase as follows:

For a given f nite set of net-specif c terminal current value matrices $I = \{\overline{I}_1, \overline{I}_2, \ldots, \overline{I}_N\}$, a set of Q layers and a given matrix of current limits $\overline{R}$, a net is current-density-critical at temperature T according to the NCP if at least one of the following two conditions NCP1 or NCP2 holds for all current types ($o = 1 \ldots O$) and operating phase ($p = 1 \ldots P$).

NCP1: The net contains at least one instance net terminal V_{Tn} with a corresponding current matrix $\overline{I}_n$ and minimum layout features in the pin-specif c metal layer set such that

$$r_{\max,o} \ < \ |i_{n,op}| \ . \tag{8}$$

NCP2: At least one net segment between the two disjunct terminal sets A and B exists that ful lls

$$r_{\max,o} \ < \ i_{\mathrm{W},o} \ . \tag{9}$$

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The currents for the LHS and RHS terminal sets required for (3) and (9) are calculated for all instance terminals as follows:

$$i_{\mathrm{L_{LHS}}} = \sum_{n=1}^{N_A} i_{\mathrm{L}n,op} \quad , \quad i_{\mathrm{U_{LHS}}} = \sum_{n=1}^{N_A} i_{\mathrm{U}n,op} \tag{10}$$

$$i_{\mathrm{L_{RHS}}} = \sum_{n=1}^{N_B} i_{\mathrm{L}n,op} \quad , \quad i_{\mathrm{U_{RHS}}} = \sum_{n=1}^{N_B} i_{\mathrm{U}n,op} \tag{11}$$

with $\overline{L}_n$ and $\overline{U}_n$ as corresponding lower- and upper-bound current matrices of instance terminals in terminal sets A as well as N_A and N_B as the number of terminals in A and B.

To be more verbatim, in sub-problem NCP1 we search for at least one instance net terminal whose minimum-sized pin layout cannot reliably sustain its given equivalent terminal currents by itself. In sub-problem NCP2 we search for at least one net segment between instance and/or virtual net terminals whose minimum-sized layout structures would not reliably sustain the given equivalent currents.

Algorithm 1 – Determination of the net criticality status of a net according to NCP1.

Input: – Set of instance terminals V_T
– Set I of TCM-S based terminal current value matrices of all N instance terminals
– Terminal layer set for each terminal in V_T
– The current-limit matrix $\overline{R}$ at temperature T
Output: – Net criticality status: {critical, non-critical}

1: **for** instance terminal $V_{Tn} \in V_T$ $(1 \leq n \leq N)$ **do**
2: **for** current type o $(1 \leq o \leq O)$ **do**
3: $i_{\max,\mathrm{L}} = \max\left(|i_{\mathrm{L}n,op}|\right)$ with $p = 1 \ldots P$
4: $i_{\max,\mathrm{U}} = \max\left(|i_{\mathrm{U}n,op}|\right)$ with $p = 1 \ldots P$
5: $i_{\max} = \max\left(i_{\max,\mathrm{L}}, i_{\max,\mathrm{U}}\right)$
6: **for** layer q $(1 \leq q \leq Q)$ in layout of V_{Tn} **do**
7: **if** $i_{\max} > r_{oq}$ **then return** *critical*
8: **end if**
9: **end for**
10: **end for**
11: **end for**
12: **return** *non-critical* according to NCP1

C. Problem Analysis

Theorem 4.1: The criticality determination in sub-problem NCP1 can be solved in polynomial time.

Proof: The worst-case complexity of the left-hand-side of (8) requires at most Q steps for each current type o and terminal as obvious from (7). Hence, its algorithmic complexity is $\mathcal{O}(Q)$. The worst-case complexity of the right-hand-side of (8) is $\mathcal{O}(2 \cdot N \cdot O \cdot P)$. Since both sides of (8) are polynomial and independent from each other, it is proven that NCP1 can always be solved in polynomial time.
This concludes the proof. ■

Theorem 4.2: For a net with unknown topology, the problem of assigning terminals to the sets A and B in sub-problem NCP2 is $\mathcal{NP}$-complete if there are always at least three net terminals with non-zero currents in an operating phase.

Proof: The assignment of net terminals to either A or B in order to get a net segment with a worst-case current f ow cannot be eff ciently calculated beforehand for nets with more than two terminals. This set assignment problem represents a transformation of the subset version of the KNAPSACK problem, which is known to be $\mathcal{NP}$-complete [31]. Hence, this problem instance of NCP2 also belongs to the class of $\mathcal{NP}$-complete problems.
This concludes the proof. ■

If a net with unknown topology contains terminal current matrices describing current f ows within an operation phase involving two or more terminals, then each matrix set $\overline{I}_n$ can be divided into at least two disjunct sub-matrix sets containing the two-terminal currents and multi-terminal currents. The sub-problem NCP2 can thus be divided into separate and independent problem instances and treated accordingly.

Theorem 4.3: NCP2 can be solved in polynomial time in case the topology of a net is known.

Proof: Each complete net layout consists of m instance and virtual terminals that are connected by at most $(m-1)$ net segments. While traversing all net segments to solve the sub-problem NCP2, it is obvious that the assignment of net terminals to the terminal sets A and B is known. Hence, the terminal assignment problem as discussed in Theorem 4.2 does not exist. The calculation of the LHS and RHS current sums for each net segment requires at most $2 \cdot m \cdot O \cdot P$ steps according to (10) and (11). The current calculation in each of the $(m-1)$ net segments takes at most $O \cdot P$ steps according to (2) and (3). The worst-case algorithmic complexity to solve NCP2 for a net with known topology is $\mathcal{O}(2 \cdot m^2 \cdot O^2 \cdot P^2)$.
This concludes the proof. ■
An interesting observation is the conclusion that the algorithmic complexity of NCP2 only depends on the number net terminals that exchange current within an operating phase and on the knowledge status of the net topology – but not on the net topology itself.

V. Net Criticality Determination

This section introduces three polynomial-time algorithms to address the net criticality sub-problems NCP1 and NCP2 as discussed in Section IV-B. These algorithms allow an eff cient and safe separation into critical and non-critical nets.

Algorithm 1 solves the net criticality sub-problem NCP1 for all current types, and it solves NCP2 for the special case that the current f ow within an operating phase occurs only between two instance net terminals. Algorithms 2 and 3 address the sub-problem NCP2 for current f ows involving more than two terminals within an operating phase. All algorithms utilize the TCM-S based def nition of terminal current value matrices.

As stated for Theorem 4.1, sub-problem NCP1 can always be solved in polynomial time. In order to detect a critical net, Alg. 1 searches for at least one terminal with minimum-sized pin layout features that cannot reliably sustain its currents according to the given limits in $\overline{R}$. Hereby, the maximum absolute value $i_{\max}$ is determined from lower- and upper-bound equivalent currents of each instance terminal V_{Tn} and for each current type o (Alg. 1, lines 3–5). According to (8), $i_{\max}$ is then compared with the maximum permitted current r_{oq} of o in a minimum-sized layout feature. A net is proven to be *critical* if for *any* current type $o : i_{\max} > r_{oq}$ (Alg. 1, line 7).

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Algorithm 2 – Determination of the net criticality status according to NCP2 (known net topology only)

Input: – Net topology graph $G = (V, E)$ with all instance and virtual net terminals as graph vertices V and all connections between terminals as graph edges E
– Set of instance terminals V_T
– Set I of TCM-S based terminal current value matrices of all N instance terminals
– Set of all metallization layers
– The current-limit matrix $\overline{R}$ at temperature T
Output: – Net criticality status: {critical, non-critical}

1: **for** connection edge $E_f \in E$ **do**
2: Split E_f to obtain LHS and RHS terminal sets A, B
3: **for** current type o $(1 \leq o \leq O)$ **do**
4: **for** current vector entry p $(1 \leq p \leq P)$ **do**
5: $i_{\mathrm{L_{LHS}}} = \left|\sum_{n=1}^{N_A} i_{\mathrm{L}n,op}\right|$ [a]
6: $i_{\mathrm{U_{LHS}}} = \left|\sum_{n=1}^{N_A} i_{\mathrm{U}n,op}\right|$ [a]
7: $i_{\mathrm{L_{RHS}}} = \left|\sum_{n=1}^{N_B} i_{\mathrm{L}n,op}\right|$ [b]
8: $i_{\mathrm{U_{RHS}}} = \left|\sum_{n=1}^{N_B} i_{\mathrm{U}n,op}\right|$ [b]
9: $i_1 = \min\left(i_{\mathrm{L_{LHS}}}, i_{\mathrm{U_{RHS}}}\right)$
10: $i_2 = \min\left(i_{\mathrm{U_{LHS}}}, i_{\mathrm{L_{RHS}}}\right)$
11: $i_{\max} = \max\left(i_1, i_2\right)$
12: **if** $i_{\max} > r_{oq}$ **then return** *critical*
13: **end if**
14: **end for**
15: **end for**
16: **end for**
17: **return** *non-critical* according to NCP2

[a] N_A – number of instance terminals in terminal set A
[b] N_B – number of instance terminals in terminal set B

Algorithm 2 addresses the sub-problem NCP2 for nets with current flows involving more than two terminals within an operating phase and known layout topology. The algorithm finds a solution for NCP2 directly and in polynomial time as discussed in Theorem 4.3. The left-hand-side and right-hand-side terminal sets A and B are here to be determined for each topology graph edge E_f (Alg. 2, line 2). The terminal-set-specific current sums of sets A and B are then calculated for each specific current type o and operating phase p in $\overline{L}$ and $\overline{U}$ (Alg. 2, lines 5–8) according to (10) and (11). Using (2), the worst-case lower- and upper-bound currents of the left-hand-side and right-hand-side of E_f are determined (Alg. 2, lines 9–11). According to (9), a net is proven to be *critical* if for *any* current type $o : i_{\max} > r_{oq}$ (Alg. 2, line 12).

In Alg. 3, we determine the highest possible net-internal current bounds for nets with known or unknown topology. Due to the $\mathcal{NP}$-completeness of the NCP2 problem instance in the topology-unknown case (Theorem 4.2), Alg. 3 can only determine with certainty whether a net is either non-critical or potentially critical. It does not prove if a net is (definitely) critical, but it filters out all provenly non-critical nets. Since non-critical nets do not need special consideration during the physical design and do not need current-density verification, Alg. 3 provides a very useful tool for current-driven design.

The core idea of Alg. 3 is firstly to calculate the global lower- and upper-bound matrix sums $\overline{I}_{\mathrm{GL}}$, $\overline{I}_{\mathrm{GU}}$ using all N instance terminals regardless of the net topology (Alg. 3, lines 1–2). Secondly, the absolute maximum of each lower- and upper-bound current is determined (Alg. 3, lines 4–6) and compared with the corresponding maximum permitted current in a minimum-sized layout feature r_{oq} using (9). A net is *potentially critical* if for any current type $o : i_{\max} > r_{oq}$ (Alg. 3, line 8).

Algorithm 3 – Determination of the net criticality status according to NCP2 (known and unknown net topology)

Input: – Set of instance terminals V_T
– Set I of TCM-S based terminal current value matrices of all N instance terminals
– Set of all metallization layers
– The current-limit matrix $\overline{R}$ at temperature T
Output: – Net criticality status: {pot. critical, non-critical}

1: $\overline{I}_{\mathrm{GL}} = \sum_{n=1}^{N} \overline{I}_{\mathrm{L}n}$
2: $\overline{I}_{\mathrm{GU}} = \sum_{n=1}^{N} \overline{I}_{\mathrm{U}n}$
3: **for** current type o $(1 \leq o \leq O)$ **do**
4: $i_1 = \max\left(|i_{\mathrm{GL},op}|\right)$ with $p = 1 \ldots P$
5: $i_2 = \max\left(|i_{\mathrm{GU},op}|\right)$ with $p = 1 \ldots P$
6: $i_{\max} = \max\left(i_1, i_2\right)$
7: **for** layer q $(1 \leq q \leq Q)$ **do**
8: **if** $i_{\max} > r_{oq}$ **then return** *potentially critical*
9: **end if**
10: **end for**
11: **end for**
12: **return** *non-critical* according to NCP2

According to the definition of the NCP in Section IV-B, a net is proven to be *non-critical* at temperature T iff Alg. 1 *and* problem-specific either Alg. 2 or Alg. 3 determine the non-criticality according to sub-problems NCP1 *and* NCP2.

VI. Application Results

The criticality of nets and instances of a commercial smart-power IC design "Industry1" is discussed to show the effectiveness of the design analysis discussed in the previous sections. The example design contains 914 analog, mixed-signal and digital project sub-circuits containing 30725 nets as well as 169 utilized process design kit (PDK) sub-circuits with 1115 internal nets.

First, we show the effectiveness of our approach by determining the critical and non-critical nets in the sub-circuits of "Industry1" using our presented algorithms (Table I). Here we also demonstrate that none of the known critical and non-critical nets are missed by our approach. Second, we verify that only a small percentage of nets that are non-critical are marked as potentially critical due to the reasons mentioned in Section V. Third, we present a design analysis based on the number of found critical and potentially critical nets and their relationship to hierarchy levels, temperature and technology node. As can be seen in Fig. 4, the presented algorithms allow a detailed "what-if" analysis of critical nets with regard to temperature and technology changes, thereby providing a powerful tool to a designer who faces these issues.

The TCM-S based terminal currents for Conditions 1–4 have been obtained from multiple circuit simulation runs using the original netlists (Conditions 1 and 2) or migrated netlists

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TABLE I: Number of critical sub-circuits (SC) and nets in smart-power example IC design "Industry1".

	Example – Industry1					
	Condition 1 [a] *Crit./Pot.Crit./Non-Crit.*		*Condition 2* [b] *Crit./Pot.Crit./Non-Crit.*		*Condition 3* [c] *Crit./Pot.Crit./Non-Crit.*	*Condition 4* [d] *Crit./Pot.Crit./Non-Crit.*
	Approach in [4]	TCM-S Approach	Approach in [4]	TCM-S Approach	TCM-S Approach	TCM-S Approach
Project SCs	609 / n.a. / 305	609 / n.a. / 305	631 / n.a. / 283	631 / n.a. / 283	553 / n.a. / 361	653 / n.a. / 261
Nets	7157/n.a./23568	7157/11387/23568	10176/n.a./20549	10176/14113/20549	4904/6258/25821	13326/16345/17399
Used PDK SCs	66 / n.a. / 103	66 / n.a. / 103	85 / n.a. / 84	85 / n.a. / 84	60 / n.a. / 109	88 / n.a. / 81
Nets in PDK SCs	151 / n.a. / 964	151 / 237 / 964	719 / n.a. / 396	719 / 947 / 396	138 / 272 / 977	726 / 897 / 389

[a] *Condition 1* — the IC design is realized in a reference technology node, nominal temperature, Metal1 is the most EM- and EOS-critical layer
[b] *Condition 2* — the IC design is realized in a reference technology node, nominal temperature + *25 Kelvin*, Metal1 is the most EM- and EOS-critical layer
[c] *Condition 3* — the IC design is realized in a *previous* technology node, nominal temperature, Metal1 is the most EM- and EOS-critical layer
[d] *Condition 4* — the IC design is realized in an *upcoming* technology node, nominal temperature, Metal1 is the most EM- and EOS-critical layer

(Conditions 3 and 4) whose results were subsequently post-processed in order to obtain the equivalent terminal currents (Table I). The TCM-S based terminal current data is here considered as a part of the netlist information. The complete netlist and layout information was known for Conditions 1 and 2. The critical and non-critical nets of all sub-circuits were here determined using a conventional current-density analysis approach [4]. The criticality analysis for Conditions 3 and 4 was entirely based on the given migrated hierarchical netlists and the technology node information.

Our TCM-S based approach used algorithms 1–3 in order to determine the criticality status of all nets in "Industry1". All critical nets found with the approach in [4] were also found with Alg. 3. The number of potentially critical nets is always equal to or greater than the number of actual critical nets. The percentage of nets for Conditions 1 and 2 that were identified as potentially critical but were finally found non-critical (using the approach in [4]) is comparably small (Table I). The runtime of each algorithm was less than 1 minute.

The sub-circuits provided by the PDK of all considered technology nodes must be designed with EM and EOS design rules in mind in order to avoid current-density design rule violations within their derived instances. The consideration of sub-circuits and their internal nets is of specific interest for layout planning since it allows a more exact estimation of the required additional layout and verification effort required for correct interconnect wire and via array sizing.

The percentage and number of critical nets and instances of "Industry1" is depicted in Fig. 4. The percentage of critical nets declines (Fig. 4a) starting with about 45% at the top-level and declining to nearly zero percent at the lowest hierarchy levels. Contrary to the expected drop of the percentage value, we see a peak of the number of critical nets in the lower hierarchy levels 3–6 (Fig. 4b). This observation can be explained with the overall large number of nets found in these hierarchy levels.

Additionally, the percentage of critical instances reduces as well (Fig. 4c) with about 50% critical instances at the top-level down to nearly zero percent at the lowest hierarchy levels. The technology scaling and an elevated on-chip temperature show only minimal impact on the percentage (Fig. 4c) and number (Fig. 4d) of critical instances in the top-level sub-circuits.

VII. Summary

The question whether the layout of a net is likely to encounter current-density stress that is critical to its electromigration and electrical overstress reliability is of significant importance for the physical design and verification of ICs. To answer that question, we firstly introduced a terminal current model (TCM-S) which supports the safe determination of current bounds in all segments of the net layout. Contrary to existing transient vector based approaches, the presented TCM-S enables for the first time a space-efficient yet safe consideration of all relevant equivalent currents at net terminals. The TCM-S can thus be used to support a current-driven IC design methodology that actively avoids electromigration and electrical overstress failures by design. Secondly, we have introduced, analyzed and solved the corresponding "Net Current-Density Criticality Problem (NCP)" that addresses the criticality determination problem for the first time.

The TCM-S and the provided algorithms have been used during the design and verification of many safety-critical automotive ASICs at Robert Bosch GmbH. These algorithms have been applied to identify critical nets during floorplanning, PCell generation, routing, compaction and layout verification. In summary, the application of the presented algorithms has significantly reduced the required design and verification effort without compromising the reliability with respect to electromigration and electrical overstress.

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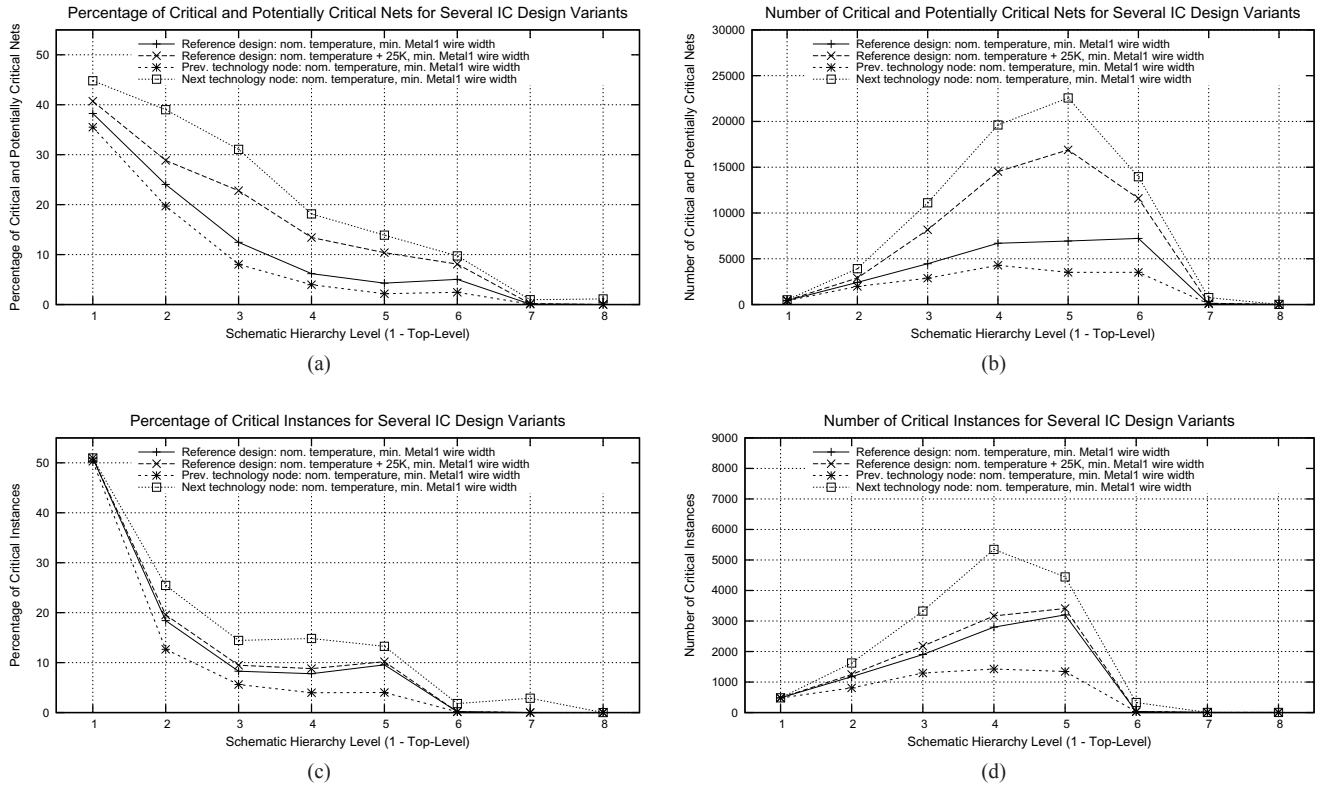

Fig. 4: Depiction of the percentage (4a, 4c) and number (4b, 4d) of critical nets and instances throughout the schematic design hierarchy in IC design example "Industry1". Four design variants and operating conditions 1–4 (Table I) were investigated. Metal1 was depicted because it was the most sensitive layer for electromigration and electrical overstress.

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