

Assembly-Related Chip/Package Co-Design of Heterogeneous Systems Manufactured by Micro-Transfer Printing

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Abstract—Technologies for heterogeneous integration have been promoted as an option to drive innovation in the semiconductor industry. However, adoption by designers is lagging behind and market shares are still low. Alongside the lack of appropriate design tools, high manufacturing costs are one of the main reasons. Micro-transfer printing (μ TP) is a novel and promising micro-assembly technology that enables the heterogeneous integration of dies originating from different wafers. This technology uses an elastomer stamp to transfer dies in parallel from source wafers to their target positions, indicating a high potential for reducing manufacturing time and cost. In order to achieve the latter, the geometrical interdependencies between source, target and stamp and the resulting wafer utilization must be considered during design. We propose an approach to evaluate a given μ TP design with regard to the manufacturing costs. We achieve this by developing a model that integrates characteristics of the assembly process into the cost function of the design. Our approach can be used as a template how to tackle other assembly-related co-design issues – addressing an increasingly severe cost optimization problem of heterogeneous systems design.

Index Terms—assembly-related chip/package co-design, heterogeneous integration on package-level, micro-transfer printing, economical cost function, manufacturing costs, wafer utilization, maximum independent set problem.

I. INTRODUCTION

Heterogeneous integration is considered to be one of the main drivers for innovation in the post-Moore era. However, current production volume and market share are still low due to high manufacturing costs and a lack of appropriate design tools. Design and manufacturing of heterogeneously integrated systems is challenging: different components of such systems are designed and manufactured independently – but eventually have to work as one unit without loss of performance or resources. This urgently asks for appropriate chip/package co-design flows [1]–[3].

As heterogeneous integration is achievable via a growing number of alternative integration and packaging technologies, manufacturing decisions have a strong impact on the economic viability of a package. For example, it is difficult to estimate which packaging technology is the best as it strongly influences the design. This ultimately leads to a manufacturing-related co-design problem in which manufacturing alternatives and parameters have to be considered additionally in the design flow (Fig. 1). To illustrate and to solve this co-design problem, we exemplarily utilize a promising new assembly technology called micro-transfer printing (μ TP) [4]–[7].

μ TP introduces a manufacturing related stamp layout, which is strongly interrelated with the chip and package layouts. However, it is not part of the conventional design flow. The

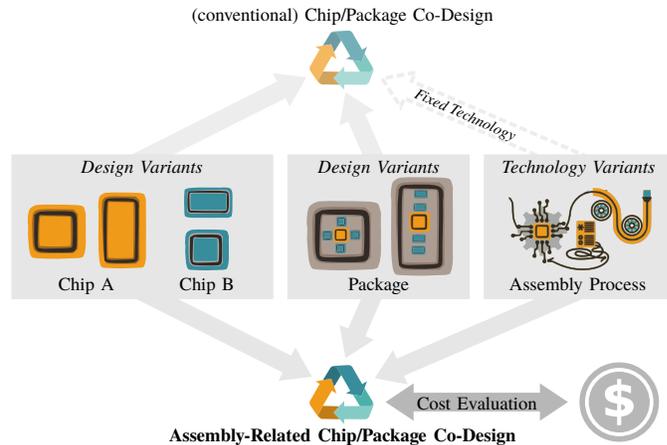


Figure 1. In contrast to conventional chip/package co-design with a fixed target technology (top), advanced packaging technologies introduces more design choices. These require an assembly-related chip/package co-design (bottom) and, ultimately, its economical evaluation (addressed in this paper).

goal is to find the combination of source, target and stamp layouts that has the lowest manufacturing costs and that meets all relevant electrical constraints. In μ TP, the manufacturing costs depend on the utilization of the source and target wafers as well as on the manufacturing throughput. Both, utilization and throughput, depend on the particular layouts of source wafer, target wafer and stamp.

In our paper, we present an algorithm to determine the wafer utilization, which is crucial for addressing the described co-design problem. Our approach allows an optimization of the layouts of source, target and stamp in order to minimize the manufacturing costs of the final package. This will enable designers to fully exploit the micro-transfer printing technology and, more generally, get an understanding of assembly-related co-designs problems and their solutions. Hence, the presented approach is intended as a first step towards models that enable manufacturing-cost based evaluations of design and process parameters and their optimization.

II. TECHNOLOGICAL BACKGROUND AND TERMINOLOGY: MICRO-TRANSFER PRINTING

With regard to manufacturing of heterogeneous systems, μ TP is a promising assembly technology as it combines the advantages of pick and place in terms of flexibility with the advantages of wafer-level processing in terms of high

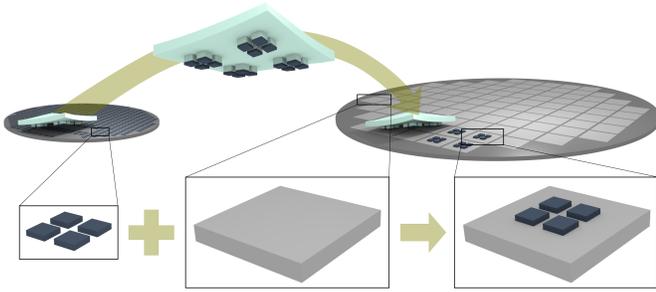


Figure 2. Major steps of the micro-transfer printing (μ TP) process: pickup of coupons from a source wafer (left), transfer via an elastomer stamp (top) and release on the target wafer (right).

throughput. Figure 2 illustrates the μ TP process with its three main constituents.

The *source wafer* (Fig. 2 left) carries different kinds of components (such as passive or active devices), referred to as *coupons*, to be integrated into a package. In order to release the coupons from the source wafer, wet chemical undercut etching is performed prior to the actual transfer process.

The *target wafer* (Fig. 2 right) comprises the *target dies* on which the coupons shall be printed. Thus, the target die serves as carrier and is therefore usually the largest component of the resulting package (e.g., a CMOS circuit). Typically, an adhesion layer is deposited on the target wafer before printing. The target wafer does not require a special treatment with regard to separation as it will undergo conventional wafer cutting.

The μ TP process utilizes a micro-structured elastomer *stamp* (Fig. 2 top), capable to pick and transfer a huge number of elements ($> 10,000$) from the source to the target wafer. The printing process is based on van der Waals forces between the coupons and the stamp. The pickup and release process can be controlled due to a stamping-speed depending adhesion between the coupons and the stamp. During a fast movement of the stamp, its adhesion is larger than the bonding with the wafer, and vice versa. Depending on the size and the layout of the stamp, not all coupons and/or target dies are accessible. The degree of which a wafer can be accessed by the stamp is called *wafer utilization*.

The μ TP process ends with the placement of the coupons, followed by processing steps on wafer-level, such as the creation of electrical interconnects via a redistribution layer (RDL).

The main benefits of μ TP are as follows: substrate-based as well as substrate-less stacking of heterogeneous components on package-level; coupons and target dies as well as the wafers can be of arbitrary sizes; highly parallelized transfer process, with the option of stemming from multiple source wafers; subsequent processing on wafer-level.

On the other hand, as discussed in Section I, the co-design becomes assembly-related, and thus, more challenging. The new layout dependencies between source, target and stamp have to be considered – focusing on their strong impact on manufacturing costs.

III. PRELIMINARIES

This section provides the reader with the background information needed to understand our focus on the determination of the wafer utilization presented in Section IV.

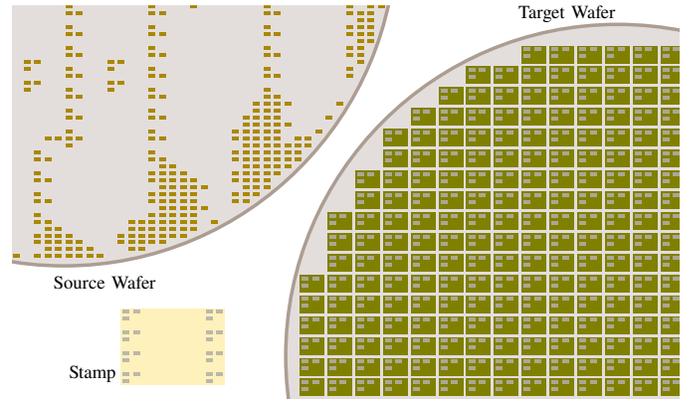


Figure 3. Design example visualizing wafer utilization on the source wafer.

A. Assembly-Related Chip/Package Co-Design

During an assembly-related chip/package co-design, not only the parameters of the chip and package designs (e.g., schematics and layouts) are optimized. Also manufacturing related options, such as the stamp layout in μ TP, need to be considered.

Irrespective of whether the parameters are determined with the aid of an optimization procedure or are specified manually, the evaluation of each solution must be possible in order to make credible design decisions. Usually, such an evaluation is implemented by a cost function combining one or more cost criteria, such as manufacturing costs. The μ TP design example in Fig. 3 is based on a certain set of parameters, such as the layouts of the coupon, the target die, and the stamp. However, in order to evaluate the manufacturing costs, it is essential to know the utilization of the source and target wafers, which is not a direct cost parameter.

B. Cost Model

The following cost model focuses on manufacturing costs and is used to motivate the modeling of assembly-related processes (in our case μ TP). This model is simplified for better comprehensibility and therefore ignores technological details, such as the required changeover times (for stamp or wafer exchange in the printing tool). In the following, n_x stands for “number of x ” and $costs_x$ gives the “costs of x ”.

$$n_{\text{Stampings}} = n_{\text{Quantity}} / n_{\text{DiesPerStamp}}$$

$$costs_{\text{Die}} = (n_{\text{TargetWafers}} \cdot costs_{\text{TargetWafer}}) / n_{\text{Quantity}}$$

$$costs_{\text{Coupon}} = (n_{\text{SourceWafers}} \cdot costs_{\text{SourceWafer}}) / n_{\text{Quantity}}$$

$$costs_{\mu\text{TP}} = costs_{\text{MachineHour}} \cdot t_{\text{StampingDuration}} \cdot n_{\text{Stampings}}$$

$$costs_{\text{PU}} = costs_{\text{Die}} + n_{\text{CouponsPerDie}} \cdot costs_{\text{Coupon}} + costs_{\mu\text{TP}}$$

The final costs are the costs per package unit ($costs_{\text{PU}}$). They are made up of the costs per die, the costs of the coupons placed on a die and the μ TP manufacturing costs. Directly considered are: design parameters ($n_{\text{DiesPerStamp}}$, $n_{\text{CouponsPerDie}}$), economic parameters (n_{Quantity} , $costs_{\text{SourceWafer}}$, $costs_{\text{TargetWafer}}$, $costs_{\text{MachineHour}}$) and technological parameters ($t_{\text{StampingDuration}}$).

However, the derived parameters $n_{\text{SourceWafers}}$ and $n_{\text{TargetWafers}}$ are not easy to compute, as they depend on the expected wafer utilization which itself depends on the wafer and stamp layouts. The cost calculation of a particular system design is hardly

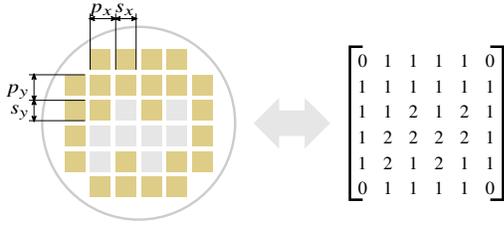


Figure 4. Matrix representation of a given wafer layout discretizing the grid to units of the elements pitch (p_x and p_y). The pitch as well as the element size (s_x and s_y) coincide with the elements on the stamp.

possible without knowing the expected utilization of the wafers during the manufacturing process.

Furthermore, the cost equation depicts the trade-off between the stamp size (and thus, high throughput) and the number of required wafers to reach the production target (i.e., the larger the stamp, the less stampings are required, but the lower the expected utilization will be). A reduced wafer utilization can increase manufacturing costs significantly.

To apply μ TP in an economically efficient manner, the optimization of stamp size and layout is required. As the wafer utilization is difficult to describe analytically, we need an appropriate heuristic as presented in the following sections.

C. Problem Formulation

As motivated above, our goal is to provide a heuristic to determine wafer utilization of a given stamp and wafer combination. Essentially, we need to find an optimal set of stamping positions in such a way that those positions are valid and the number of picked coupons from a wafer is maximized. The corresponding algorithm is described in Section IV and works with the abstractions outlined next.

As the stamp and the (source) wafer have identical grid and element sizes, the wafer utilization can be determined independently of these parameters; only the relative layouts of the elements matter. Thus, the wafer and stamp layouts, which are required as input to the algorithm, can be reduced to discretized matrices as illustrated in Figure 4.

Basically, each element in the layout corresponds to an entry in a matrix $M_{r,c} = (m_{i,j})$, where the rows and columns represent the layout grid. An entry $m_{i,j}$ has the corresponding layout position $(x, y) = ((j-1) \cdot pitch_x, (i-1) \cdot pitch_y)$. We set $m_{i,j} = 1$ if an element exists at that position (e.g., a coupon on the source wafer), $m_{i,j} = 0$ if there is no element at that position, and $m_{i,j} = 2$ if the element is “picked” (relevant for wafers only). The layout coordinates originate at the top left with x increasing in positive horizontal direction and y increasing in negative vertical direction. The utilization can be easily determined by counting the picked elements in $M_{r,c}$.

Throughout the paper, the following assumptions and simplifications are made: the target die pitch is a multiple of the source wafer pitch; each stamp needs to be fully populated; usage of a single stamp only (i.e., no repair steps, no stamp combinations); wafer layouts do not contain any auxiliary structures (e.g., alignment markers, test structures); no consideration of known good die or yield models.

IV. ALGORITHM FOR ESTIMATING THE STAMP UTILIZATION

The optimization of the stampings on a wafer to maximize utilization is NP-hard (see Sec. IV-A4). Hence, we need an appropriate heuristic to estimate the wafer utilization.

A. Algorithm Description

Figure 5 illustrates the stamp utilization process. Input data are the wafer layout (Fig. 5a) and the stamp layout (Fig. 5b). Basically, the provided layout data is reduced to a Maximum Independent Set (MIS) problem and (heuristically) solved by KaMIS, a third party MIS solver [8]. The algorithm outputs the utilization of the wafer (Fig. 5g) and is divided into the following five steps (enumeration as in Fig. 5):

1) *Determination of Valid Stamp Positions*: The first step is to identify all valid stamp positions (Fig. 5c). In our current setup we assume only fully populated stamps as valid¹. Valid positions are derived from a “simulated” application of the stamp on the wafer. Note that the resulting stamp positions may have negative indices with regard to the wafer matrix.

First, we create two sets W and S containing all wafer and stamp elements, respectively. Based on W and S , the valid stamp indices V are obtained.

$$\begin{aligned} W &\leftarrow \{(i, j) \mid m_{i,j} = 1 \wedge m_{i,j} \in M_{\text{Wafer}}\} \\ S &\leftarrow \{(i, j) \mid m_{i,j} = 1 \wedge m_{i,j} \in M_{\text{Stamp}}\} \\ V &\leftarrow \{(i, j) \mid i, j \in \mathbb{Z}, \forall (i_s, j_s) \in S \exists (i + i_s, j + j_s) \in W\} \end{aligned}$$

2) *Identify Stamp Implications*: In order to find out how a stamping on one particular position $v_m \in V$ invalidates other positions, we analyze S and obtain the first order dependencies. A stamp on a position v_m would pick some elements from the wafer. In consequence, a stamp position v_n which also requires one of these already-“picked” elements is related to v_m . We store these directed dependencies within another set D , which contains the affected positional offsets (Fig. 5d). Note the point reflection of the resulting (directed) dependency offsets. Since we will target undirected relations between each stamp position in the next step, this symmetry can be used to reduce the number of offsets by half.

$$\begin{aligned} D &\leftarrow \{(i_o, j_o) \mid i_o, j_o \in \mathbb{Z}^* \exists (i_s, j_s) \in S \exists (i_t, j_t) \in S : \\ &\quad (i_s + i_o, j_s + j_o) = (i_t, j_t)\} \\ D' &\leftarrow \{(r, c) \mid (r, c) \in D \wedge ((r < c) \vee (r = c \wedge r > 0))\} \end{aligned}$$

3) *Building the Stamp Dependency Graph*: Based on D' and V we derive a graph which represents the dependencies between different stamp positions (Fig. 5e). Each node in this graph maps to one valid stamping position. If a stamp dependency between two positions exists, an edge is inserted between the two corresponding nodes.

$$\begin{aligned} G &= (V(G), E(G)), V(G) \leftarrow V \\ E(G) &\leftarrow \{e \mid \Psi_G(e) = (u, v) = (v, u), \\ &\quad u, v \in V(G), \exists d \in D' : u + d = v\} \end{aligned}$$

4) *Solving the Maximum Independent Set Problem*: In order to get the maximum number of stampings on the wafer, we need to identify the maximum number of independently selectable

¹It is also possible to consider partially populated stamps as valid. However, this would require a transition towards a maximum weighted independent set problem which is not within the scope of this paper.

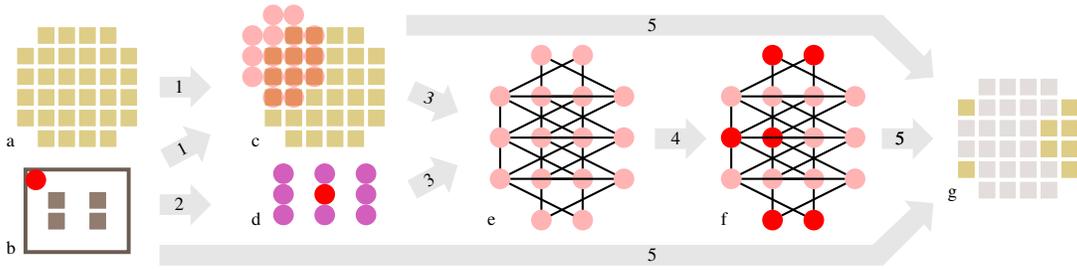


Figure 5. Graphical illustration of our algorithm to determine the wafer utilization (described in Section IV).

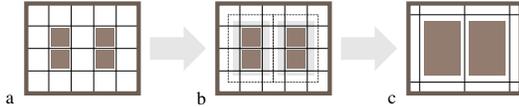


Figure 6. Conversion of the stamp layout from source (a) to target grid (c) by matching it with the target die layout (b).

nodes in G (i.e., all selected nodes must not share a single edge, Fig. 5f). This NP-hard problem, known as a maximum independent set (MIS) problem, is solved by applying KaMIS, a solver for the MIS problem [8]. As result, KaMIS returns the desired maximum independent set.

$$V_{IS} \leftarrow \{v \mid v \in V\} : \nexists u, v \in V_{IS}, e \in E(G), \Psi_G(e) = (u, v)$$

$$V_{MIS} \leftarrow V_{IS} \text{ with the maximum number of elements}$$

5) *Apply Stampings on Wafer:* With V_{MIS} available, it is straightforward to apply the corresponding stampings on the wafer (Fig. 5g). For each element position on the stamp, the respective stamp position offset is applied.

$$W_S \leftarrow \{(i, j) \mid \forall (i_p, j_p) \in V_{MIS} \forall (i_s, j_s) \in S, \\ (i, j) = (i_p + i_s, j_p + j_s)\}$$

B. Adaptation to Target Wafer

The presented algorithm can be applied directly to obtain the source wafer utilization as each element on the stamp directly corresponds to an element on the source wafer. In contrast, the target wafer utilization can not be calculated directly with the presented algorithm; instead, a slight modification is required. Specifically, we need to create a virtual “target wafer stamp” on which the element grid corresponds to the target wafer grid.

Figure 6 illustrates the conversion. A given (source) stamp is partitioned corresponding to the source wafer grid (cf. Fig. 6a). In consequence of the μ TP process, the stamp also shows an implicit second order pattern (i.e., the repeating target die layout). This can be seen in Fig. 6b where two coupons are placed on each target die. These sub-layouts result in a new (target die) grid which yields the required “target wafer stamp” (cf. Fig. 6c).

If this derived stamp is used in combination with the target wafer layout as input, the presented algorithm determines the target wafer utilization.

V. SUMMARY AND OUTLOOK

In this paper we used the new μ TP technology to illustrate the interdependencies between design and manufacturing in

order to introduce assembly-related chip/package co-design. Specifically, we developed a model of the assembly process (wafer utilization) to evaluate design decisions (stamp and wafer layout) with regard to their impact on manufacturing cost.

In contrast, conventional chip/package co-design typically is limited to a single integration technology. Hence, it is not suitable for design problems that consider different assembly variants. Such a comparison requires models of the assembly processes integrated into the design tools. The presented model is a first step towards such an integration. It enables manufacturing-cost-based evaluations of design and process parameters and their optimization.

In the future, we will employ this new approach in a co-design flow in order to find optimized die dimensions, source and target wafer layouts, and stamp designs with regard to manufacturing cost. Furthermore, we plan to extend our tool in order to support stamps of different sizes, which will further reduce cost of heterogeneous systems manufactured using the μ TP technology.

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