Hierarchical Current Density Verification for Electromigration Analysis in Arbitrarily Shaped Metallization Patterns of Analog Circuits

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Overview

- Motivation and previous works
- Design flow
- How do we characterize pin currents?
- How is current density calculated?
- How do we visualize and verify current density?
- Experimental results
- Summary

Motivation

Analog circuits for automotive applications

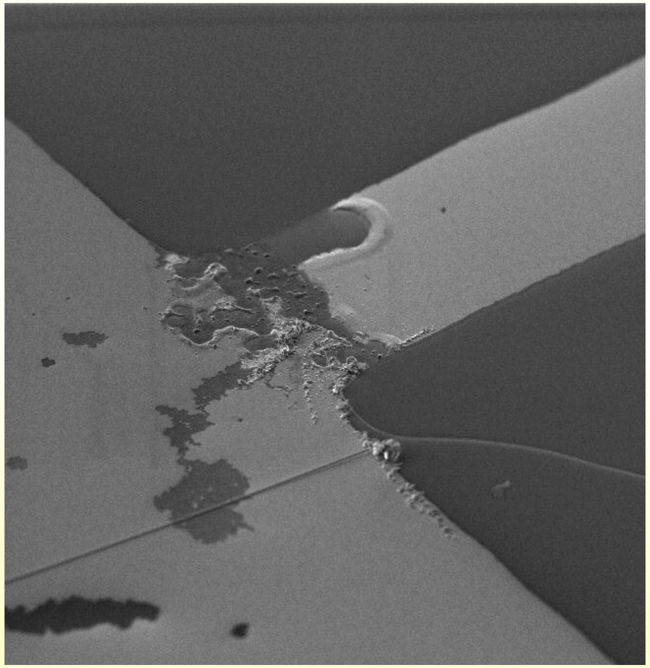
- High interconnect currents
- Ongoing reduction of circuit feature sizes, including interconnects

⇓

- Insufficiently dimensioned cross section area of interconnects

⇓

- High current densities which might lead to electromigration



http://ap.polyu.edu.hk/apavclo/public/gallery.htm

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Motivation (cont.'d)

- No commercial tools available for electromigration analysis of arbitrarily shaped metallization patterns (as commonly used in analog circuits)
- Manual current density verification is very time consuming and error prone

⇒ Need for an automatic verification methodology tailored for electromigration analysis of arbitrarily shaped metallization patterns in analog circuits

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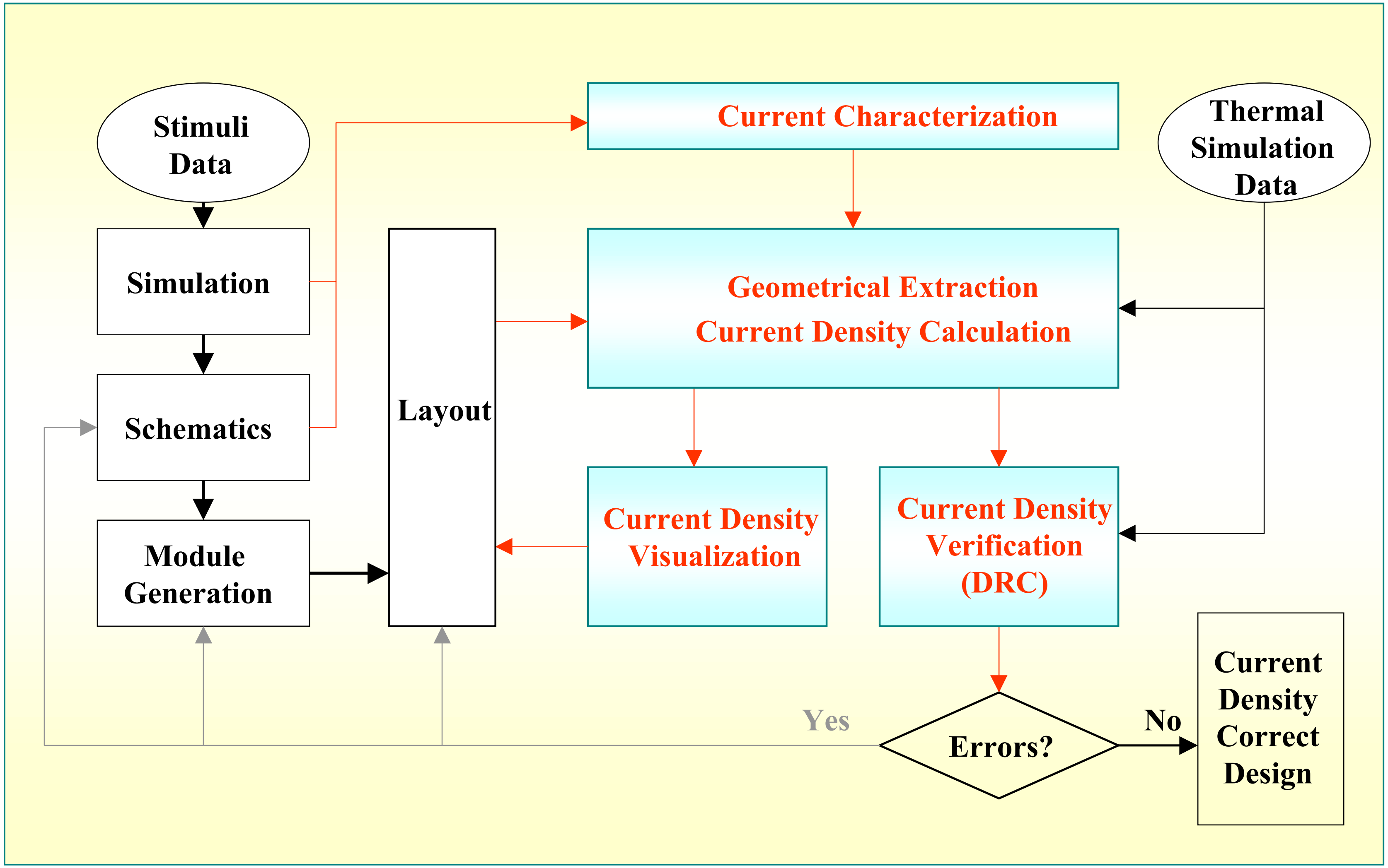
Previous Works

- Studies of electromigration and its relation to the mean time to failure (MTTF) of electronic circuits
  [Black 1969][D'Heurle 1971][Maiz 1991][Young et al. 1994]

- Electromigration analysis in digital systems
  [Hajj et al. 1991][Steele et al. 1998]

- Electromigration analysis in analog circuits limited to rectangular shapes [Adler et al. 2000]

Design Flow



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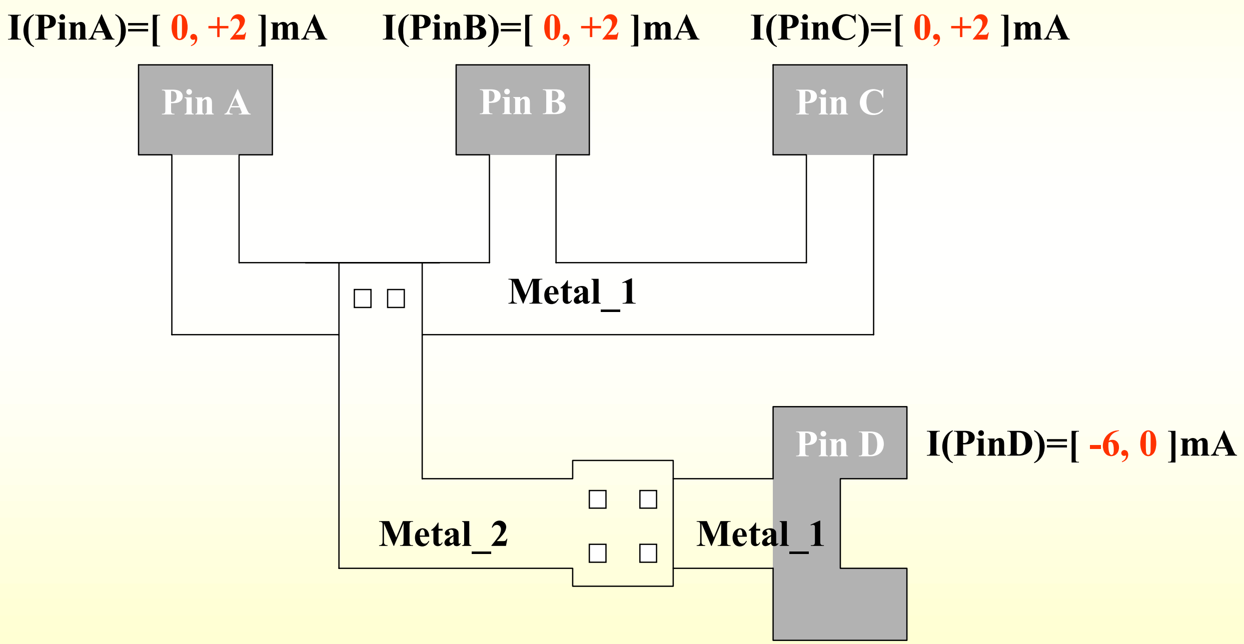
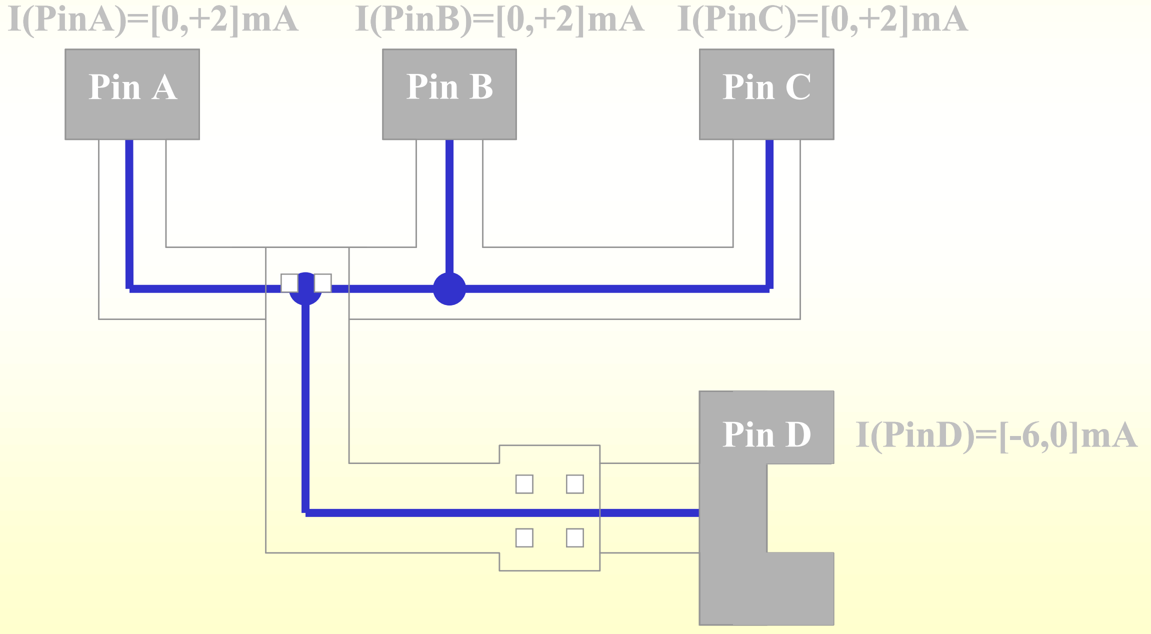
Pin Current Characterization

- Pin current values are attached as $[I_{min}, I_{max}]$



Layout Segmentation

(1) Determination of the current graph



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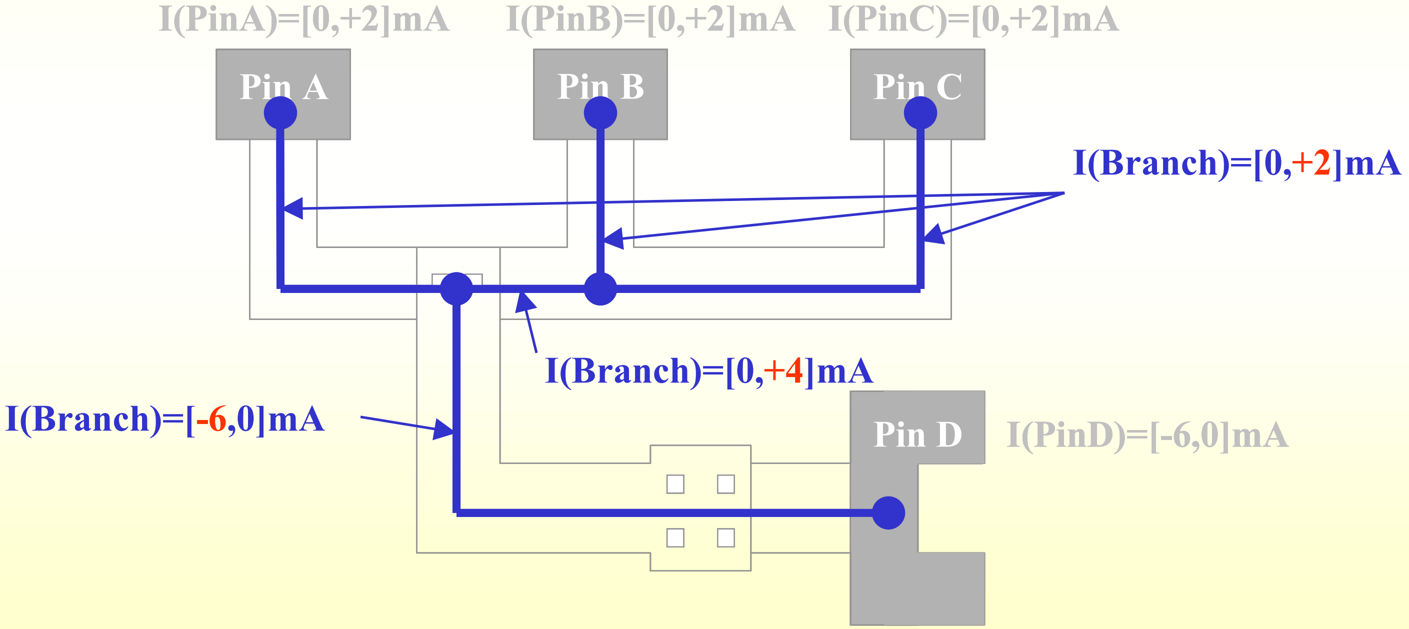
Layout Segmentation

(1) Determination of the current graph

(2) Worst case analysis within the current graph



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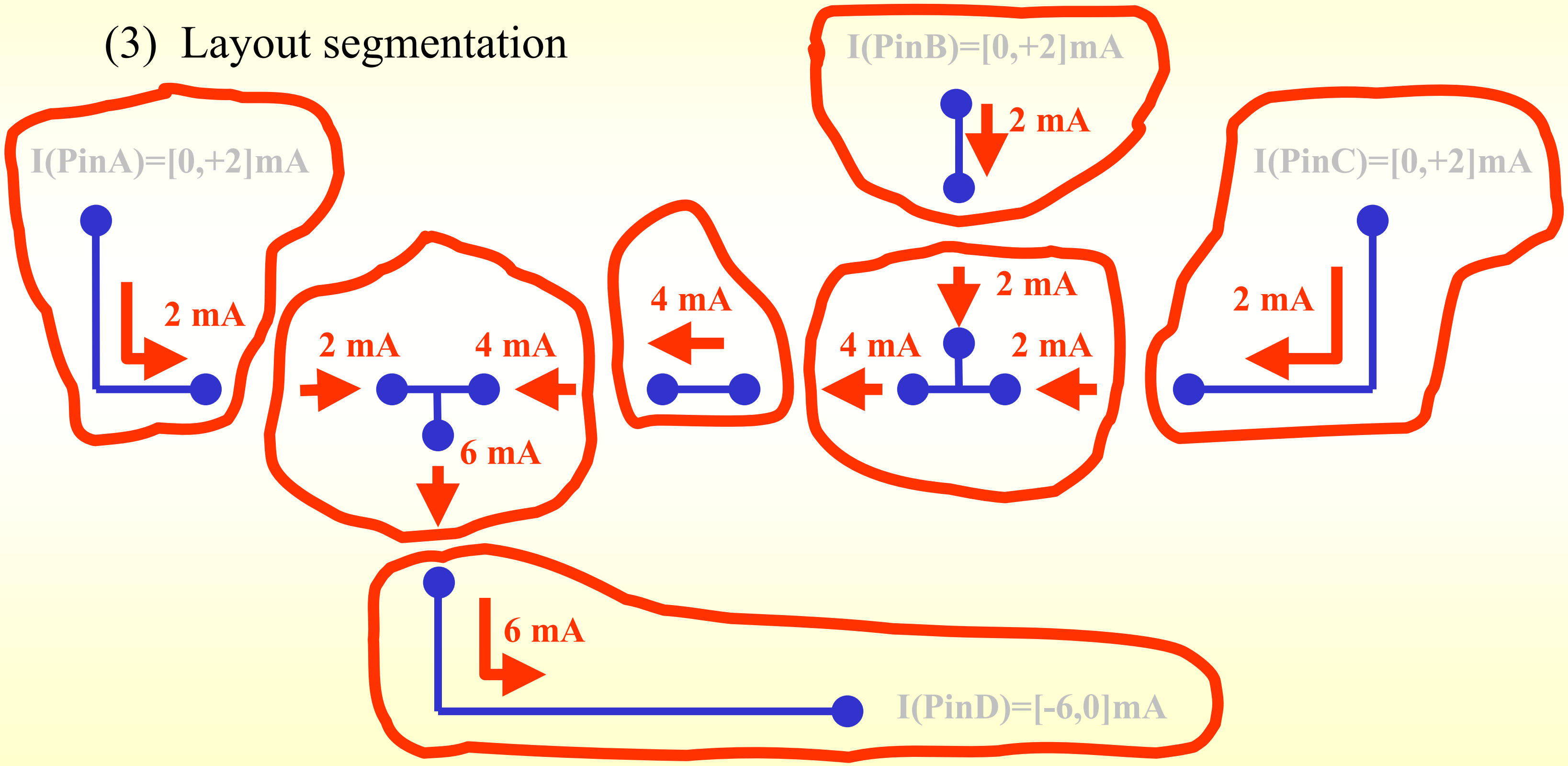
Layout Segmentation

(1) Determination of the current graph

(2) Worst case analysis within the current graph

(3) Layout segmentation



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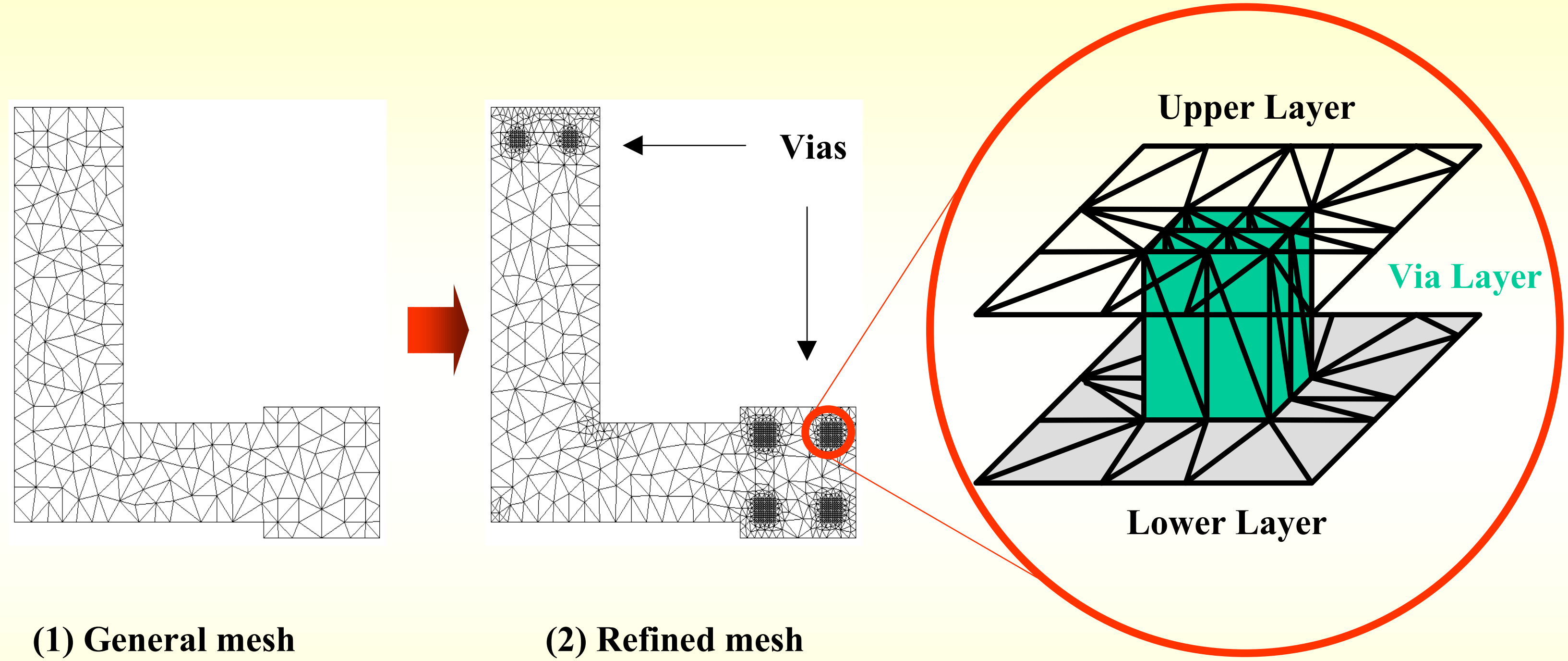
Geometry Extraction for Finite Element Method



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Current Density Calculation

- Given:
  Segments from layout segmentation with geometry and currents

- Goal:
  For each layout segment determine current density by using Maxwell's equation

$$\underline{J} = \frac{1}{\rho}\left(\frac{\partial\varphi}{\partial x}, \frac{\partial\varphi}{\partial y}, \frac{\partial\varphi}{\partial z}\right)^{\mathrm{T}}$$

- Solution:
  In order to obtain the potential field configuration $\varphi(x,y,z)$, the Laplacian equation has to be solved using the Finite Element Method (FEM)
  (→ see Section 4.2 in paper)

$$\Delta\varphi = \frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} + \frac{\partial^2\varphi}{\partial z^2} = 0$$

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Current Density Calculation: Incorporating Thermal Simulation Data

- Problem:
  Calculating current density is temperature dependent because any change in the temperature distribution influences the gradient of the electrical potential field $\varphi(x,y,z)$

Maxwell's equation $$\underline{J} = \frac{1}{\rho}\left(\frac{\partial\varphi}{\partial x}, \frac{\partial\varphi}{\partial y}, \frac{\partial\varphi}{\partial z}\right)^{T}$$

- Solution:
  Electrical conductivity $\rho(x,y,z)$ is determined under consideration of a thermal potential field

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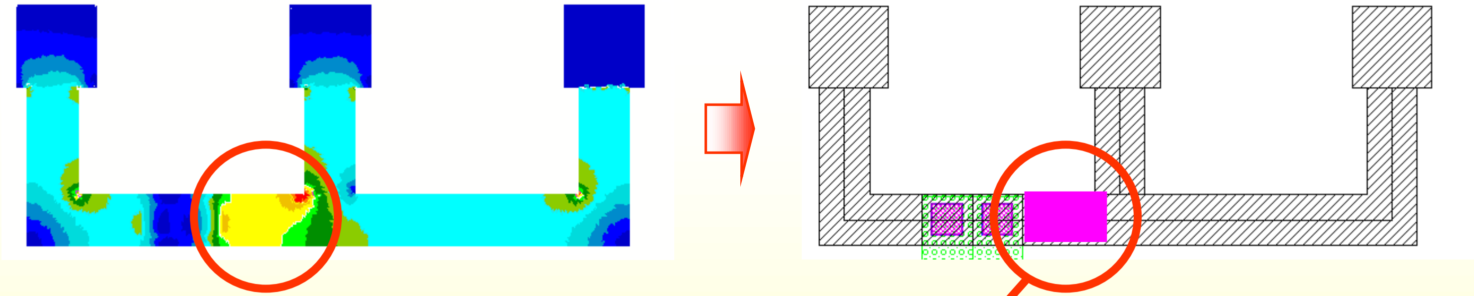
Current Density Verification

- Does calculated current density value exceed the reference value of the maximum current density of the layer material?

⇒ “Current density DRC”



Calculated current density > Permissible maximum current density

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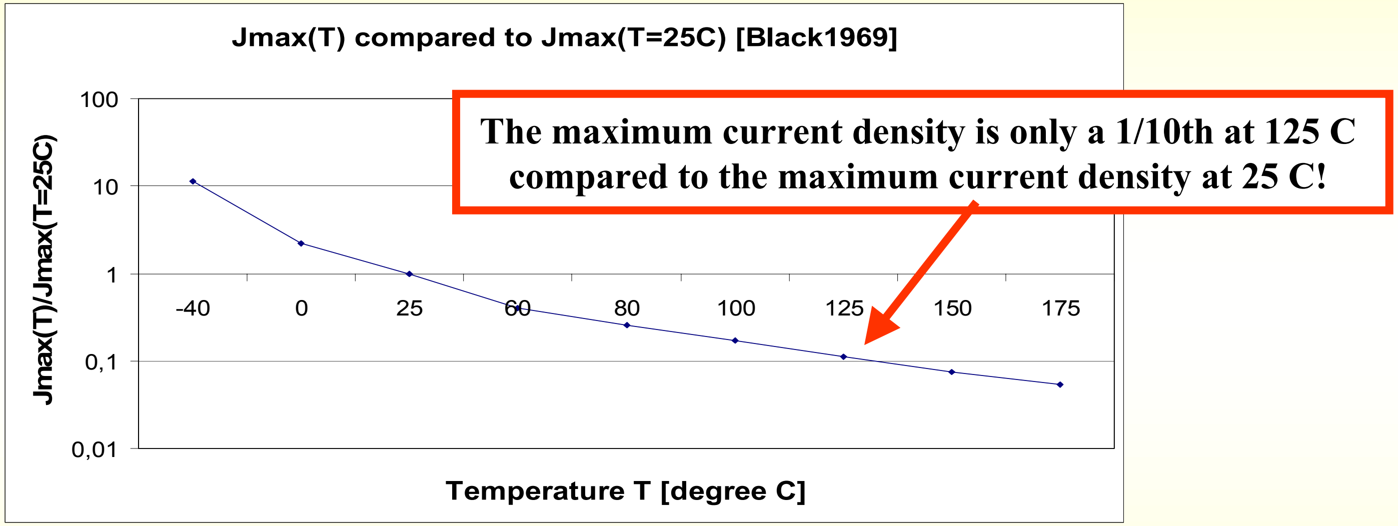
Current Density Verification: Incorporating Thermal Simulation Data

- Problem:
  Verifying current density is temperature dependent because acceptable maximum current varies with temperature



- Solution:
  In order to verify if calculated current density is acceptable, we compare calculated current density with a reference current density scaled by the actual working temperature

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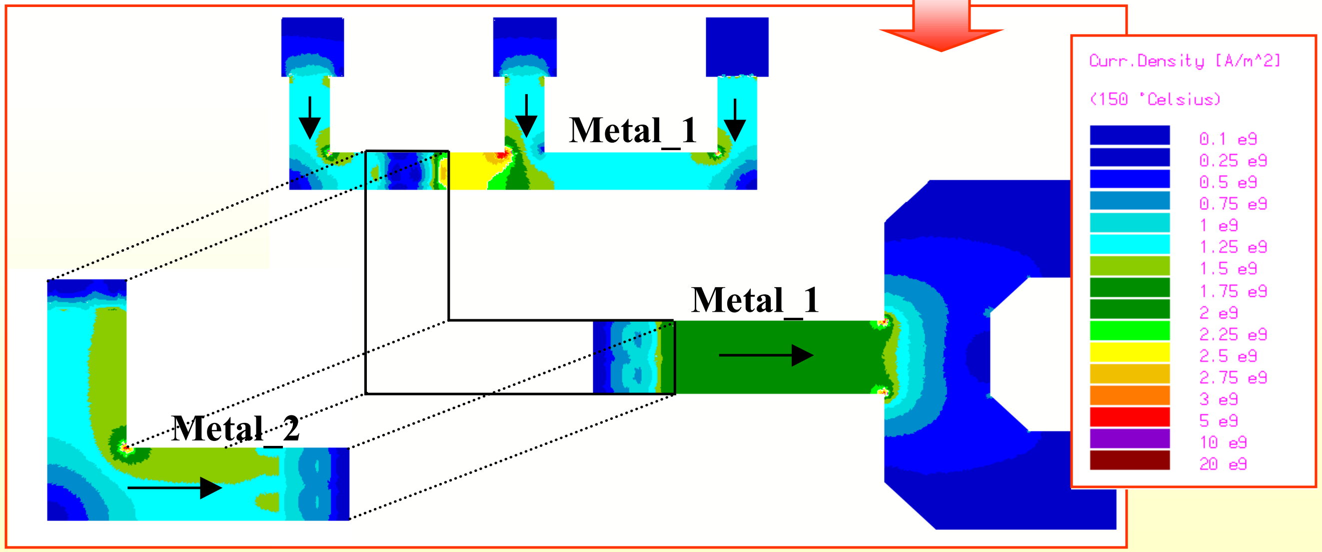
Current Density Visualization

- Time-dependant pin current values
- No layout segmentation

Geometrical Extraction
Current Density Calculation

Current Density Visualization



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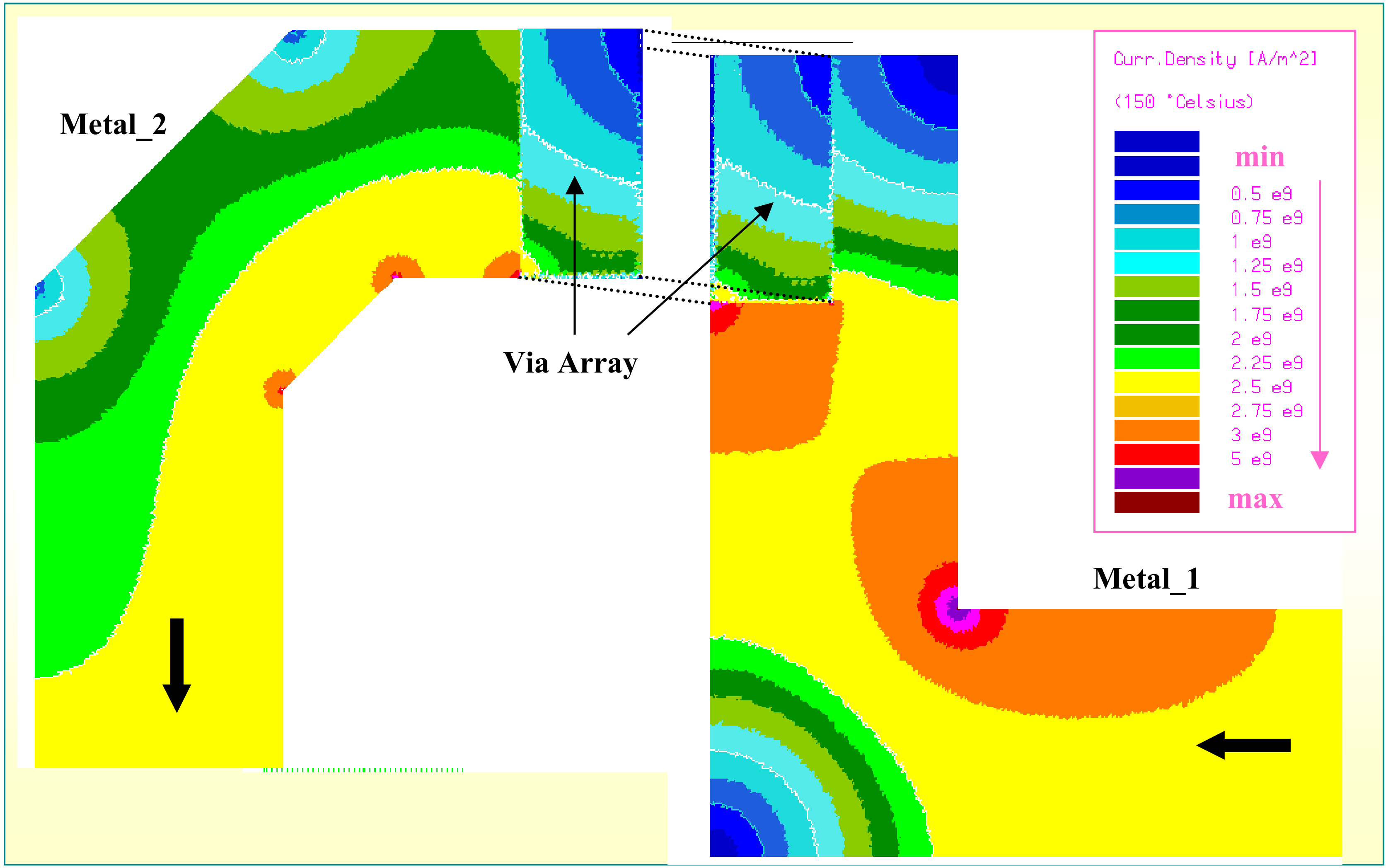
Results: Interconnect and Via Array



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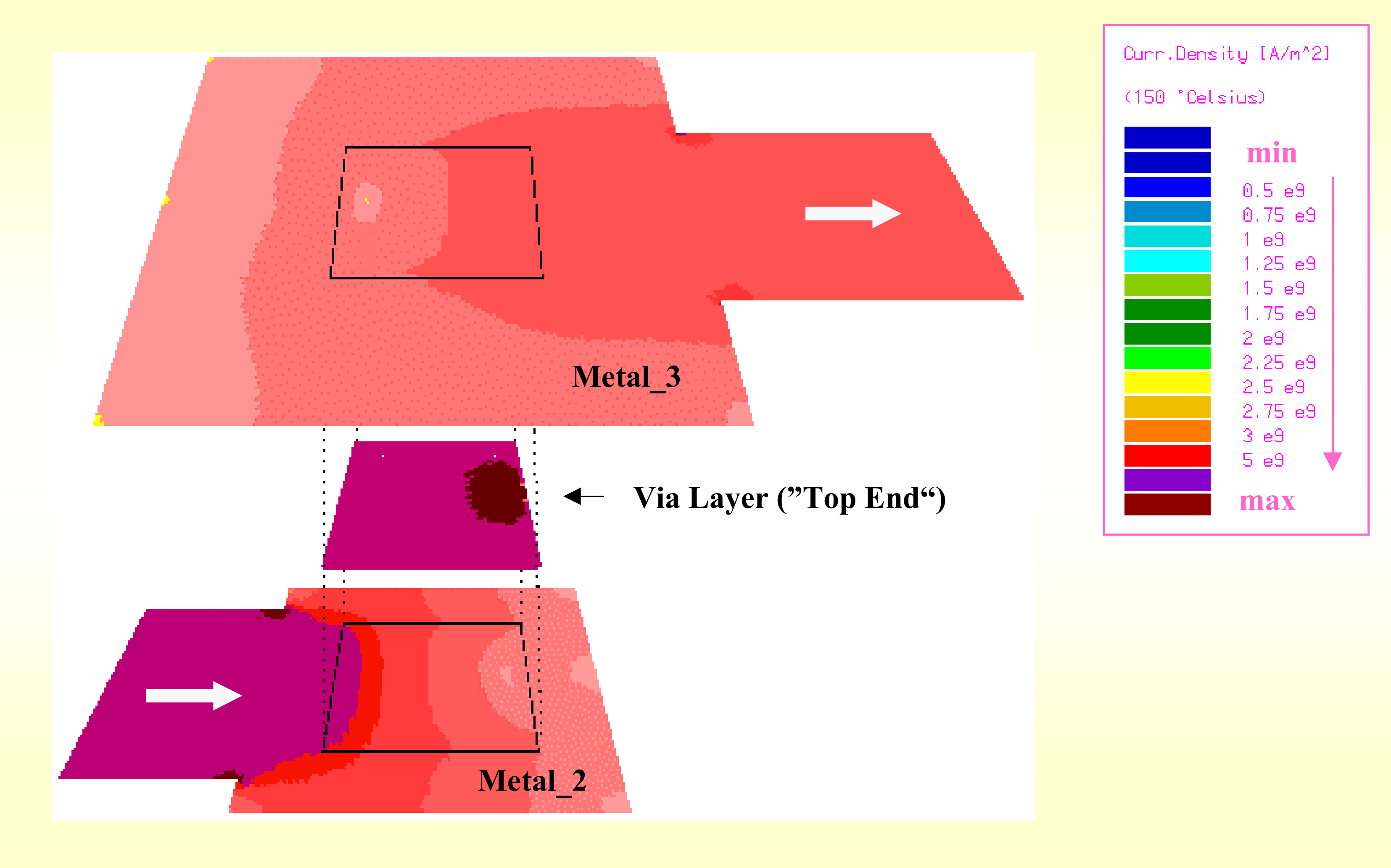
Results: Single Via



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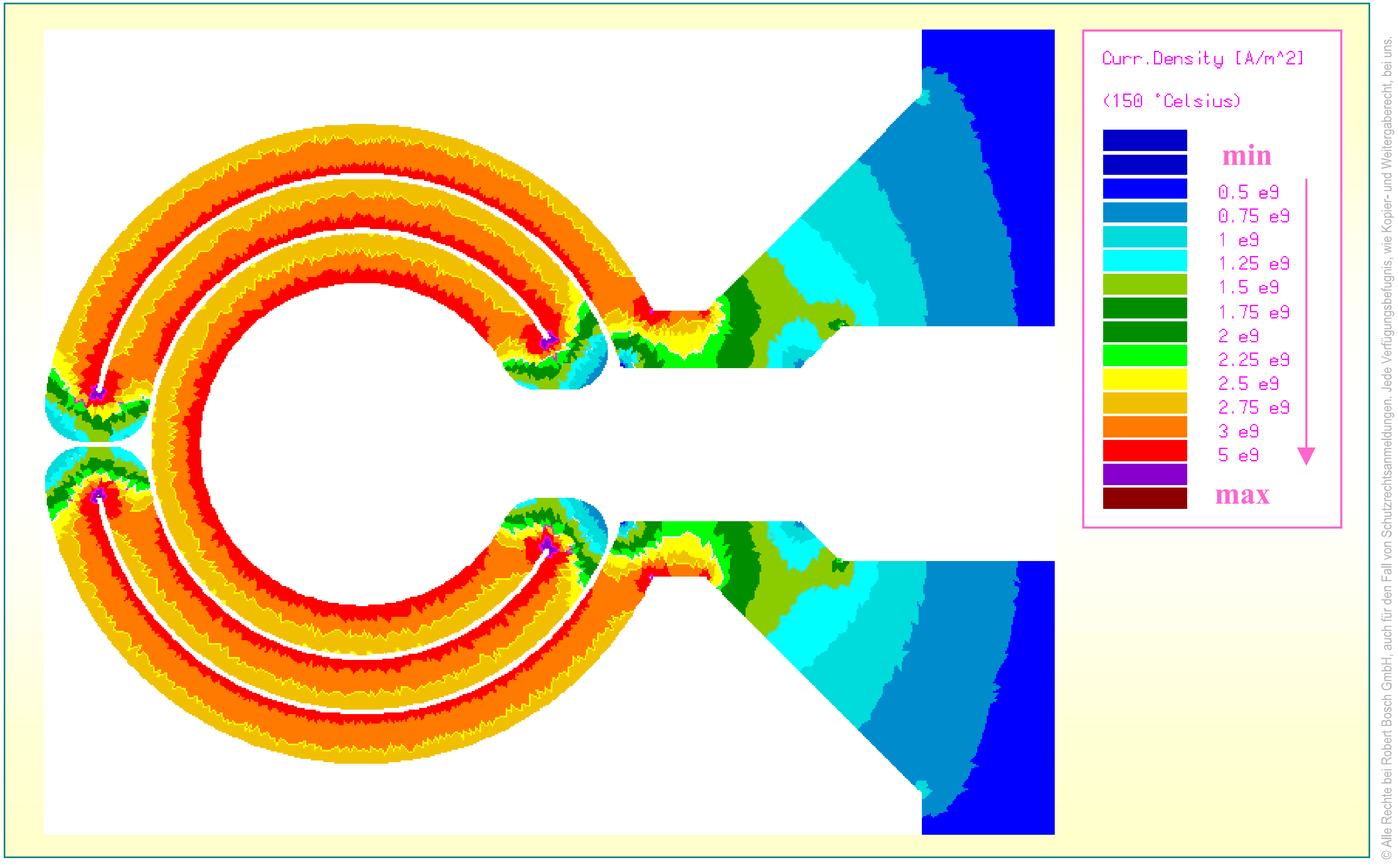
Results: MEMS Structure



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Summary

- New methodology for hierarchical verification of current densities in arbitrarily shaped analog circuit layouts
- Quasi-3D model for verifying irregularities like vias and via edge stress, using “bee-comb”-like structures
- Incorporating thermal simulation data to account for temperature dependency of electrical field configuration and electromigration
- Option of integrating our methodology as an automated current density DRC in virtually any IC-design flow
- Verification of our methodology on “real world” analog circuits

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Appendix: Current Density Calculation (FEM)

(1) Perform triangulation

(2) Use linear assumption for triangles Δ $\varphi = a_0 + a_1 x + a_2 y$

(3) Generate the *Element Equations* $\underline{i}_\Delta = \underline{Y}_\Delta \cdot \underline{\varphi}_\Delta$

(4) Assemble the *System Matrix* with all triangles $\underline{i} = \underline{Y} \cdot \underline{\varphi}$

(5) Apply boundary constraints $\underline{i_{BC}} = \underline{Y} \cdot \underline{E^{BC}} \cdot \underline{\varphi}$

(6) Solve equation system (e.g., with Conjugated Gradient Method)

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