Reliability-Driven Layout Decompaction for Electromigration Failure Avoidance in Complex Mixed-Signal IC Designs

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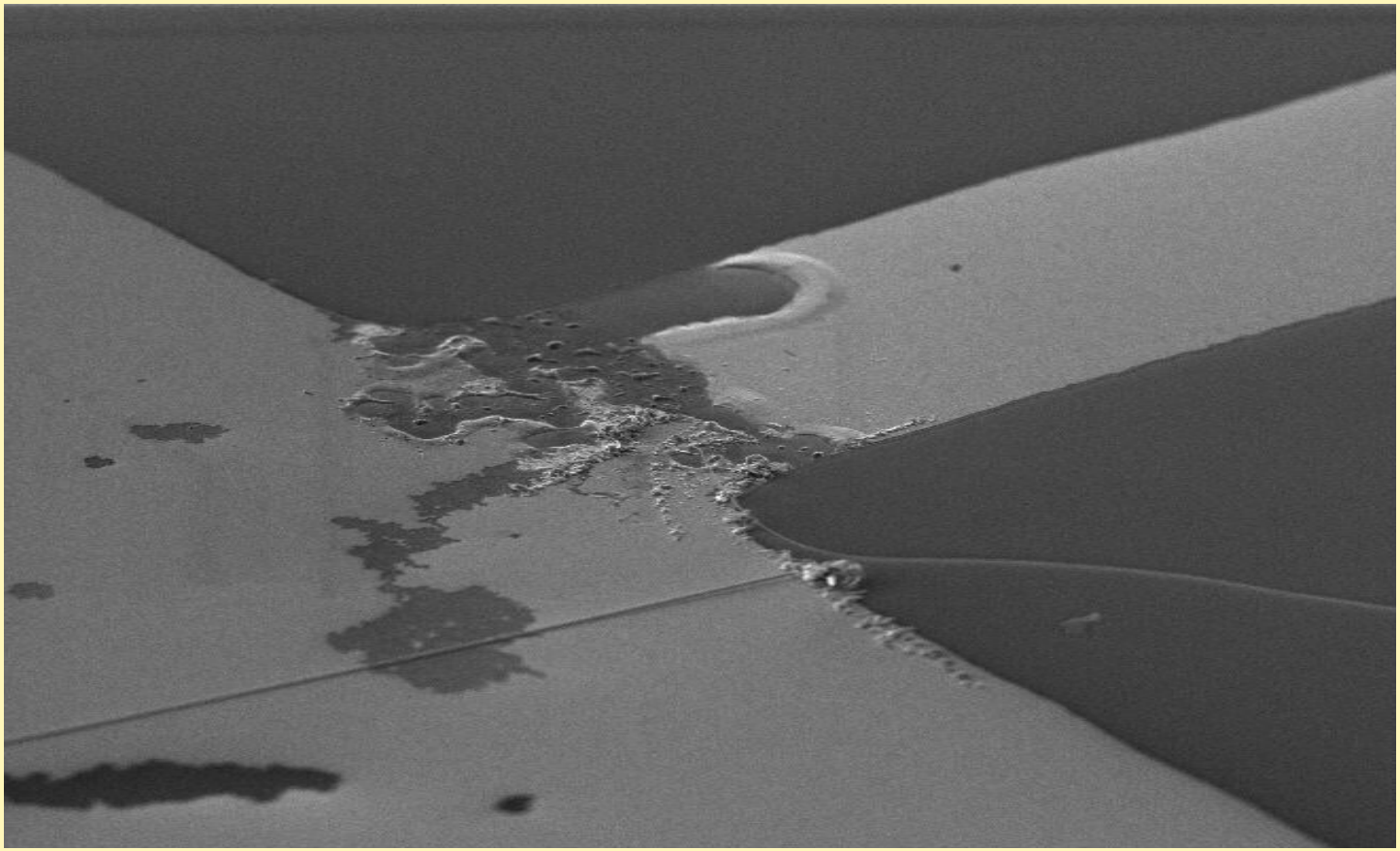
Outline

- Motivation
- Design Flow
- Reliability-Driven Layout Decompaction
- Results
- Conclusion

Motivation

Electromigration is a reliability problem:

- Creation of voids → drift of parameters, open circuits
- Hillocks and whiskers → short circuits

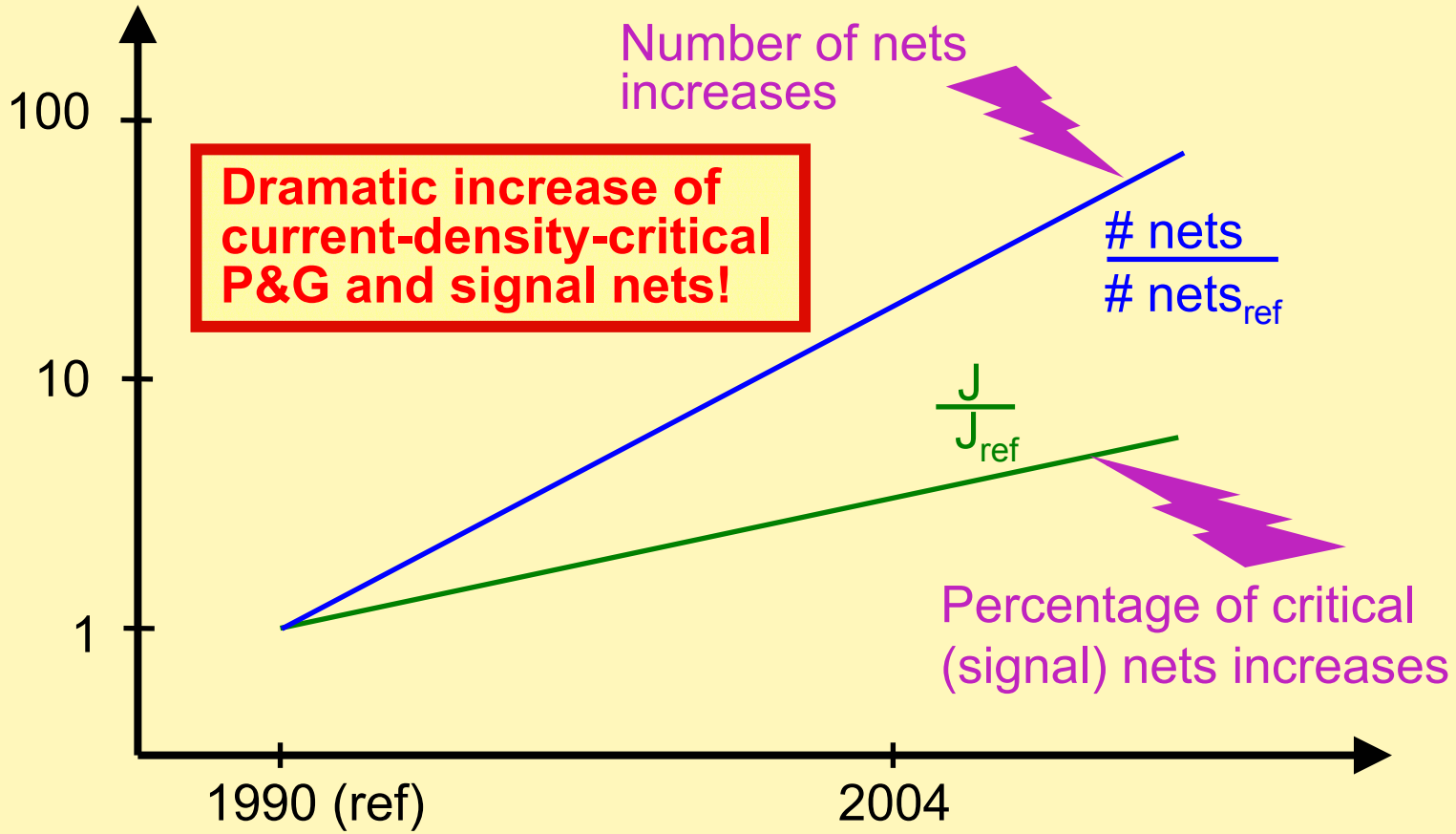


http://ap.polyu.edu.hk/apavclo/public/gallery.htm

Motivation (2)

Electromigration is a design problem:

- Percentage of current-density-critical (signal) nets increases
- Overall number of nets increases



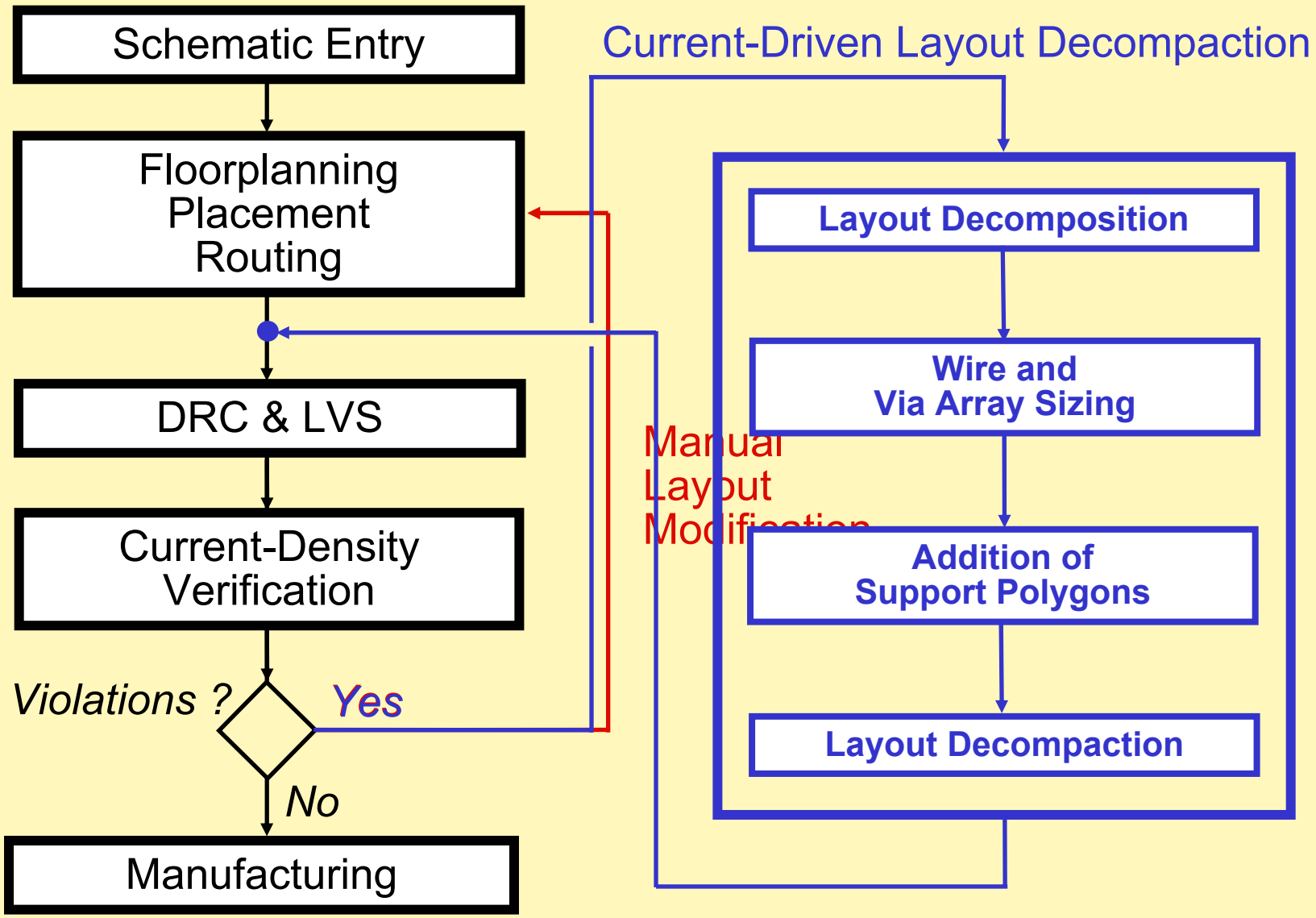
Solutions ?

- "Net classes":
  - Current-density-correct layouts cannot be guaranteed
  - Either route space wasting or insufficient wire and via sizing

- Current-driven routing strategies:
  - Current-density-correct layouts due to "correct-by-construction"
  - Must solve a cyclic design problem: topology $\leftrightarrow$ segment currents

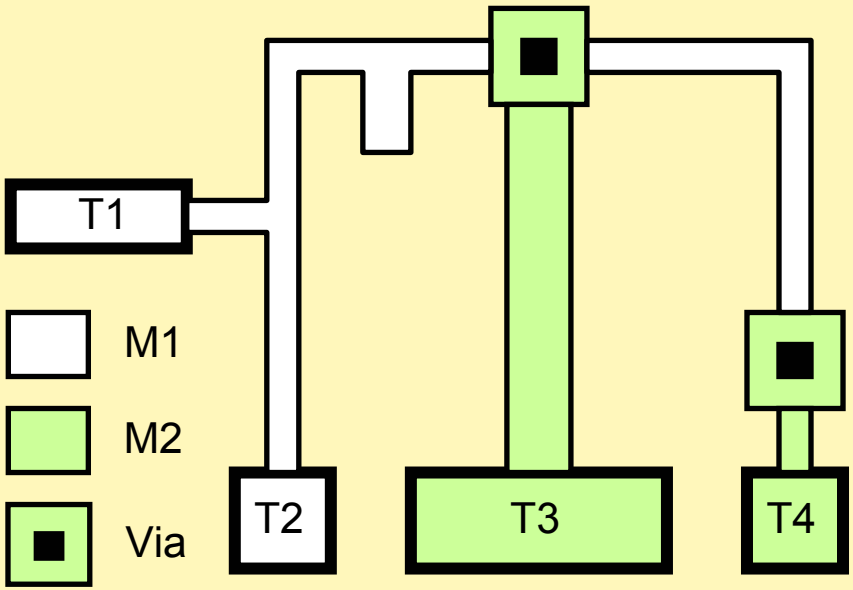
- **Our Solution:**
  - Post-route modification of the existing physical layout
  - Net topology is known $\rightarrow$ segment currents can be derived easily (no cyclic design problem exists)

Design Flow

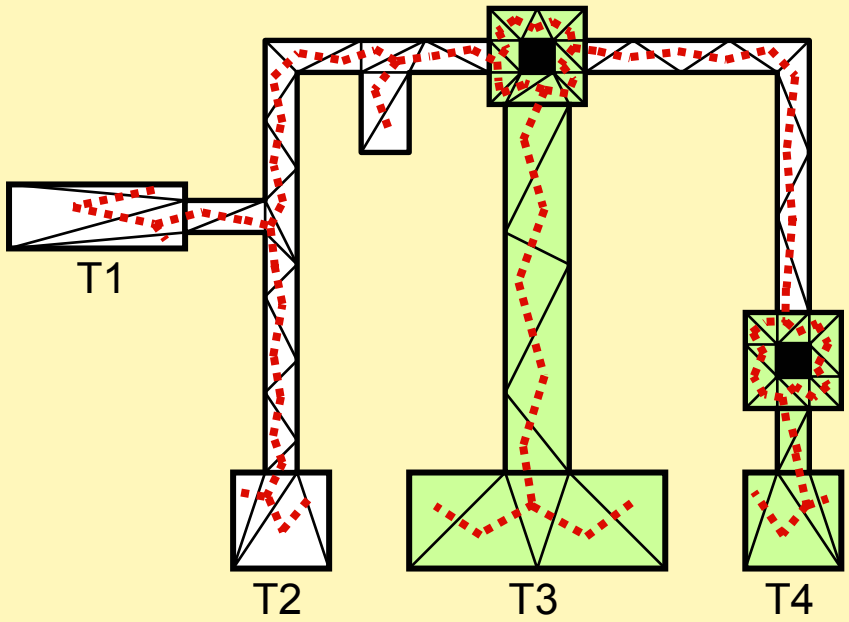

Schematic Entry
Floorplanning
Placement
Routing
DRC & LVS
Current-Density
Verification
Violations ?
Yes
No
Manufacturing
Current-Driven Layout Decompaction
Layout Decomposition
Wire and
Via Array Sizing
Addition of
Support Polygons
Layout Decompaction
Manual
Layout
Modification

Layout Decomposition

- Given: Net layout with terminal currents
- Objective: Determination of all independent net segments



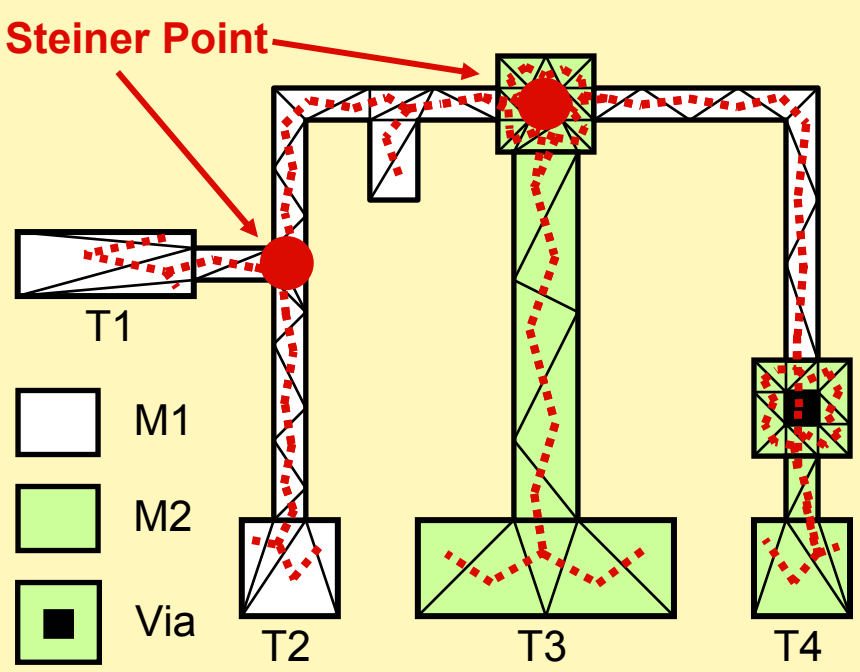
1) Original net layout

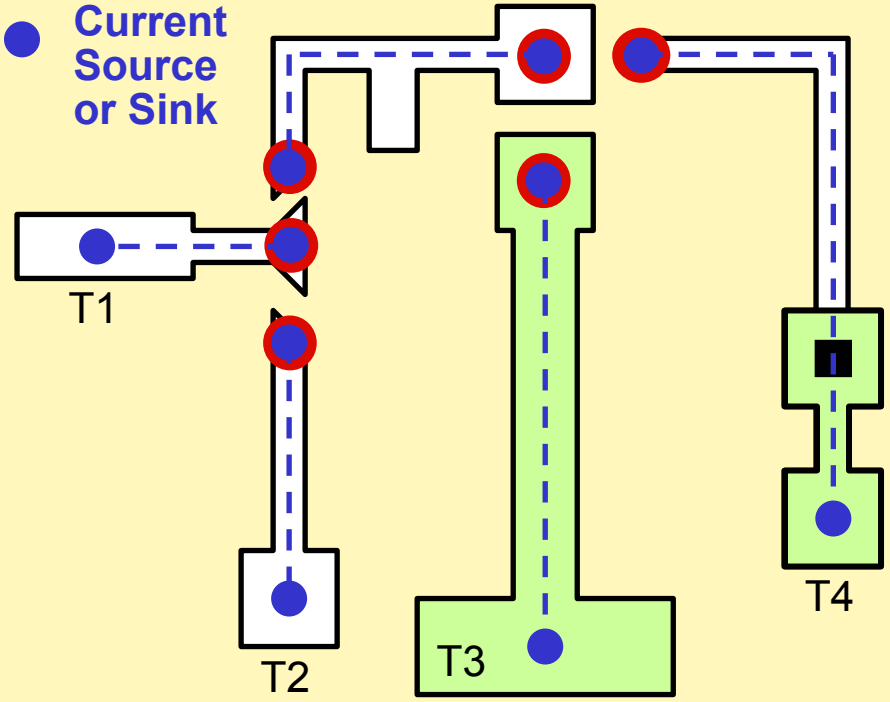


2) Sub-element creation (Triangulation and Mid-point connections)

Layout Decomposition (2)

- Given: Net layout with terminal currents
- Objective: Determination of all independent net segments





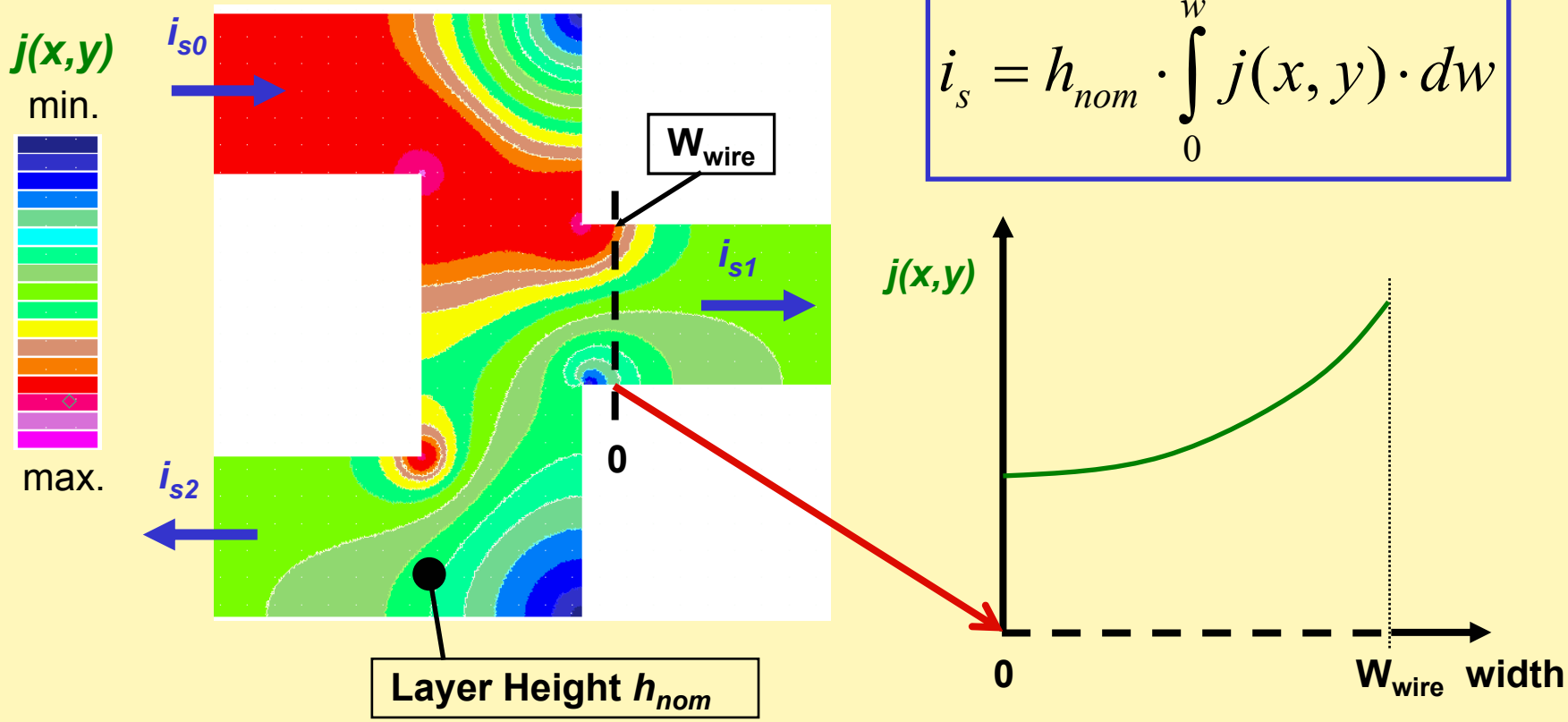
3) Tree pruning, retrieval of SP and net segment objects

4) Independent net segments with current sources and sinks

Wire and Via Array Sizing

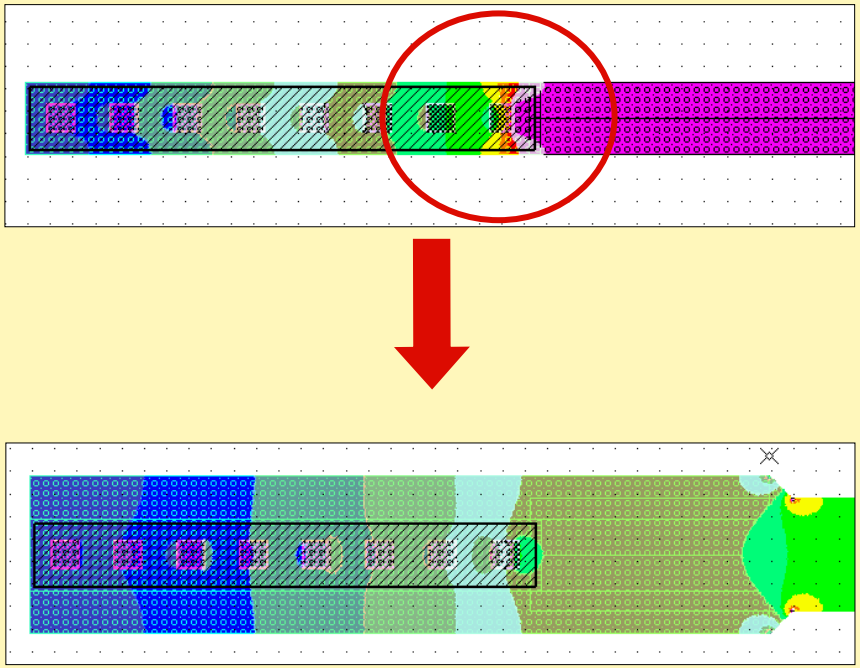
- Given: Net segments + current-density distribution ***j(x, y)***
- Objective: Determination of net segment currents i_s

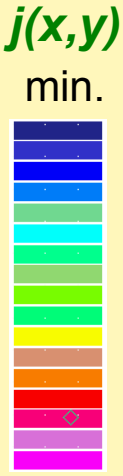
$$i_s = h_{nom} \cdot \int_0^w j(x,y) \cdot dw$$

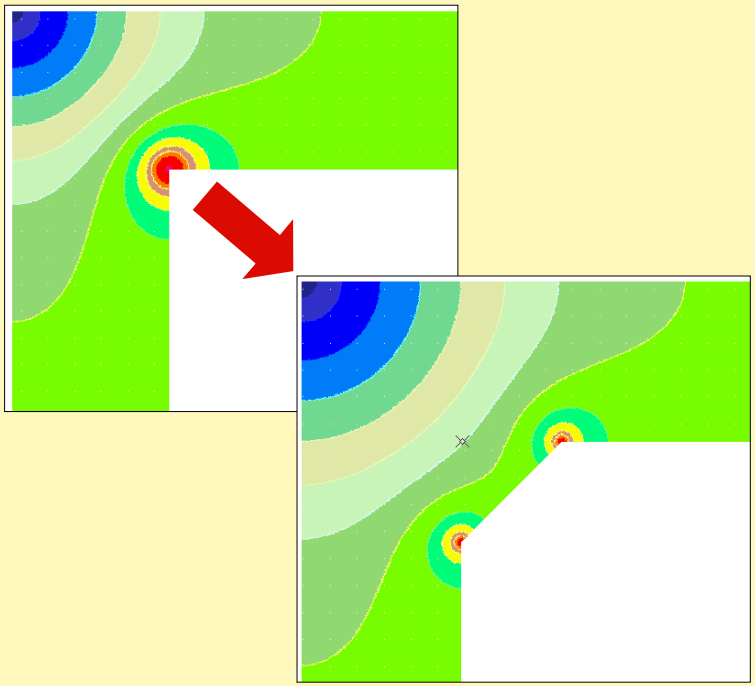


Addition of Support Polygons

- Given: Net layout and current-density distribution ***j(x, y)***
- Objective: (1) Resolve current-density problems within terminals
  (2) Current-flow homogenization

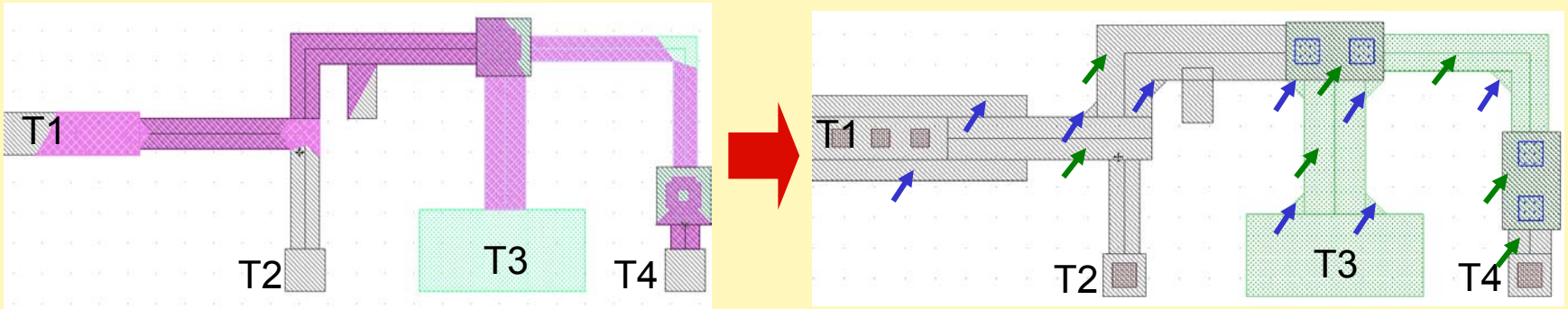






Layout Decompaction

- Given: Net layout and decompaction information
- Objective: Current-density-correct layout modification

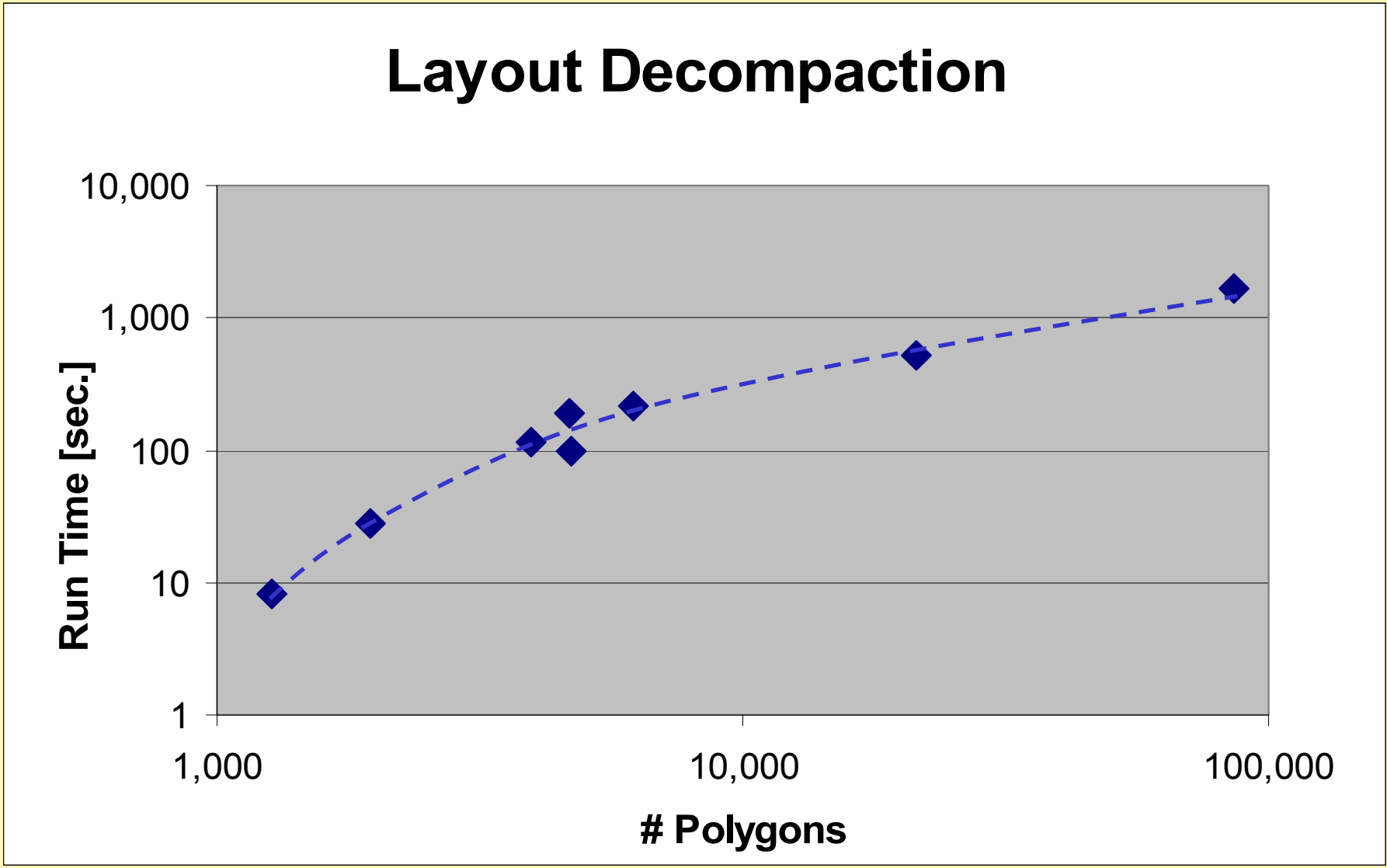


Violation Flags

(a) Wire and Via Adjustments

(b) Added Support Polygons

Results


Layout Decompaction
10,000
1,000
100
10
1
Run Time [sec.]
1,000
10,000
100,000
Polygons

Conclusion

- Our approach automatically adjusts current-density-critical layout sections of P&G and signal nets after layout generation
  - No cyclic design conflict to solve
  - Wire and via dimensions are exactly known:
    - Electromigration robust layouts
    - No wasting of route space
  - Represents a cornerstone towards a fully automated layout generation of analog- and mixed-signal ICs

- Future:
  - Net topology optimization can further improve this approach (requires additional terminal current values)
  - Current-driven layout generation (current-driven routing)