Electromigration Avoidance in Analog Circuits: Two Methodologies for Current-Driven Routing

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Overview

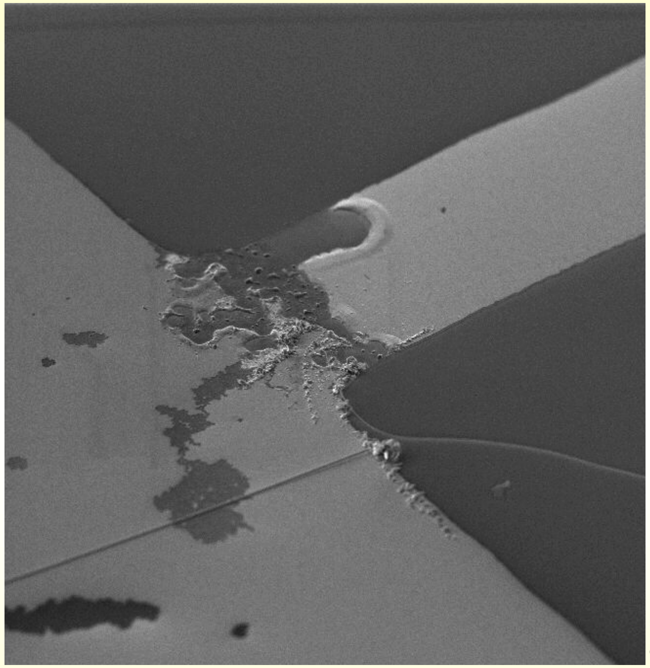
- Motivation
- Design Flow
- Current Characterization
- Global Routing Method 1: Connection Graph, Steiner Tree
- Global Routing Method 2: Terminal Tree
- Method 1 + 2: Detailed Routing
- Experimental Results

Motivation

- Analog circuits for automotive applications
  -> high currents
  -> electromigration

- Until now, commercial analog layout tools do not consider current densities during routing of signal nets

- Hence, in-house development of current-driven routing tool is necessary as an "add on" to existing design system (Mentor Graphics)



Quelle: http://ap.polyu.edu.hk/apavclo/public/gallery.htm

Definition "Current-Driven Routing"

Global routing
- (1) Determination of the routing sequence of net segments
- (2) Calculation of the current in each net segment (Kirchhoff's current law)
- (3) Calculation of the wire width of each net segment

(4) Detailed routing of the net segments in accordance with (1)

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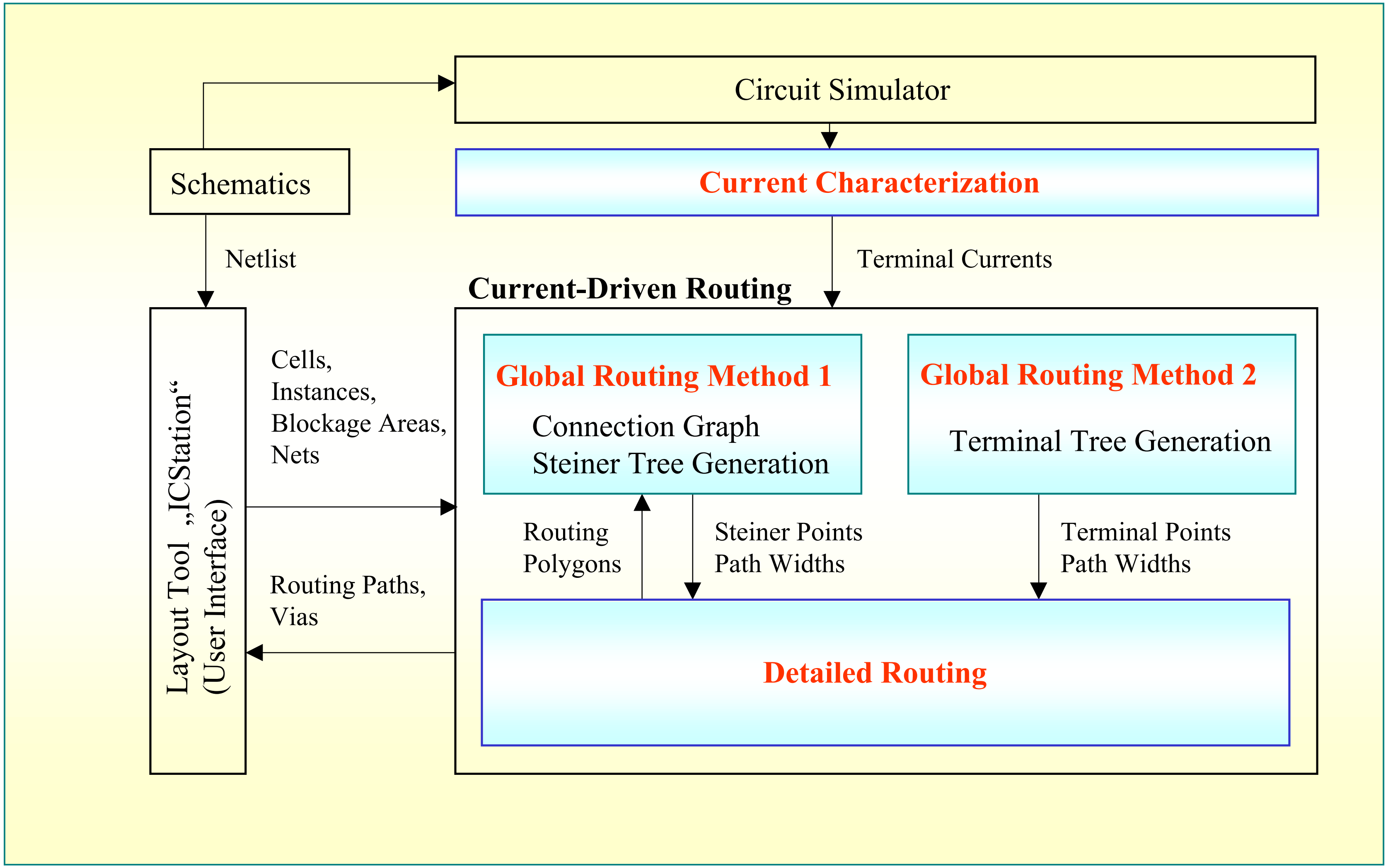
Design Flow



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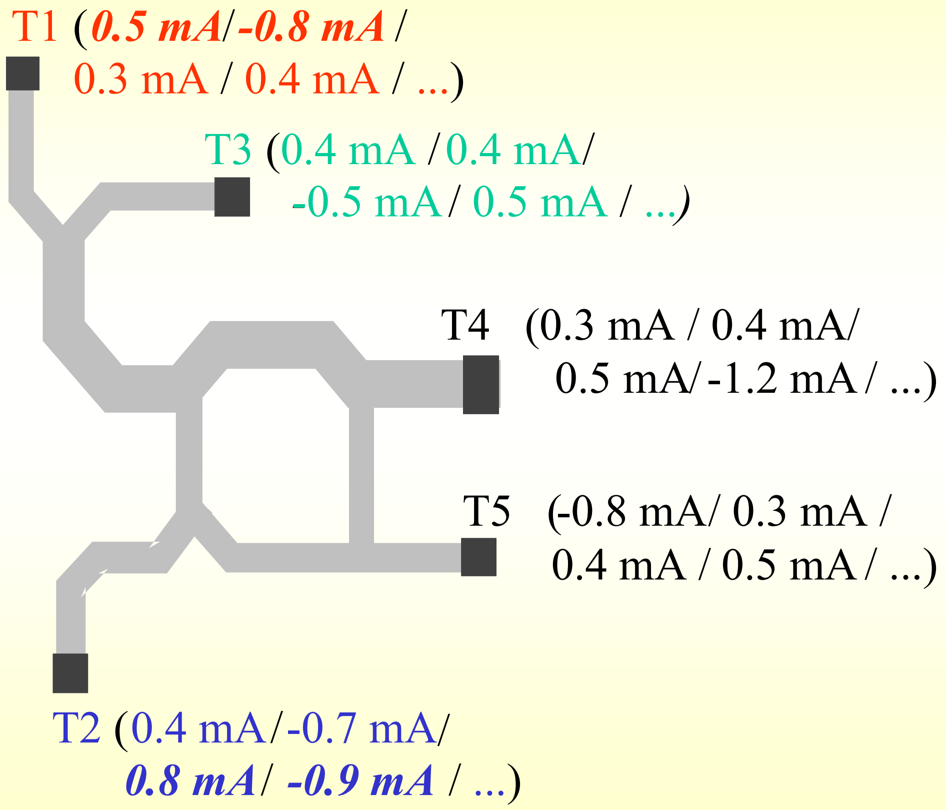
Current Characterization



	T_1	T_2	T_3	... T_n
t_{1_max}	***0.5***	0.4	0.4	...
t_{1_min}	***-0.8***	-0.7	0.4	...
t_{2_max}	0.3	***0.8***	-0.5	...
t_{2_min}	0.4	***-0.9***	0.5	...
:	:			
<2n>				

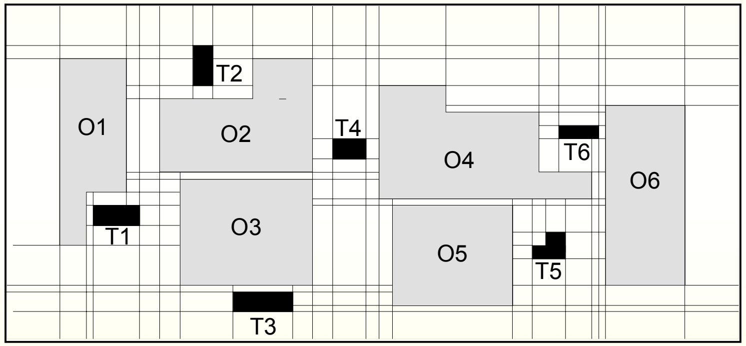
Wire Width Determination

$$w_{\min} = \max \begin{cases} \dfrac{|I_{\max}| \cdot s}{J_{peak\_Layer} \cdot d_{Layer}} \\ \\ w_{\min\_process} \end{cases}$$

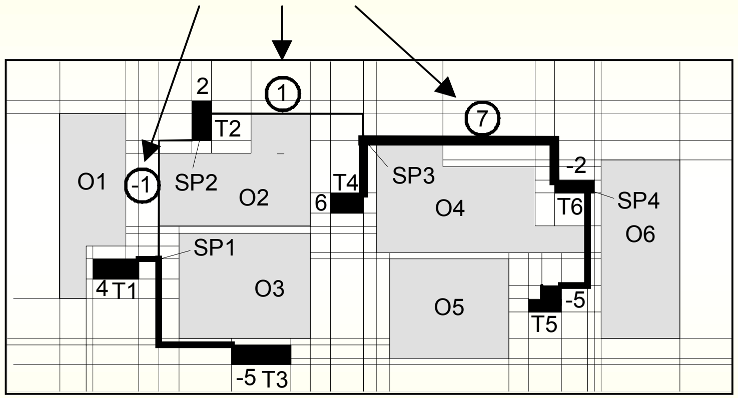
s	= safety factor ($s \approx 1.1$ .. 1.2)
d_{Layer}	= thickness of routing layer
I_{max}	= the maximum current on this path
J_{peak_Layer}	= layer dependent peak current density (process dependent)
$w_{min\_process}$	= minimum wire width determined by manufacturing process

Global Routing Method 1: Steiner Tree

Unknown currents prior to Steiner tree generation



Connection graph



Current-correct Steiner tree

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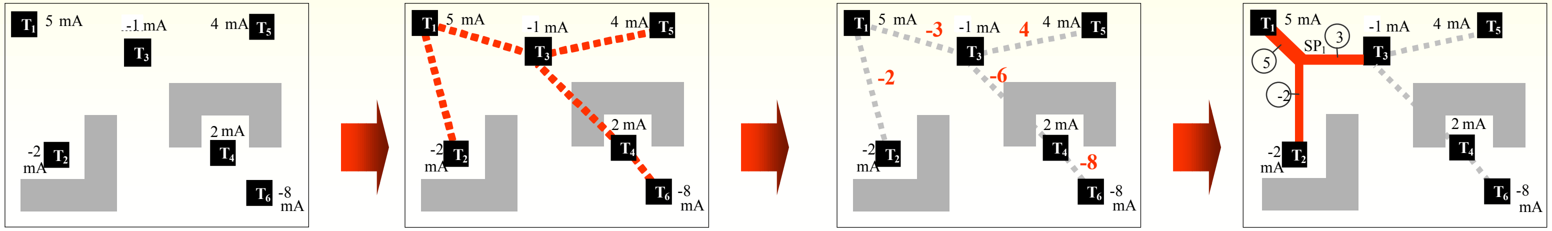
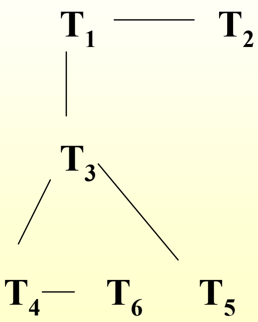
Global Routing Method 2: Terminal Tree

Given:
Terminal topology with current vectors, terminals labeled in increasing x-order



(1) Left to right, beginning with T2: Find closest terminal among previously considered terminals:
T_2 -> T_1, T_3 -> T_1, T_4 -> T_3, T_5 -> T_3, T_6 -> T_4

(2) Derive terminal tree:



(3) Calculate currents *I* of branches (from leaves inbound)
$I(T_6\text{-}T_4) = -8\text{mA}$
$I(T_4\text{-}T_3) = -6\text{mA}$
: :
$I(T_1\text{-}T_2) = -2\text{mA}$

(4) Forward terminal connections and calculated wire widths to detailed router

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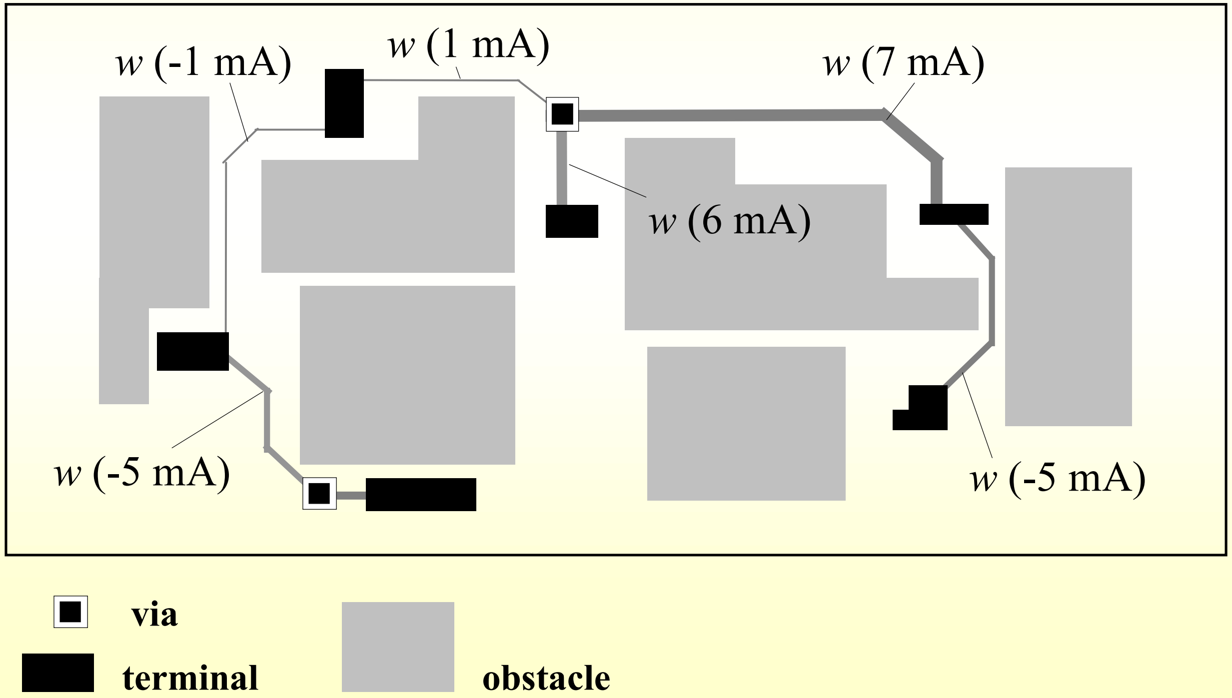
Method 1 + 2: Detailed Routing

- Oversizing
- Special spacing rules, etc.

=> see Section 7 in Paper



Experimental Results

Circuits	Cells	Terminal-to-terminal connections (Flylines)	Nets
analog1	90	116	68
analog3	132	220	96
analog5	380	370	174

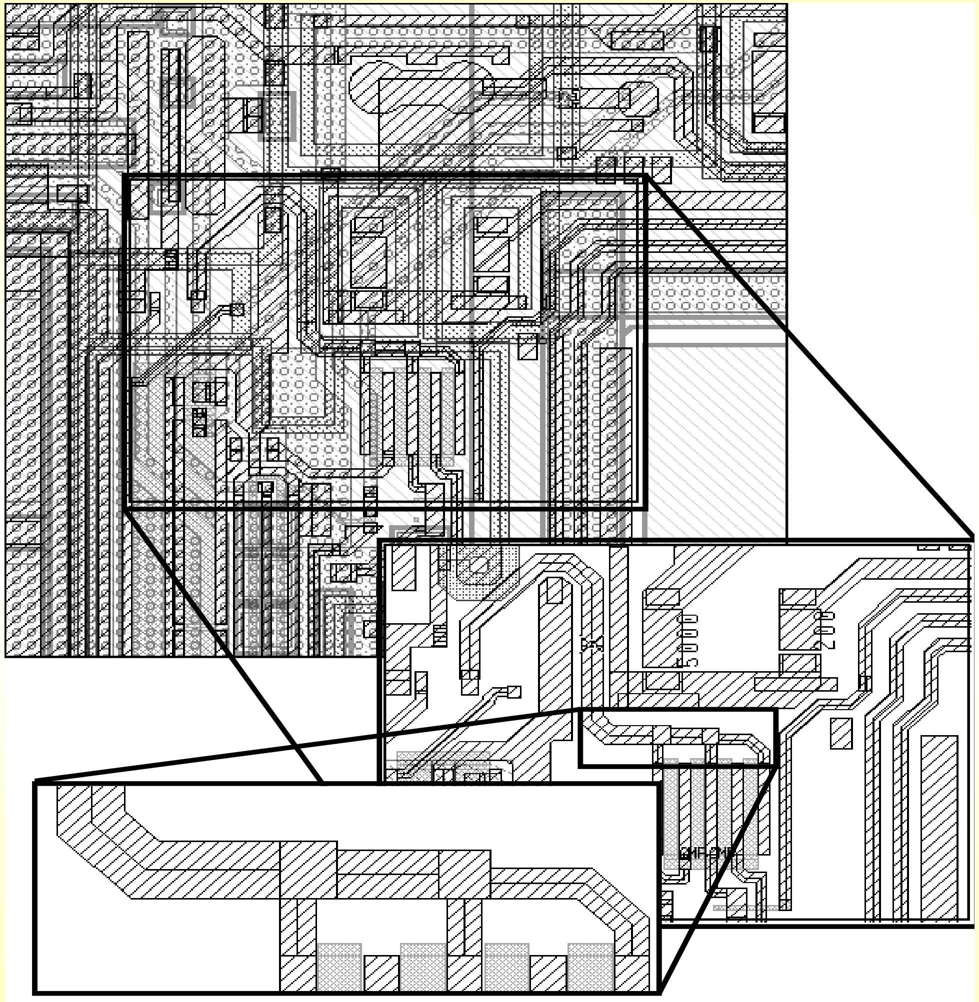
Circuits	Method	Steiner Points	Routing lengths (μm)	Vias	Area Reduction (vs. Manual Routing)
analog1	**Steiner tree**	**48**	**24342**	**142**	**-0.4 %**
	Terminal tree	**14**	**23921**	**138**	**0.0 %**
analog3	**Steiner tree**	**116**	**37201**	**266**	**-0.3 %**
	Terminal tree	**27**	**36403**	**252**	**-0.1 %**
analog5	**Steiner tree**	**234**	**45585**	**458**	**-1.1 %**
	Terminal tree	**44**	**45548**	**456**	**-0.9 %**

⇒ Routing quality is similar between both approaches, however:

- Terminal-tree-based approach is easier to implement
- Steiner-tree-based approach has problems with large complexities

⇒ Run times are only a fraction of manual current-correct routing time

Experimental Results (cont.'d)



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Summary

- Fast, yet sufficiently exact current characterization method based on current vectors
- Two global routing methodologies which calculate all branch currents *prior* to detailed routing, with the terminal-tree-based approach being the superior approach
- Efficient detailed routing which considers all constraints of current driven routing, especially varying wire widths
- Verification of our methodologies on “real world” analog circuits