Full Custom MEMS Design: 2.5D Fabrication-Process Simulation for 3D Field-Solver-Based Circuit Extraction

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***Abstract*— Due to the lack of sophisticated component libraries for microelectromechanical systems (MEMS), highly optimized MEMS sensors are currently designed using a polygon-driven design flow. The advantage of this design flow is its accurate mechanical simulation, but it lacks a method for an efficient and accurate electrostatic analysis of parasitic effects of MEMS. In order to close this gap in the polygon-driven design flow, we present a customized electrostatic analysis flow for such MEMS devices. Our flow features a 2.5D fabrication-process simulation, which simulates the three typical MEMS fabrication steps (namely deposition of materials including topography, deep reactive-ion etching, and the release etch by vapor-phase etching) very fast and on an acceptable abstraction level. Our new 2.5D fabrication-process simulation can be combined with commercial field-solvers such as they are commonly used in the design of integrated circuits. The new process simulation enables a faster but nevertheless satisfactory analysis of the electrostatic parasitic effects, and hence simplifies the electrical optimization of MEMS.**

***Index Terms*— Electrostatic analysis, parasitic extraction, process simulation, MEMS sensors.**

I. Introduction

MICROELECTROMECHANICAL systems (MEMS) devices consist, in general, of a MEMS element with mechanical structures in micrometer range and a signal processing unit with analog and digital circuits. Both components are commonly designed in parallel in two different design environments as depicted in Fig. 1 [1].

Therefore, during the last few years, the focus of research has been concentrated on the development of a component-library-driven design flow for MEMS which is similar to and integrated in the commonly used design flow for integrated analog circuits (e.g. [2]–[4]). The flaw of this approach is that the MEMS component-libraries so far available are not sophisticated enough for the design of complex and highly optimized MEMS [1]. For this reason, these MEMS are currently designed using the classic polygon-driven design flow in which the MEMS structures are manually constructed by drawing polygons.The advantage of this polygon-driven design flow is its accurate mechanical simulation, but it lacks a fast method for the precise analysis of electrostatic parasitic effects on the level of the entire chip design. Such an electrostatic analysis is necessary for the extraction of the parasitic coupling capacitances arising between the mechanical structures and the wiring. These data are essential for the electrostatic optimization and enable the advanced system-level simulations that are required for a more robust co-design of the MEMS and its corresponding evaluation circuit (ASIC, application specific integrated circuit) (Fig. 1).

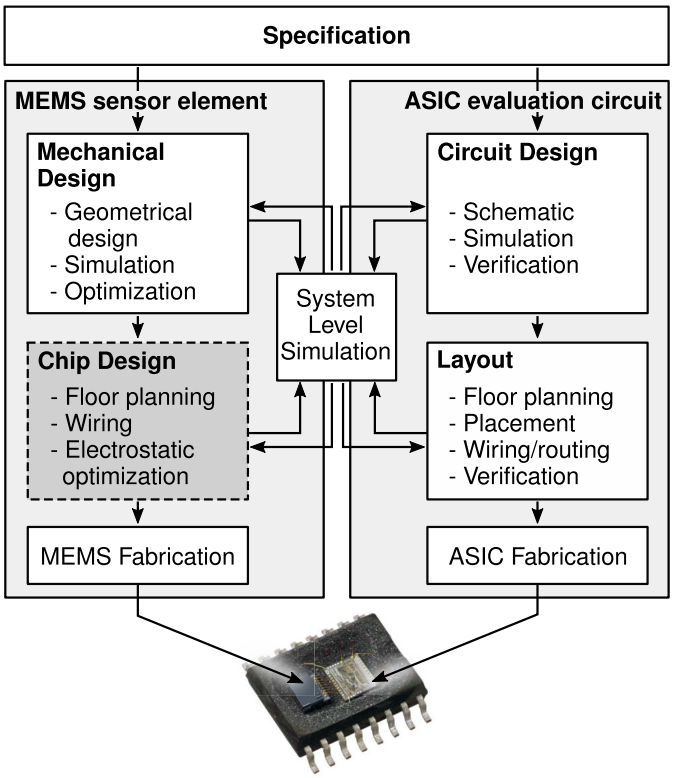

Fig. 1. A general MEMS device development flow is based on MEMS-ASIC co-design [1]. Our proposed electrostatic analysis flow is part of MEMS chip design (gray).

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The electrostatic analysis can be done by a pattern-based approach which is commonly used in the design of integrated circuits (IC) (e.g. [5] and [6]). This extraction method requires that the typically used structures are characterized and transferred into formulas prior to their use. The so defined formulas are associated with recognition patterns, which allow to apply the formulas during the electrostatic analysis to certain regions. For homogeneous regions, like the wiring in the chip frame of the MEMS, this technique is very fast and reaches a sufficient accuracy. But this is not the case for the entire MEMS element. Our own experiments showed that for complex layer stacks and highly diversified structures, as are common in today's MEMS, the assumptions in the formulas of the patterns do not meet the requirements concerning the extraction accuracy (see Sec. V and e.g., [7]). This is also related to the problem of how to model the joints between the regions defined by the patterns [5].

The electronic design automation (EDA) industry provides 3D process simulation tools (e.g. SEMulator3D [8] or IntelliSense [9]) with associated field-solvers for an electrostatic analysis. The drawback of their approaches is, that plenty of details are taken into account during the 3D process simulation and the following electrostatic analysis. During the electrostatic optimization, this leads to a long runtime or even makes this approach impractical for the analysis of huge and complex MEMS. The polygon-driven design flow lacks a tool independent, fast and simplified process simulation approach, enabling the usage of 3D field-solvers for a faster but still satisfactory parasitic extraction of MEMS. This is given when the error of the extraction results caused by the assumptions in the model and the error of the electrostatic field calculation is lower than the expected process variation, which is for wafer fabrication processes typically in the range of 5-10%.

In order to close this gap, we present in this paper a 2.5D fabrication-process simulation for the modeling of typical MEMS process technology features. It enables us to describe the layer stack of current MEMS appropriate for commercial field-solvers, which can use this data to generate a 3D model and perform an electrostatic analysis with an extraction accuracy better than the typical fabrication process variations.

In summary, this paper makes the following contributions:

(1) Customized electrostatic analysis flow which enables the usage of 3D field-solvers of the IC design domain for the parasitic extraction in MEMS design.
(2) A new 2.5D fabrication-process simulation for the modeling of typical MEMS process technology features.
(3) Demonstration of our simulation approach on a 1-axis MEMS yaw-rate sensor with a comparison to a commercial simulation tool.
(4) Verification of the extraction results by characterized test structures, using our process simulation in combination with the field-solver Calibre xAct3D [10].

The problem is described in detail in Sec. II, followed by the description of the customized electrostatic analysis flow in Sec. III. Sec. IV shows our new 2.5D fabrication-process simulation. Sec. V contains the contributions (3) and (4). The paper closes with a summary and a look at further works in Sec. VI.

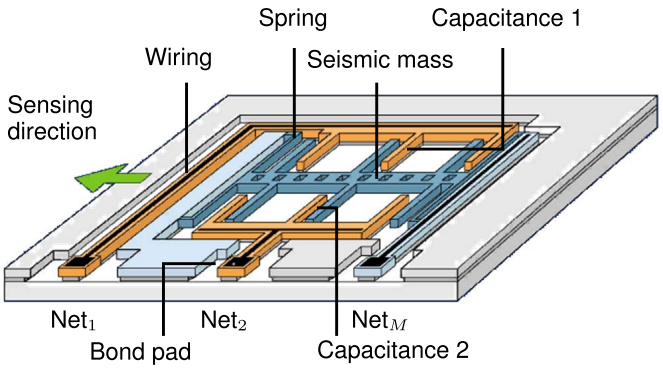

Fig. 2. General structure of a MEMS acceleration sensor [12].

II. Problem Description

Most MEMS devices are currently fabricated in silicon [11]. They are commonly composed of mobile mechanical elements and immobile wires. A prominent feature of MEMS is that the wiring and the mobile mechanical elements (which also have electrical functions) overlap. This results in parasitic coupling capacitances between the wires and the mechanical elements. Additionally, wires below mobile structures can give rise to dynamic parasitics when the structures move. These parasitic coupling capacitances can cause crosstalk between signals or positive feedback converted to a mechanical deflection, especially in MEMS sensors.

We will refine the problem for capacitive inertial MEMS sensors in the following investigation. Similar effects occur in other commonly used MEMS devices.

Conventional inertial sensors have the following structure and working principle. The sensor is composed of a seismic mass, acting as a mobile (movable) electrode that is connected by springs to anchor points. The (immobile) counter electrode structures are located close to the seismic mass. The different electrical potentials of the electrodes cause coupling capacitances to the seismic mass. Thus, moving the seismic mass causes a change in the coupling capacitance. The coupling capacitance changes are evaluated by a customized integrated circuit. Figure 2 depicts this working principle by means of a simplified acceleration sensor.

Due to the electrostatic working principle, it is necessary to perform an electrostatic optimization of the MEMS on chip level with respect to the requirements of the evaluation circuit (see Fig. 1). This includes, for example, the matching of parasitic coupling capacitances of symmetrical nets. For this reason, the development of an efficient method of accurate electrostatic analysis is essential. As mentioned in Sec. I, we tackle this problem by customizing a field-solver extraction flow from the IC design for MEMS. These field-solvers cannot model natively the very special layer stacks of MEMS inertial

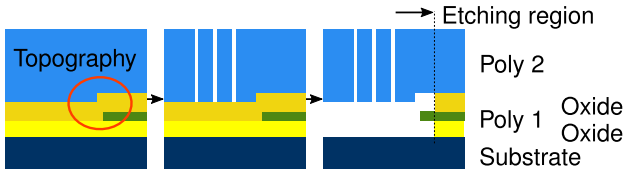

Fig. 3. Schematic cross-section of the main steps of a basic MEMS process technology [1], [11]. **Left:** deposition of all poly-silicon and oxide layers. **Center:** trenching by deep reactive-ion etching (DRIE) of the mechanical structures. **Right:** release etch of the mechanical structures by a vapor-phase etching step which removes the oxides in certain regions around the holes in the upper layer.

TABLE I
OUTLINE OF TYPICAL MEMS-TECHNOLOGY FEATURES WHICH ARE NOT COMMON IN ASIC-TECHNOLOGIES

Basic MEMS-technology	ASIC-technology
High topography steps can occur, which influence the parasitic coupling capacitances (Fig. 3, left)	Topography caused by the wiring is obviated by chemical-mechanical polishing (CMP) (e.g. [13])
High variation in the etch-rate of DRIE, which enables to etch structures with a very high aspect ratio (Fig. 3, middle, see also IV-A)	No deep trenches with a high aspect ratio are necessary, due to the thin materials in ASIC-technology in respect to MEMS-technology
Vapor-phase etching for the release of the mechanical structures (Fig. 3, right)	No comparable process step

sensors as depicted in Fig. 3. It is therefore necessary to perform a separate fabrication process simulation.

The main differences between common MEMS and ASIC-technologies are outlined in Tab. I:

All MEMS typical process features of Tab. I can be simulated by a 3D simulator like SEMulator3D [8] with a very high accuracy at the cost of the computation time. To balance the accuracy and the computation time, we present in Sec. IV our 2.5D fabrication-process simulation. In this 2.5D simulation approach we model the layers only as reduced 3D elements if it is absolutely necessary, as in the vapor-phase etching simulation and during the generation of the layer stack.

III. ELECTROSTATIC ANALYSIS FLOW

As discussed in Sec. II we decide to use a 2.5D process-simulation approach to balance the computation time and the model accuracy. Figure 4 depicts the flow of our electrostatic analysis. It uses the polygon representation of the full MEMS chip, which includes the mechanical structures, the wiring and the chip frame with its bond pads (Fig. 4, left top). Beside the geometry, the electrostatic analysis needs the definition of variable process parameters, like layer thicknesses or etch-rates (Fig. 4, right top). These inputs are combined in our 2.5D fabrication-process simulation, described in detail in Sec. IV. The process simulation generates mask layers for the structured poly-silicon and oxide layers and additionally for air gaps and topography steps (see Fig. 3). With a customized interface, a field-solver can calculate a 3D model and perform an electrostatic analysis.

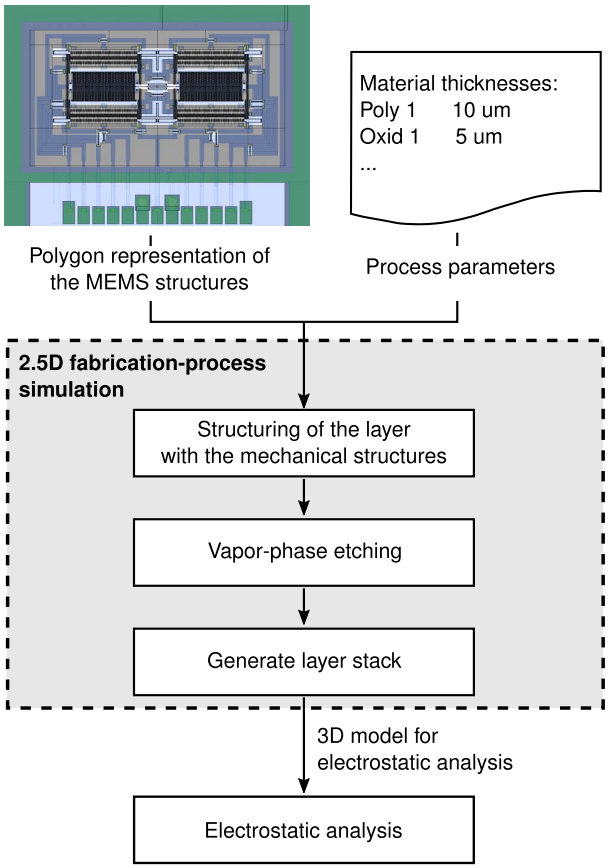

Fig. 4. Chart showing the flow of the electrostatic analysis used and the steps of our new MEMS specific 2.5D fabrication-process simulation.

IV. 2.5D FABRICATION-PROCESS SIMULATION FOR MEMS

Figure 4 shows the steps of our new MEMS specific 2.5D fabrication-process simulation. The simulation steps are described in the following subsections.

A. Structuring of the Mechanical Part

As depicted in Fig. 4, our process simulation starts with the modeling of the structuring process of the mechanical parts of the MEMS. In surface micro-machining MEMS processes, as sketched in Fig. 3, the mechanical parts are structured by deep reactive-ion Etching (DRIE [14]). This kind of etching process allows trenches with a very high aspect ratio and is one of the key process technology features for MEMS fabrication [15], [16].

The etch-rate of DRIE varies in first proximity with the width of the trenches (e.g., [17]). In relation to this etch-rate, the width of the trenches drifts from the designed trench width. In consequence, the etch-rate has an influence on the whole MEMS structure and therefore on the functional and parasitic coupling capacitances.

In common IC production, a post processing of layout data ensures that the layout structures are mapped correctly to silicon. In this automatic step the layout elements are over- or undersized to compensate edge shiftings occurring in the fabrication process. Such compensation techniques require a

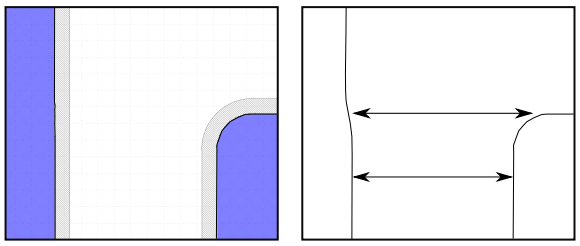

Fig. 5. Modeling of the deep reactive-ion etching (DRIE) by shifting of the edges. **Left:** Gray: designed structure, blue: structure after our simulation of the DRIE. **Right:** Amplified and schematic sketch of our approach for the modeling of the DRIE.

mature fabrication process that is stable over the whole wafer. Due to the quite young MEMS processes ([14], 1996) and the common MEMS paradigm "one product, one process", such techniques have still not been established.

Therefore, we have to model the influences of the DRIE process step in our simulation. This is done by shifting the edges of the corresponding layer by a certain value that depends firstly on the distance between opposite edges. This approach is depicted in Fig. 5.

It is quite difficult to measure and model the influences of the DRIE precisely. To cover all process corners and variations of the etch-rate of the DRIE, we recommend running at least three electrostatic analyses with a minimum, maximum and nominal shift of the edges.

B. Vapor-Phase Etching

As depicted in Fig. 4, the next step is the vapor-phase or release etch (see Fig. 3, right). In this process step, the mechanical structures are released by a vapor-phase etching step which removes the oxides in certain regions around the holes in the upper layer (see Sec. IV-A) [18].

In the simulation of the vapor-phase etching we have to model how the etch gas is spread in the layer stack. To balance the accuracy and speed, we decide to use a 2.5D simulation approach. For this model we assume that all layers are planar and have a constant thickness. The flow chart of our 2.5D vapor-phase etching algorithm is depicted in Fig. 6 and a schematic demonstration is given in Fig. 7.

The etch gas is introduced through the holes in the top layer which is in our case the layer with the mechanical structures. Therefore, the apertures for the etch gas are defined by the simulation of the DRIE, described in Sec. IV-A. As depicted in Fig. 6, the apertures in the top layer are the seed layer for the initial vertical etch step that defines the first *etch mask*. The following three steps are repeated until the predefined maximum etch depth of the vapor-phase etching is reached.

1) Horizontal etch step: lateral size by the predefined etch step size of the current etch mask.
2) Vertical etch step: copy the previous etch mask to the layer above and below.
3) Analyze material: check with which material the etch masks are overlapping. If it is oxide, the etching process can continue with the current etch mask. If it is poly-silicon, the etching will stop at this place.

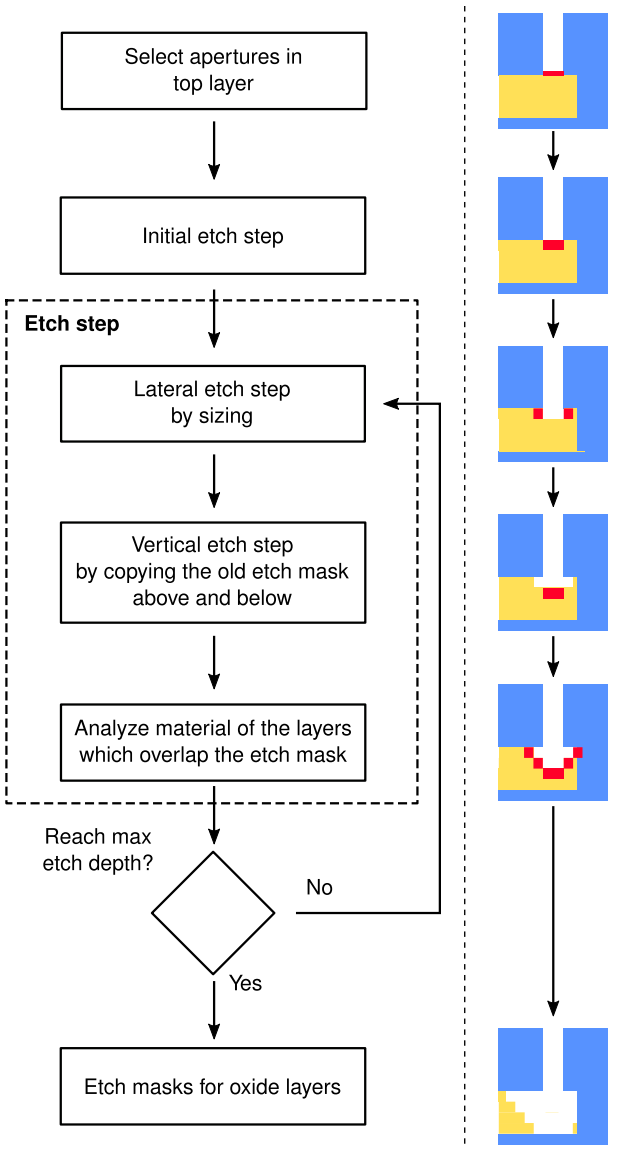

Fig. 6. Flow chart of our 2.5D vapor-phase etching algorithm on the left and on the right the corresponding visualization on a minimal example.

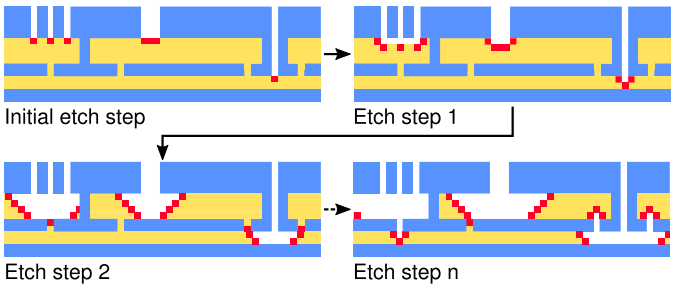

Fig. 7. Schematic demonstration of our 2.5D vapor-phase etching algorithm.

To synchronize the horizontal and vertical etch speed, we split up the oxide layers (in yellow) into slices whose thickness is equal to the horizontal etch step size (Fig. 7).

C. Generate Layer Stack

The simulation of the trenching by DRIE (Sec. IV-A) delivers the masks for the poly-silicon layers, and the vapor-phase

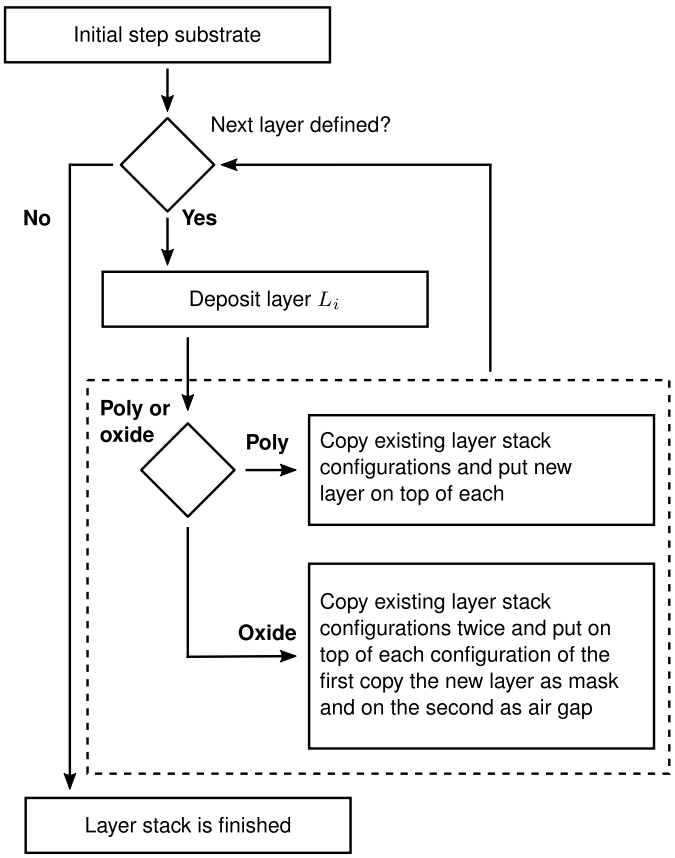

Fig. 8. Flow chart of our deposition algorithm which generates the layer stack configurations for the electrostatic analysis.

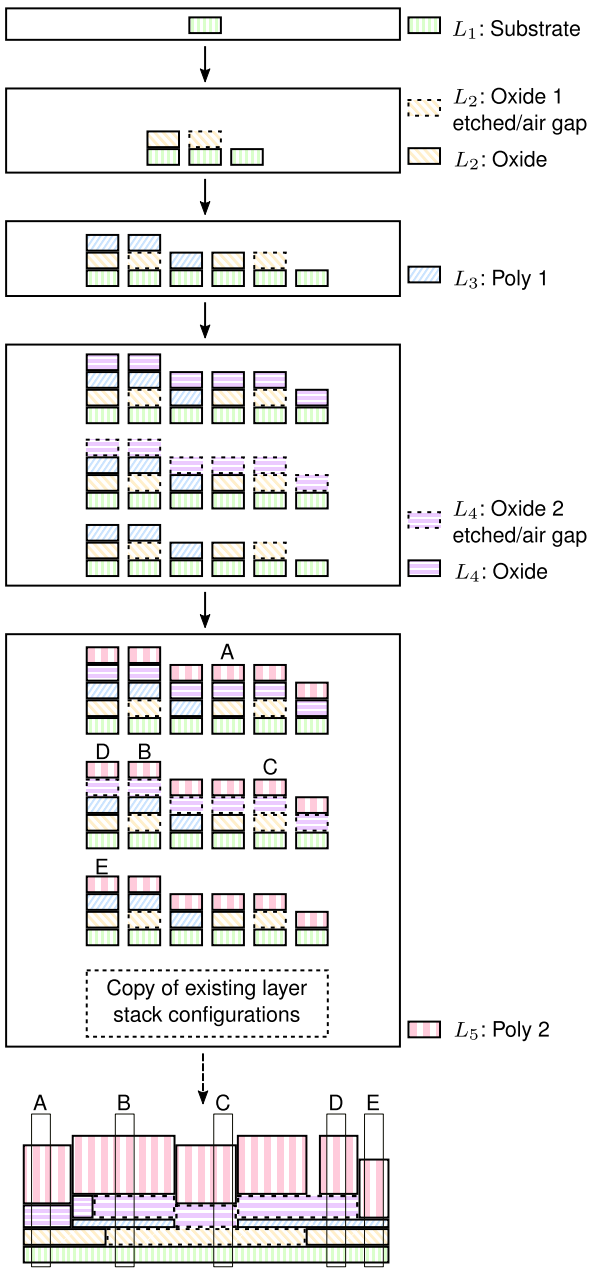

Fig. 9. Visualization of our deposition algorithm on the basic process technology of Fig. 3. The initial step is followed by the deposition of two oxide and two poly-silicon layers. At the bottom is a schematic example of a layer stack with some highlighted layer stack configurations.

etching simulation of Sec. IV-B the mask layers for the oxide and air gaps. On the basis of these data, we construct the layer stack for the electrostatic analysis in the following.

As depicted in Fig. 3, the poly-silicon and oxide layers are deposited and in some cases structured successively. The deposition of the materials causes topography steps (e.g., [18]) that can affect the output signal of the MEMS (see Sec. II). For a satisfactory electrostatic analysis, it is necessary to include such topography steps in the model. Therefore, we simulate the deposition of the materials by stacking and combining them in all possible ways. A flow chart of the algorithm is given in Fig. 8 and in Fig. 9 the algorithm is visualized on the basic process technology depicted in Fig. 3.

For a better approximation to the deposition of a material, we introduce a lateral size of each deposited layer. This lateral size depends on the thickness of the underlying material (Fig. 10, right, compare overlap of upper yellow and upper blue layer).

Figure 10 shows the layer stack and the modeling of topography steps of the basic process technology depicted in Fig. 3.

V. Demonstration & Verification

In this section, we demonstrate our new 2.5D process simulation on a MEMS-sensor and compare the simulation results to the very accurate 3D model of SEMulator3D [8] of Coventor. Afterwards, we show on a set of 57 characterized test structures that the model of our 2.5D process simulation can be used for a field-solver-based electrostatic analysis with an extraction accuracy better than the expected fabrication process variations of 5-10%.

For the demonstration, we use the one-axis gyroscope MEMS-sensor depicted in Fig. 11. The sensor is designed in the basic two-poly-layer technology, shown in Fig. 3.

We have implemented the 2.5D process simulation in CalibreDRC [10] and run the simulation with a vapor-phase etch step size of 200 nm. For comparison, we run the process simulation for the demonstration sensor by SEMulator3D with

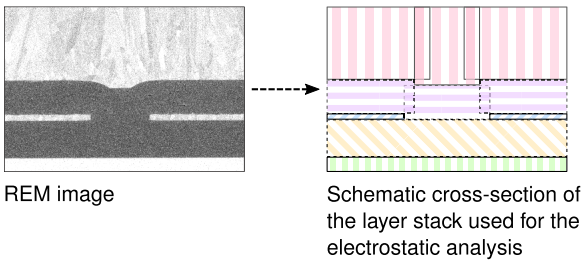

Fig. 10. Modeling of the basic process technology depicted in Fig. 3 with topography steps.

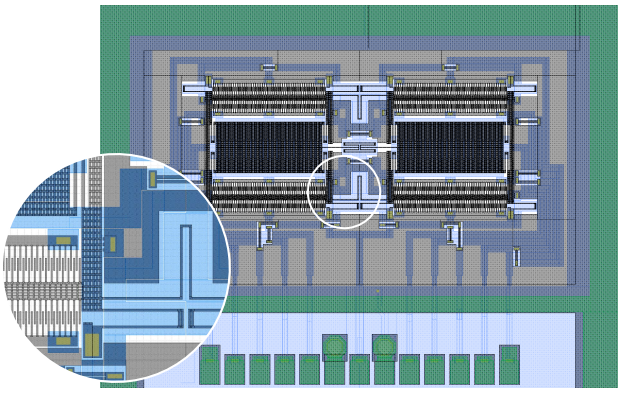

Fig. 11. Layout of an one-axis gyroscope MEMS-sensor [19].

a Voxel size of 200 nm. Figure 12 shows a part of the demonstration sensor in top-view after the simulation in both tools, wherein SEMulator3D needs about 7 minutes for the calculation and our simplified process simulation implemented in CalibreDRC about 1 minute. Even in this very small and simple MEMS sensor example, there is a remarkable difference in the runtime between the two approaches.

As described in Sec. IV, our model also includes the 3D topography information, provided in separate topography layers. For a better visualization of the calculated topography (see. Fig. 13), we use the tool xActview of Mentor Graphics, which is included in the field-solver Calibre xAct3D [10].

The model of SEMulator3D includes far more details (e.g. roughness of the sidewalls caused by the DRIE) as our simplified model. Nevertheless, we show in the following that our approach enables an electrostatic analysis of a MEMS by a field-solver with a very fast process simulation, which meets the above defined requirements.

For this purpose, we use a set of 57 special test structures. These were designed, fabricated and characterized in the framework of the publicly funded project MEMS2015 [20].

The test structures include typical MEMS structures like perforated plates, non-Manhattan framework structures and electrode-comb structures. A subset of these is shown in Fig. 14.

To be as close as possible to real MEMS structures, the test structures are designed using different layer stack variations (see Sec. IV-C). As depicted in Fig. 14, the lower halves of the structures shown have partly wires (Poly 1) under the

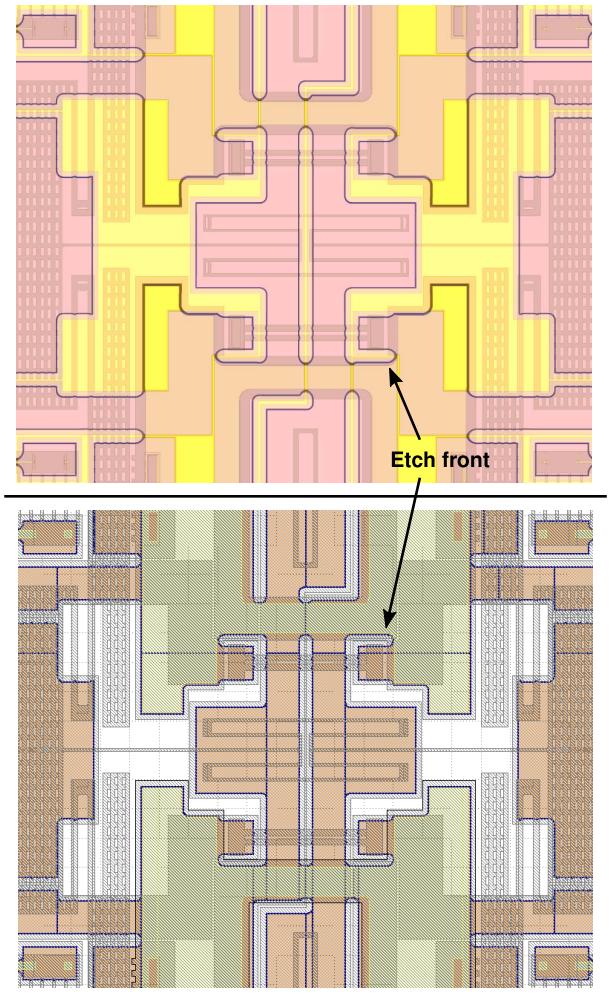

Fig. 12. **Top:** Top-view on the SEMulator3D [8] model. **Bottom:** Top-view on output model of our 2.5D process simulation. The MEMS sensor is designed in the basic two-poly-layer technology, shown in Fig. 3. Please note the black-marked boarder of the etch front in the oxide 1 of the vapor-phase etching.

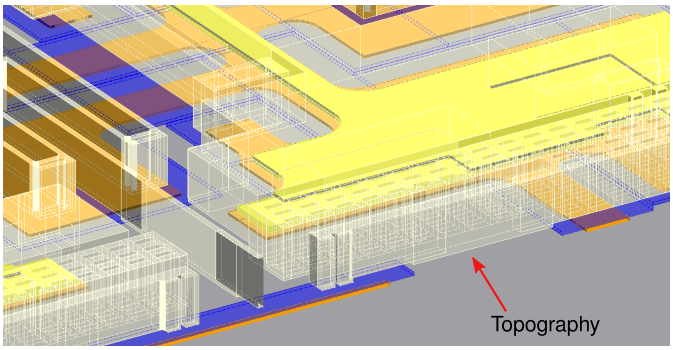

Fig. 13. Visualization of the internal 3D model of the field-solver Calibre xAct3D with xActview [10]. The figure shows a cross-section through the 3D stack. Note the topography step, calculated by our presented 2.5D process simulation.

structures in the upper layer (Poly 2). This configuration will cause topography steps (see Fig. 3 and Sec. IV-C).

We used the field-solver Calibre xAct3D by Mentor Graphics [10] for verification. Nevertheless, our process simulation is

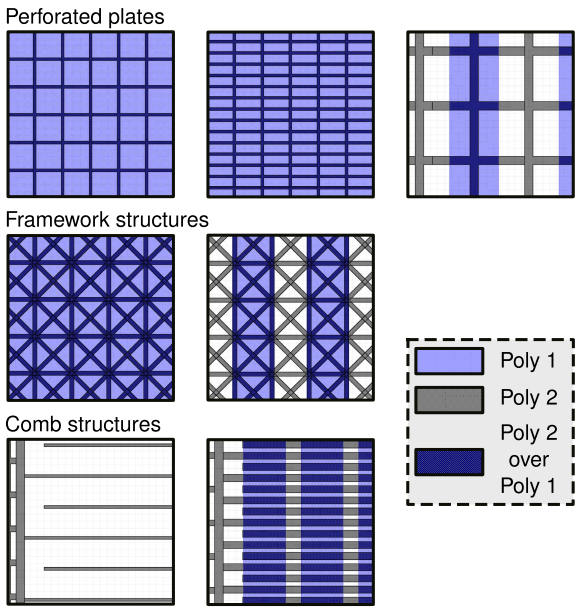

Fig. 14. Verification test structures fabricated using the basic process technology depicted in Fig. 3.

TABLE II

OVERVIEW OF THE ACCURACY AND RUNTIME OF THE DIFFERENT EXTRACTION METHODS AND THE INFLUENCE OF THE DRIE SIMULATION ON THE EXTRACTION ACCURACY ON A TOTAL OF 57 TEST STRUCTURES (FIG. 14)

Tool	Field-solver	Field-solver	Pattern
Sim. of DRIE	constant	dynamic	constant
Error [%]	3.27	2.71	24.83

tool independent and can be combined with other field-solvers by a customized interface.

In the first step we performed an electrostatic analysis, assuming that the etch-rate of the deep reactive-ion etching is constant over the whole chip. Afterwards, we performed another electrostatic analysis with the same setting, except of the DRIE simulation. In this case we used the environmental dependent etch-shift approach, described in Sec. IV-A. The deviation on average of the measured values of both extractions are shown in Table II. The more accurate modeling of the DRIE allows us to tune the absolute extraction accuracy to an average error below 3%, which is better than the typical fabrication process deviations of 5-10%.

For reasons of completeness, we also run the electrostatic analysis by our old pattern based approach (Table II, right column). The extraction is very fast, but the absolute extraction results deviate on average by 25% of the measured values (Table II). The version used is optimized for the analysis of perforated plates with square holes, which were the dominant structure-type in MEMS design. This analytic approximation does not fit very well the analysis of non-Manhattan framework structures, as are commonly used nowadays. Additionally, the fabrication process's inherent topography steps and the interface between the regions of the patterns are not accurately modeled.

As a conclusion, the parasitic extraction by a field-solver on base of the model of our 2.5D process simulation leads to satisfactory absolute extractions results, which enables the faster optimization of the electrostatic parasitic effects. Beside the absolute extraction results, we also have the benefit of the very high tool inherent relative extraction accuracy, which is even more important for the design of nowadays MEMS sensors.

VI. SUMMARY AND OUTLOOK

We present in this paper a parasitic extraction flow for MEMS, designed in a polygon-driven design flow. Our extraction flow features a very fast 2.5D process simulation. The latter enables the usage of commercial field-solvers from the IC design domain and accelerates the electrostatic analysis and the electrical optimization of MEMS. We demonstrate our 2.5D process simulation on a capacitive MEMS gyroscope sensor and compare the results to the model of a commercial process simulation tool. Additionally, we verify by characterized test structures that our simplified model can be used for a satisfactory electrostatic analysis by a field-solver. Its extraction accuracy is better than the typical expected fabrication process variations.

Our rule-based structure recognition method of [21] and [1] can be integrated in the presented extraction flow. The method allows us to split the nets of a MEMS into meaningful subnets. The recognized subnets enable the back annotation of extracted parasitic capacitances to parts of the MEMS geometry.

So far, the electrostatic analysis by a field-solver of a polygon-based designed MEMS has been limited to parasitic capacitances. We plan to upgrade our extraction flow to enable the parallel resistance and capacitance extraction in the future.

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