Increasing EM Robustness of Placement and Routing Solutions based on Layout-Driven Discretization

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***Abstract*—Nowadays, electromigration (EM) is mainly addressed in the verification step. This is no longer possible due to the ever increasing number of EM failures in the future. An EM-aware physical synthesis could reduce the number of critical locations but the layout complexities prevent this from already being used. To solve this problem, we propose a novel method to discretize placement and routing solutions to enable a fast EM analysis. In addition, we suggest adjustments in the placement and routing step to enhance the EM robustness based on early analysis results. In contrast to the standard approach of running a numerical simulation outside the physical design step and after the synthesis, we perform most of the analysis steps within our placement and routing tools to consider the results; thus enabling early and specialized EM-robust solutions. Particularly, our methodology exploits layout structures to enable an efficient discretization inside the geometrical representations of synthesis tools. We demonstrate how to reduce the discretization effort significantly while achieving sufficient accuracy to improve EM robustness.**

***Index Terms*—Reliability, Electromigration, Placement, Routing**

I. Introduction

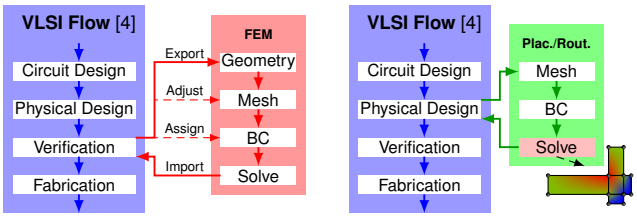
The semiconductor industry continuously upgrades the performance of very large scale integration (VLSI) circuits with every new technology node. This leads to an ongoing downscaling of the transistor dimensions and a subsequent shrinking of interconnects.

Electromigration (EM) is a process of material migration caused by the momentum exchange between moving electrons and lattice atoms. The main driving force behind EM is current density, but it also depends on temperature, among other things. Both factors are increasing over time, escalating the EM impact. The International Technology Roadmap for Semiconductors (ITRS) predicts EM damage to worsen significantly in the future, while at the same time claiming that there are no known solutions [1].

To assure the EM robustness of a layout, circuit designers use rule-based verification tools or spatial discretization methods, e.g., the finite element method (FEM). The former are based on simplified models and the latter are typically performed on only parts of the layout due to its complexity. The usual goal of the FEM is to develop a simplified model, which can then be incorporated in a verification tool. Examples of this methodology are presented in [2], [3] and [4].

In this paper, we present a method to close the gap between the aforementioned simplified EM analysis and a complex FEM simulation. We suggest performing most of the analysis steps within existing electronic design automation (EDA) tools and to incorporate the EM results in order to synthesize EM robust solutions (compare Fig. 1). This is becoming increasingly important because of the increasing number of EM problems in the verification step. In the future, fast analyses integrated within the synthesis tools are needed to estimate the layout robustness as early as possible to take appropriate countermeasures.

As illustrated in Fig. 1, we integrate basic analysis steps such as the discretization and the boundary condition (BC) assignment step into the placement and routing tools based on their layout representations. While these steps are carried out using an in-house tool, we exploit an external tool only for solving the already discretized EM equations.



(a) Standard method (b) Proposed method

Fig. 1. Illustrating the difference between the (a) standard method and (b) the proposed method. Our suggestion is performing the discretization and boundary condition assignments (analysis steps) within the placement and routing tools and during synthesis. This generates fast EM results and enables synthesis algorithms to improve their results.

To integrate the analysis steps and to reduce the discretization time (which can take up to 80% of the overall analysis time [6]), we also develop algorithms to discretize placement and routing structures. These algorithms are incorporated in the placement and routing step, respectively.

Summarized, our main contributions are

- a new method for an EM analysis based on algorithms to discretize placement and routing solutions within EDA tools achieving a comparable result quality to an FEM simulation while significantly reducing the problem complexity, and
- procedures on how to consider these EM results within the placement and routing algorithms in order to synthesize EM-robust layouts.

II. Electromigration

A. Physical Model

The physical EM model contains the electrical, mechanical and thermal domains as depicted in Fig. 2.

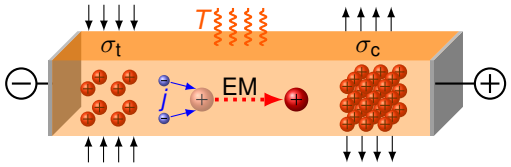


Fig. 2. Because of the collision of the electrons (blue) with the atoms (red), atoms migrate in the electron flow direction. This depletes atoms at the cathode and accumulates them at the anode. The change of concentration introduces tensile ($\sigma_t > 0$) and compressive stresses ($\sigma_c < 0$), respectively. At the same time, the current flow heats the interconnect due to Joule heating.

To describe the effect of EM, the governing equations are Fick's first and second law. In the presence of an external force, such as a current density or a stress gradient, Fick's first law (describing the atomic flux $\vec{J}$ of chemical diffusion (CD)) is extended by the atomic flux of EM and stressmigration (SM) given by

$$\vec{J} = \vec{J}_{\mathrm{CD}} + \vec{J}_{\mathrm{EM}} + \vec{J}_{\mathrm{SM}} = -D\nabla C + \frac{CD}{kT} eZ^* \rho \vec{j} + \frac{CD}{kT} \Omega \nabla \sigma, \quad (1)$$

where the concentration gradient ∇C, the stress gradient $\nabla\sigma$ and the current density $\vec{j}$ are the main driving forces of the atomic flux [7]. It also depends on the diffusion coefficient D, Boltzmann's constant k, the temperature T, the charge of an electron e, the effective charge number Z^*, the resistivity ρ and the atomic volume Ω. Fick's second law (the mass balance equation) given by

$$\frac{\partial C}{\partial t} = -\nabla \cdot \vec{J} + G, \quad (2)$$

expresses the change of the atom concentration over time depending on the divergence of the atomic flux and a generation/annihilation rate G. Korhonen et al. [8] presented a one dimensional mechanical stress equation derived from Eq. (2) by neglecting the chemical diffusion and the generation/annihilation term and using Hooke's law ($\partial\sigma = -B\partial C/C$) with the bulk module B to express the stress caused by EM as

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB}{kT}\left(eZ^*\rho j + \Omega\frac{\partial \sigma}{\partial x}\right)\right]. \quad (3)$$

To calculate the EM stress in Eq. (3), one must also solve the electrokinetic and heat equation for static problems to calculate the current density and temperature, respectively.

B. Numerical Techniques

To obtain a solution for the problems presented in Sec. II-A, analytical means are not suitable due to the complexity of the physical equations and the geometries that are investigated. Therefore, numerical techniques such as FEM, finite difference (FD) or finite volume (FV) schemes are required. Since we separated the discretization from the solving step, we can utilize any solver. We calculate the heat map by an in-house tool using the finite integration technique (FIT) [9], which is similar to FD and FV schemes. The commercial FEM solver from *ANSYS* solves Eq. (3).

III. Discretization

This section presents the algorithms to discretize placement and routing solutions to model cell placements and interconnect structures. To estimate EM effects, the placement discretization enables a fast temperature simulation based on the placement. The interconnect discretization enables a fast EM estimation on routing results due to a small number of elements.

A. Discretization of Placement Structures

We developed the algorithm to enable a fast discretization of the current placements in order to calculate the heat distribution within a chip. We suggest using the regular placement grid as the discretization template with optional subdivision. Therefore, we discretize only once before the first placement solution is calculated and then, we reuse this discretization after a new placement has been calculated. Furthermore, we use an *rtree* from the *boost geometry* library to map our elements to the newly calculated cell positions. This means that we can iterate through our elements and query the *rtree* to determine simulation parameters like power dissipation or material properties at the corresponding locations. Fig. 3a-c show this procedure. By adding the third dimension to Fig. 3a, one can model the entire chip as shown in Fig. 3d to consider Joule heating within interconnects if a routing solution is provided. Since the placement discretization might be too coarse for interconnects, one has to scale the current densities within the elements covering a part of an interconnect to keep the power generation constant.

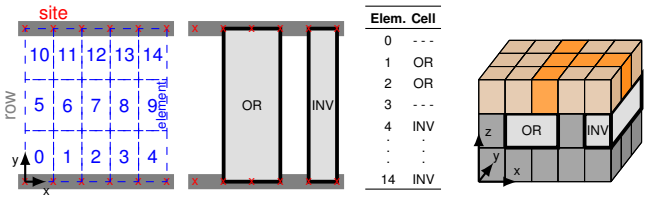


Fig. 3. (a) Generated elements (blue) align with the placement sites (red). (b) Geometric placement representation for fast querying. (c) Mapping of element properties to cell locations. (d) Procedure can be repeated for all layers.

B. Discretization of Routing Structures

To perform a fast EM analysis on interconnects while routing, we propose an algorithm to discretize routing structures, which aligns elements according to the geometry of the interconnects. Fig. 4 shows an exemplary interconnect structure to demonstrate the algorithm.

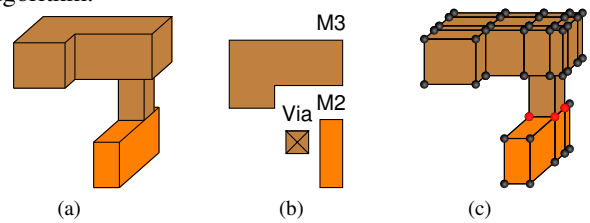


Fig. 4. (a) Exemplary interconnect. (b) Decomposition of (a) into layers M2, Via and M3. (c) Generated elements on each layer. The colors represent continuous material and the red circles electrically coupled nodes.

The algorithm to discretize interconnects operates in the following three steps (Fig. 5): (1) Remove vias from layer, (2) generate maximum rectangles and (3) recursively decompose the maximum rectangles into non-overlapping rectangles. In the first step, the vias are subtracted from the connecting routing layers and stored as one element. The second step creates maximum rectangles within the resulting structure on each layer. A maximum rectangle is a rectangle which extends in the x and y directions until it touches the structure borders at both sides. The third step decomposes recursively the maximum rectangles into overlapping and non-overlapping rectangles. The former are gathered for a re-run and the latter become elements.

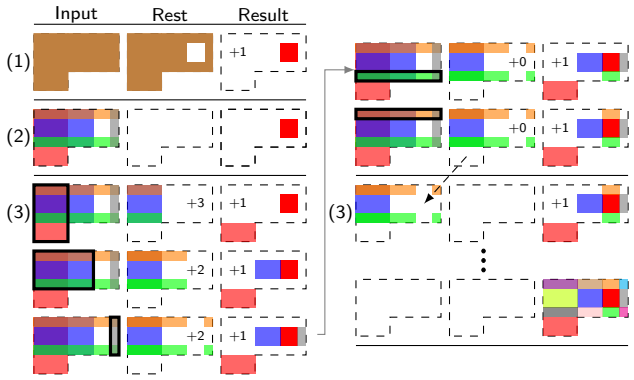


Fig. 5. Discretization of the routing structures. (1) Subtraction of vias from routing layer. (2) Construction of maximum rectangles. (3) Decomposition of maximum rectangles into overlapping and non-overlapping rectangle (become elements). The numbers +1, +2 and +3 represent the number of added rectangles per column and step.

To address the state of the art *dual-damascene-techniques (DDT)*, elements represent continuous materials within each copper layer (brown and orange color in Fig. 4c). Between the different copper layers, we couple the electrical domains of coincident nodes (red nodes in Fig. 4c). This blocks the migration between the layers as given by the DDT.

IV. Simulation Results

A. Case Study

In this section, we assume that we have identified one net connecting three cells and driving a relatively high current compared to the other nets in the *multiplier plus adder* design from [10]. Therefore, this net is potentially EM critical. We demonstrate how the placement and routing step can reduce the EM risk of this net by running and considering a thermal analysis in the placement and a stress analysis in the routing step. As mentioned in Sec. I, we use our in-house placement and routing tools to perform the discretization, to assign the BCs and to call the external solver (Fig. 1).

B. Placement with Temperature Consideration

Since most of the placement algorithms iteratively calculate cell locations, we suggest performing temperature simulations in between these iterations and consider high temperature locations as inconvenient locations for EM critical cells. Our proposed strategy is to perform the discretization step before the first placement iteration to create elements aligned to the placement sites as shown in Fig. 3. In between the different iterations, we pause the computation of the cell locations to run the thermal analysis. We suggest considering the current placement solution by performing geometry queries with all element locations to determine the properties such as material or power generation (given by the corresponding data sheets of the physical design kit). These queries are typically very fast. At the end, we transfer the element property information together with the appropriate boundary conditions to a solver to calculate the temperature map. Here, we use an in-house FIT tool solving the heat equation for static problems. In the next placement iteration, we consider the heat results (Fig. 6) and move critical cells out of hot areas by adding pseudo nets and pins, which drag these cells to less critical areas.

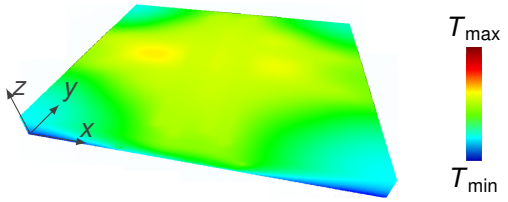


Fig. 6. Three-dimensional heat map of the case study layout. Our algorithm discretizes the placement solution and we solve the static heat equation with appropriate BCs by an in-house FIT solver.

The temperature map in Fig. 6 shows that sites close to the corners of the chip are favorable for EM critical cells (Fig. 7) because of the lower temperatures compared to the center.

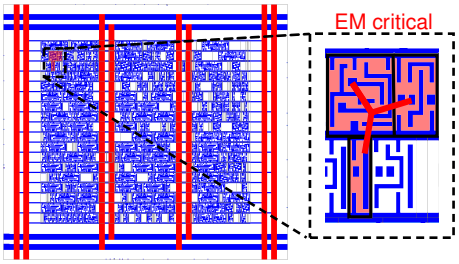


Fig. 7. Case study layout with zoom in to the EM critical cells. Locations close to the corners of the layout are favorable for EM critical cells.

C. Routing with Stress Consideration

To estimate the EM effects while routing, we run current density and stress analyses. Since EM moves atoms and changes atom concentrations, hydrostatic stress builds up within the interconnect, which we refer to as stress. Our analysis includes the effect of SM, which counteracts EM to reduce the stress gradient.

In this work, the interconnect dimensions are taken from the process design kit of [10]. The current values are given in look up tables (depending on the parasitics) in [11], which are assigned as boundary conditions to the end of each interconnect.

Our idea of an EM-aware routing is the following: First, we calculate a routing solution. Second, we use our algorithm to discretize the interconnects within the router. Third, we transfer the elements and boundary conditions to an external solver that calculates stress results by solving Eq. (3)

in all three dimensions. In the last step, we control the commercial router from *Cadence* through its interface function `setAttribute` with the argument {`bottom`,`top`}`_preferred_routing_layer` to avoid the critical routing layer with the maximum stress.

To investigate the result quality of our approach, we simulate the interconnect structure of the critical net from Fig. 7 with the *ANSYS* FEM tool which we refer to as the standard method. The top row of Fig. 8 shows the discretization and stress values of the standard and our method. Both stress results of the initial routing solution identify the maximum stress on metal 2 and therefore, we instruct the router to prefer metal 3. As a result, we generated an improved solution (bottom row of Fig. 8), which experiences around 25% less tensile stress than the standard solution and thus, significantly prolongs the lifetime of the interconnect. Although we choose a much coarser discretization, our method still leads to the avoidance of the same metal layer without time-consuming discretization.

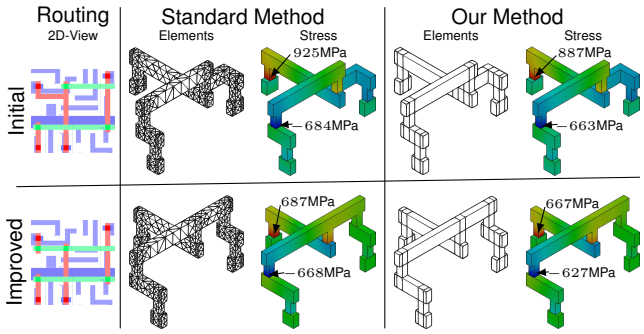


Fig. 8. Comparison between the initial and improved routing solution with stress results calculated by the standard and our method.

Tab. I shows that the principle stress results are qualitatively in good agreement between the standard and our method. However, our approach uses fewer elements on straight lines. Therefore, we trade result quality for a smaller problem size since the current density (main driving force of EM) is almost constant within a straight line. This is a reasonable inaccuracy to enable fast EM estimations on different routing solutions.

TABLE I
COMPLEXITY AND RESULT COMPARISON OF THE IMPROVED ROUTING SOLUTION BETWEEN THE STANDARD AND OUR METHOD.

Characteristic	Standard Method	Our Method	Relative Difference
Elements	1596	36	98%
Runtime	69s	11s	84%
Max. Stress	687 MPa	667 MPa	3%
Min. Stress	-668 MPa	-627 MPa	6%

D. Discretization Performance

To show the performance of our discretization algorithms, we test it on four benchmarks with different problem sizes. They are synthesized with the technology and cell library from [10] and [11], respectively. The problem sizes range from a small analog design to a large digital design. Our benchmark suite contains a *clock divider*, *counter*, *multiplier plus adder* from [10] and the *OpenRISC 1200* core from [12]. Tab. II demonstrates that our algorithms are capable to discretize large designs in a reasonable amount of time on a single core of an Intel Xeon E5-2620 at 2.40 GHz.

TABLE II
ELEMENT NUMBER AND DISCRETIZATION TIME

		Placement-driven		Interconnect-driven	
Design	Nets	Elements	Time	Elements	Time
Divider	5	660	<1s	44	<1s
Counter	15	137K	<1s	13K	1s
Mult/Add	344	467K	3s	34K	7s
Or1200	15K	30M	123s	13M	1h57m

V. SUMMARY AND CONCLUSION

We presented a novel method to improve the EM robustness of layouts. With our approach, temperature and stress results are effectively calculated and widely considered within the placement and routing steps. To achieve this, we proposed algorithms to discretize placement and interconnect solutions, which can be used within a placement or routing tool.

Our approach is the first to show how to perform most of the analysis steps within placement and routing tools. In addition, we describe how EM results can be effectively achieved and considered in these tools. Our methodology has the advantage of being fast, accurate and flexible due to the separation of discretization and solving strategies. Fast and accurate, because our developed discretization algorithms are specialized to layout structures; thus generating relatively few elements. Flexible, because the discretization step is independent of the solving process; thus enabling the use of any solver in the background. The simulation results show that we are able to find less EM critical cell locations in the placement step and robust interconnect structures in the routing step.

We believe that our EM-aware synthesis will become highly important in the near future due to increasing reliability concerns. Our approach is the starting point for future work on EM-aware synthesis to increase EM robustness of a layout.

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