

Load-Aware Redundant Via Insertion for Electromigration Avoidance

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ABSTRACT

The ongoing shrinking of interconnects in integrated circuits (ICs) induces reliability issues caused by electromigration (EM), including void-induced failure mechanisms in IC vias. We propose a new post-routing approach to insert redundant vias specially targeted for EM avoidance. Our algorithm compares all possible insertions and utilizes the configuration with the highest reliability gain. This is achieved by considering the connecting segment loads. These loads are an estimation of the risk involved in creating EM-induced voids as a continuous function of current density, segment length and stress development over time. Inserting vias in those segments with highest loads, our approach efficiently increases circuit reliability by reducing EM effects. We were able to reduce the total, average and maximum via load for the MCNC benchmark suite on average by 6.6%, 4% and 13.9%, respectively. The increase in via reliability was confirmed by subsequent modeling of EM-inducing factors.

Keywords

Electronic design automation; physical design; reliability; redundancy; electromigration; post-routing redundant via insertion; layout

1. INTRODUCTION

As the downscaling of integrated circuits (ICs) continuously decreases IC structures, reliability issues due to interconnect and via failures gain more and more influence. Particularly, vias are critical elements in a design [18]. This is due to the influence of material transport caused by electromigration (EM) which is higher in via regions than in interconnects due to the smaller cross-sectional area.

Via failures can also be introduced by the manufacturing process or by thermally induced stress. Nevertheless, EM is the primary cause of via failure during an IC lifetime, since manufacturing defects can be detected by design-for-

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ISPD'16, April 03-06, 2016, Santa Rosa, CA, USA

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ACM ISBN 978-1-4503-4039-7/16/04.

DOI: <http://dx.doi.org/10.1145/2872334.2872355>

Please quote as follows:

S. Bigalke and J. Lienig. Load-aware redundant via insertion for electromigration avoidance. In *Proc. of the 2016 ACM International Symposium on Physical Design (ISPD)*, pages 99–106, Apr. 2016. DOI: 10.1145/2872334.2872355.

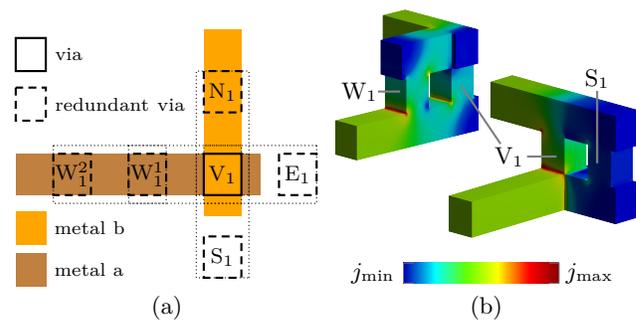


Figure 1: (a) Candidate positions for redundant vias to the north (N_1), south (S_1), east (E_1) and west (W_1, W_2) of the (original) via (V_1). (b) Two different via insertions with on-track via W_1 distributing the current density (j) better than off-track via S_1 .

test structures and thermally introduced stress has been mainly identified on bigger structures such as through silicon vias (TSVs) or packaging elements.

EM is a material dislocation caused by the momentum transfer of moving electrons to steady lattice metal ions at the moment of collision. Therefore, one of the main factors of influence is the current density (j). The International Technology Roadmap for Semiconductors (ITRS) [9] predicts a rise in current density, since interconnects and vias are shrinking at a higher rate than the reduction in current consumption in active silicon elements [9]. Hence, in the near future almost every net, including signal nets, will be affected by EM. The IC industry is facing a lack of EM solutions from, and including, 5 nm technology nodes and beyond [9][18].

Redundant vias, as shown in Fig. 1, not only increase yield but also extend chip lifetime [1]. The manufacturing process introduces voids between metal and via layers, which can be starting points for a via failure induced by EM. Figure 2a shows that voids in via areas predominantly occur at the interface of via trenches and interconnects. These defects can also grow through the entire interconnect (Fig. 2b). If a redundant via is inserted next to a failing via, then chip lifetime is extended since EM must deplete two or more via areas before this net segment fails. Here (as in other papers), a *segment* is defined as a single part of a net, which is located only in one metal layer and enclosed by a diffusion barrier.

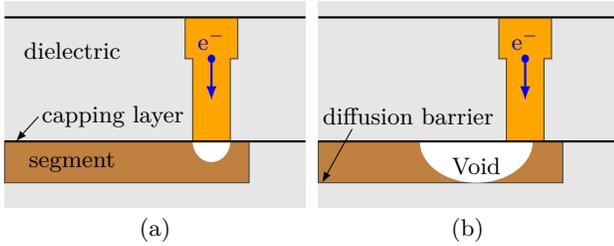


Figure 2: A void formation directly underneath the via trench is shown in (a), while (b) depicts a void growth through the entire interconnect.

This paper presents a novel, post-routing redundant via insertion process. It is based on combining EM-inducing factors into a *load* metric. Here, a *segment load* represents the risk of void creation in a particular segment based on current density, segment length and resulting time-dependent stress development. A *load per via* is defined as the highest segment load of the via-connected segments divided by the number of vias used to establish this particular connection. In our opinion, these parameters determine the reliability gain with each redundant via.

To the best of our knowledge, this is the first algorithm that optimizes the (local) redundant via insertion in order to minimize the (global) sum of all “loads per via” in the design (*total via load*).

Our paper is structured as follows. After outlining the current via insertion algorithms in Sec. II, we demonstrate the necessity for their extension in Sec. III. Section IV describes such a comprehensive via insertion procedure and Sec. V presents our experimental results.

2. PREVIOUS WORKS

Redundant via insertion can be applied as part of the routing step or as an additional post-routing optimization with the latter being the main focus in physical design. Nevertheless, redundant via insertion while routing has been investigated as well, such as in [5][19][24].

Post-routing redundant via insertion was first presented and utilized in EYE/PEYE [1]. In general, the redundant via insertion subject can be formulated as maximum bipartite matching (MBM) or maximum independent set (MIS).

The MBM approach was investigated in [26] and adapted to timing constraints in [25] and [22]. Lei et al. extended the MBM problem in [16] to a maximum-weighted bipartite matching (MWBM) (includes candidate dependencies and weights) and solved it by using an efficient heuristic minimum weighted matching algorithm. In [15] the MWBM approach is particularly used to insert aligned stacked vias in a grid-based layout with up to three metal layers. Later on, Chang et al. [4] introduced a new rectangle via candidate, which occupies a smaller footprint than a two via compound while it still prolongs via lifetime.

MBM is generally less time consuming than MIS but it cannot always determine the optimal solution [13]. Therefore, our algorithm is based on MIS.

MIS was first applied to the redundant via insertion problem in [13]. Here, all feasible redundant via candidates are simultaneously examined which improves the solution quality. In [14] the same author introduced a zero-one integer linear programming (0-1 ILP) algorithm to solve the MIS problem. Since finding the solution of this can be NP-complete,

Lee et al. proposed in [11] speed-up techniques to reduce the problem size and enabled the consideration of via density constraints. In [12] the approach has been extended by weights to consider on-track vias or non-wire bending redundant via candidates.

Pak et al. in [21] were the first to apply the MIS approach for EM-aware redundant via insertion. The authors presented a two-phase algorithm, which first determines only feasible redundant vias based on current density, before inserting as many as possible additional vias. However, their approach lacks the consideration of segment length and time-dependent stress, which greatly influence EM-induced via failures.

3. PROBLEM DEFINITION

3.1 Electromigration

EM is a material transport caused by the momentum transfer of moving electrons to metal ions. The metal ions break out of their lattice and begin to move towards the anode. The amount of dislocated material over time depends on the current density and therefore also on current and cross sections of each net segment. Not only does the cross-section geometry matter but also the length of a segment. Next to current density and segment geometry, EM also depends on the temperature, the material and the manufacturing process [17]. These three factors are excluded from our study, since they are given parameters for physical design.

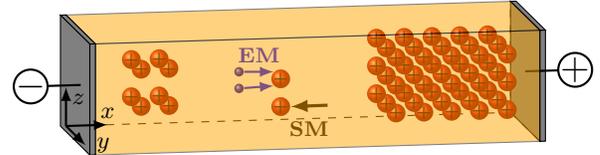


Figure 3: Metal ion transportation from cathode towards anode due to EM, resulting in tensile stress at the cathode and compressive stress at the anode. The stress gradient causes SM which compensates EM and results in a balanced state [8].

The current density and segment geometry essentially influence the build up of the time-dependent stress along a segment. As Fig. 3 depicts, the dislocated metal ions build up tensile stress at the cathode and compressive stress at the anode. This is mathematically expressed by:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[\frac{D_a B \Omega}{kT} \left(\frac{\partial \sigma}{\partial x} - \frac{|Z^*| e \rho j}{\Omega} \right) \right], \quad (1)$$

where σ is the stress, D_a the self-diffusion coefficient, B the applicable modulus, Ω the atomic volumes, kT the thermal energy, $|Z^*|$ the effective charge number, e the elementary charge, ρ the electrical resistivity and j the current density [10].

The exemplary one-dimensional solution of Eq. (1) along the x -axis is plotted in Fig. 4 for a $50 \mu\text{m}$ long segment and a current density of 1 MA m^{-2} . The plot shows the stress increase over time until EM is compensated by stress migration (SM, red straight line). From this moment on, the absolute maximal stress (σ_{max}) is reached on both segments ends. We should point out that the tensile stress at the cathode is more critical than the compressive stress at the anode because the critical stress (σ_{crit}) for void creation is usually lower than the threshold for hillock building.

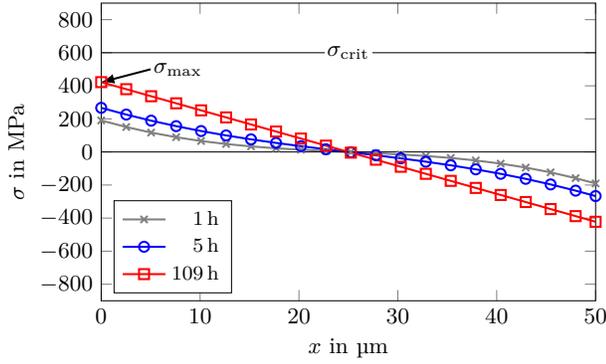


Figure 4: One-dimensional stress development over time, based on a current density of 1 MA m^{-2} and a segment length of $50 \mu\text{m}$.

The void formation starts with the depletion process until the stress oversteps the critical stress. Equation 1 must be solved to determine the void depletion time (when the stress reaches the critical stress). From this point on, the void starts to grow and the interconnect resistance starts to significantly increase till a chip failure is detected due to a voltage drop that is too great, or an open circuit.

If the stress development is stable over time, the steady state is reached and EM is balanced by SM. In 1975 *Blech* found that an interconnect segment is immortal to EM if the maximal stress is lower than the critical stress [2]. The so called Blech-length effect connects current density and segment length to the time-dependent stress:

$$jl \leq (jl)_{\text{crit}} = \frac{\Omega \sigma_{\text{crit}}}{|Z^*| e \rho}. \quad (2)$$

Equation (2) shows that the higher the product of current density and segment length, the higher the risk of EM failure.

As a consequence, an EM-robust redundant via insertion process should not only consider current density, but also segment length. The following sections explain in detail why current density, segment length and time-dependent stress must be considered in order to prevent EM-induced via failures.

3.2 Influence of Current Density

A segment's current density is the main driving force behind EM. As shown in [12], on-track vias facilitate a more balanced current distribution and enable a shorter wire length than off-track vias. Even though the approach in [21] states that off-track triple via configurations can have a 2% longer lifetime than on-track configurations, we recommend balancing and reducing current densities per via.

A reason to prefer on-track to off-track vias is shown in Fig. 5. An unbalanced current density per via can easily lead to a void, which grows through the segment (compare Fig. 2b). The reason for this is the increase in current density under void V_1 . While the void is growing underneath the via trench, the current density is rising in the region underneath the void (red zone). Therefore, EM is continuously increasing to move material out of this area until the increase in resistance leads to a chip failure. This might happen even before the redundant via fails.

As mentioned, the higher the current density, the more stress builds up and therefore the more likely the segment is to fail (Fig. 6).

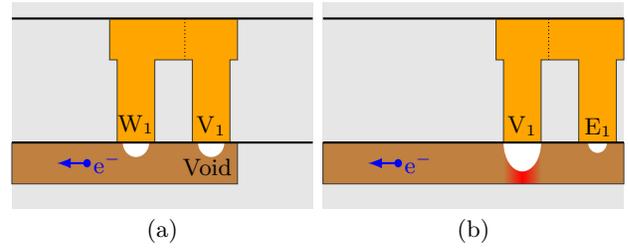


Figure 5: Systematic void growth in on- and off-track vias. Figure (a) depicts uniform void growth under the via and the redundant via. Figure (b) shows the increased current density in the red area underneath the via (V), which continues to grow until an interconnect failure occurs.

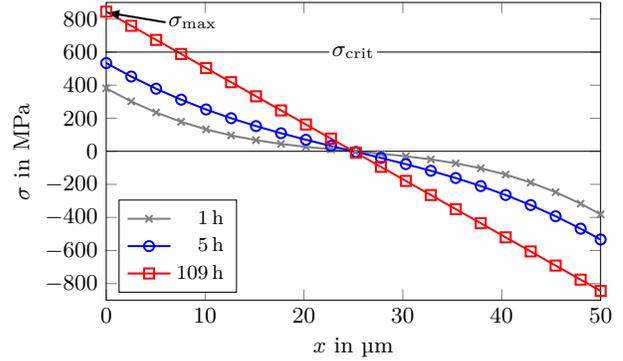


Figure 6: One-dimensional stress development over time, based on a current density of 2 MA m^{-2} and a segment length of $50 \mu\text{m}$ (compare with Fig. 4).

Comparing Figs. 4 and 6, we can see that while the time to reach steady state does not depend on the current density, the time to reach a certain level of stress does. The general rule is that the higher the current density, the faster the stress builds up.

Current density thus impacts the segment load and should be considered when evaluating the importance of a redundant via in a segment. To the best of our knowledge, current densities have never been used to directly rank redundant via candidates.

To lend credence to our recommendation to compare current densities in different segments, we constructed the “academic example” in Fig. 7a. Here, there is only one redundant via location for an insertion in either net 1 or net 2. (By definition, a *via location* is a connection of two metal segments on different layers at a single position in the design.) In Fig. 7a, the net of via 2 carries twice as much current as the net of via 1. Again, as far as we are aware, all published redundant via insertion algorithms solve this conflict randomly if both segments are EM critical or EM stable.

If we compare the current density distribution of both vias without insertion (Fig. 7b), we can clearly see that via 2 carries a higher current density than via 1. Therefore, the redundant via W_2 (Fig. 7d) balances the current density distribution per via better than a redundant via E_1 (Fig. 7c). This example illustrates that the commonly applied goal of “as many as possible” redundant vias is not detailed enough for an EM-robust redundant via insertion process.

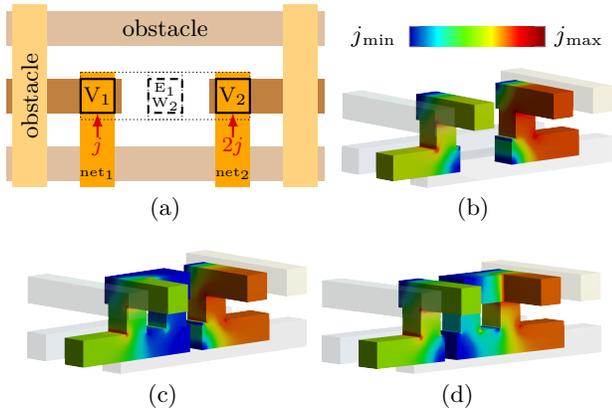


Figure 7: (a) Layout with only one redundant via location which qualifies for an insertion in either net 1 or net 2. Figure (b) shows the current density distribution without insertions. Figures (c) and (d) depict the current density distribution after an insertion in net 1 and net 2, respectively. Here, configuration (d) balances the current density best and therefore gains reliability.

3.3 Influence of Segment Length

In this section we show that not only current density but also segment length should be considered. Therefore, we expand our previous example in Fig. 7a to the example in Fig. 8. Here, the segment lengths are added to show their influence.

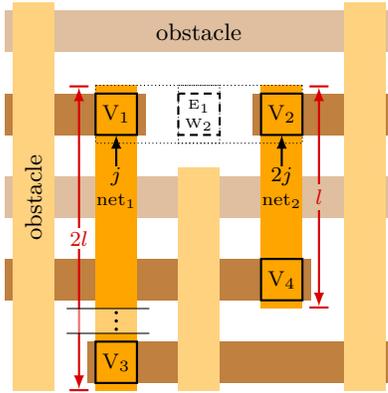


Figure 8: Extended layout example of Fig. 7 to illustrate the influence of segment length on EM. Please note that the distance between via 1 and 3 is twice as long as the distance between via 2 and 4. However, the current density between via 1 and 3 is only half the value of that between via 2 and 4.

The subsequently derived stress development in Fig. 9 demonstrates that the product of current density and segment length is not sufficient to fully describe the influence of stress induced by EM. This product is the same in both segments. Therefore, the maximum stress is also the same after it reaches the steady state condition for EM and SM. Nevertheless, in this configuration the redundant via should be inserted next to V2 since Fig. 9 shows that the critical stress is reached about five times faster at this via than it is at the other one. This means that a void underneath via 2 depletes about five times faster than a void under via 1.

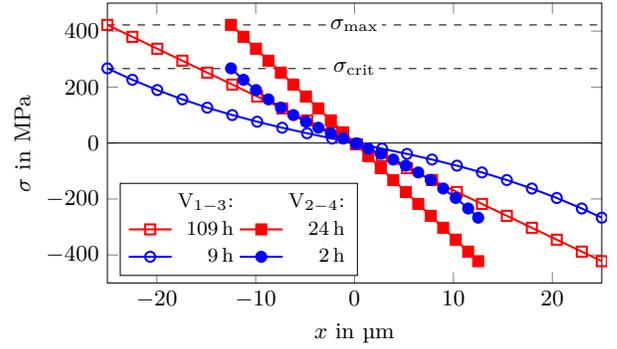


Figure 9: Comparison of one dimensional stress development over time, based on a $j_{1,3} = 1 \text{ MA m}^{-2}$, $l_{1,3} = 50 \mu\text{m}$, $j_{2,4} = 2 \text{ MA m}^{-2}$ and $l_{2,4} = 25 \mu\text{m}$.

3.4 Segment Load

We recommend that an EM-aware redundant via insertion process should consider: (1) current density, (2) segment length, and (3) time-dependent development of stress. These three EM-inducing factors are subsequently labeled as segment load. (Please refer to Eq. (3) for their mutual relationship). With these factors, we can not only estimate whether a segment is EM critical or EM stable but we can also estimate and compare the reliability gain of each via insertion.

The term “EM critical” means that the segment stress exceeds the critical stress. EM stable segments are (in theory) immortal against EM because the segment stress is lower than the critical stress. In reality, however, the manufacturing process induces defects, which are starting points for void creation. Therefore, we should also insert redundant vias in EM stable segments but only if there are no other redundant via candidates with higher segment loads that could also use this location. In summary, the insertion of redundant vias must be based on the connecting segment loads.

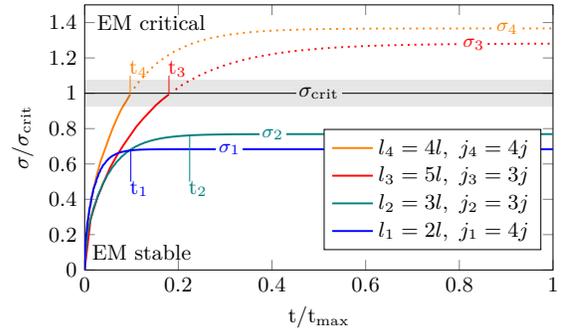


Figure 10: Time dependent stress development for different current densities and segment length combinations ($j = 1 \text{ MA cm}^{-2}$ and $l = 1 \mu\text{m}$). Segments 1 and 2 are EM stable since their maximum segment stresses are lower than the critical stress. Consequently, segments 3 and 4 are EM critical.

Figure 10 plots four different combinations of current densities and segment lengths. Please note that the critical stress threshold is blurred by manufacturing variances. Two of the segments are EM stable and two are EM critical. The plot shows that we have to calculate all load factors for each current density and length combination because void depletion time and maximum stress do not correlate.

4. LOAD-AWARE VIA INSERTION PROCEDURE

4.1 Flow Sequence

This section describes the main steps in our approach. Net capacities and currents, both determining the segment loads, are input values of our algorithm. Furthermore, technology information is needed as a constraint while searching for redundant via locations. The latter are represented in a conflict graph including geometric dependencies between the redundant via candidates. Finally, these conflicts are transformed into a 0-1 ILP problem which allows us to find the *optimal* redundant via insertions with regard to EM effects.

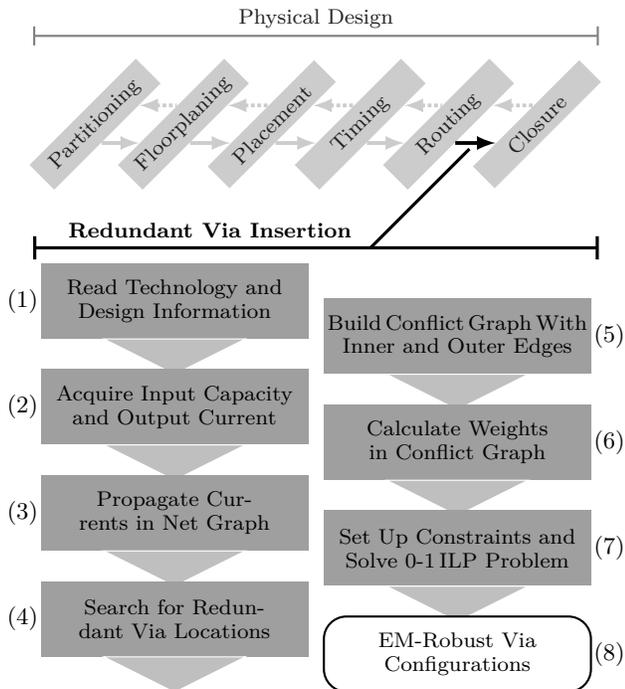


Figure 11: Main steps in our algorithm for load-aware redundant via insertion. These steps are fleshed out in Sec. 4.1 (Step 1) to (Step 8).

Step 1: Read Technology and Design Information

The first step is to read the technology and design information which are commonly provided in the Layout and Design Exchange Format (LEF/DEF). Our approach requires technology information such as interconnect space, width and height in each layer. The design information include the routing result and possible via configurations.

Step 2: Acquire Input Capacity and Output Current

Next, the net currents, based on net topology and input pin capacitances, are determined. Pins in standard cells are usually characterized in a look-up library file (.lib) which contains the information about current characteristic and pin capacitance. Our approach assigns to each input net pin the appropriate capacitance and determines the current values based on the waveform and switching activity.

Step 3: Propagate Currents in Net Graph

We model the current flow starting from the net output pin and heading towards the input pins. Therefore, we transform the interconnect segments for each net into a current flow graph. This graph representation contains a vertex for each net segment and edges between connecting segments as shown in Fig. 12.

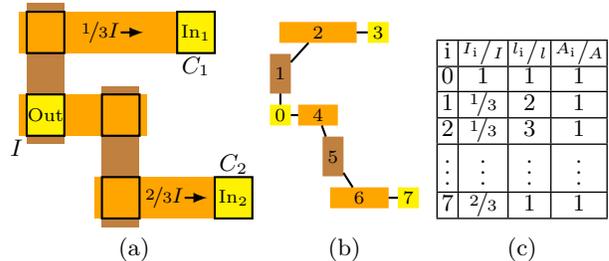


Figure 12: (a) Net transformation into a graph representation. (b) Propagation of currents along segment connections. (c) Vertex properties including segment length (l), current (I) and cross section (A).

Circuit analyses have shown that, in a first approximation, the current in each path between output and input pins can be divided as per the ratios of the different path capacitances to the total net capacitance. To determine the shortest path between output and input pins in the current flow graph, we execute the Dijkstra algorithm [6] starting at the output. After that, the different paths are obtained by backtracking from the inputs pins. The currents for all identified segments on each path are added up to the total segment current. From now on, each segment contains its current, length and cross-section information, so that the current density value can be calculated.

All previous steps must be finished before executing the next step, searching for redundant via locations.

Step 4: Search for Redundant Via Locations

This step detects all possible locations in the design which can serve as redundant via locations (Fig. 13).

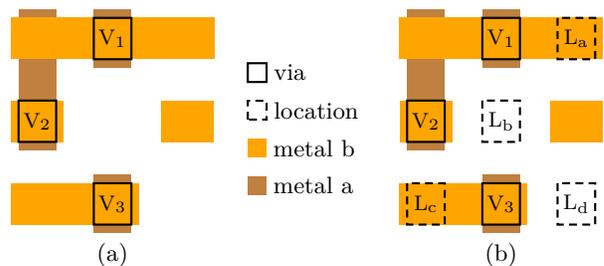


Figure 13: (a) Design example with vacant space after routing. (b) Redundant via locations in accordance with the design rules.

The following conditions must be fulfilled to ensure a location is suitable for a redundant via:

- Inserting a redundant via must not violate any spacing rules to existing interconnects, and
- the redundant via candidate can only intersect with its own net.

Step 5: Build Conflict Graph With Inner & Outer Edges

Each via location, identified in the previous step, is tested by the adjacent vias to check if it can serve as a redundant via location. If one or more redundant vias can be inserted, candidates are found and a vertex is added for each candidate to a conflict graph (Fig. 14). Various redundant via candidates which occupy the same location are defined as “in conflict”.

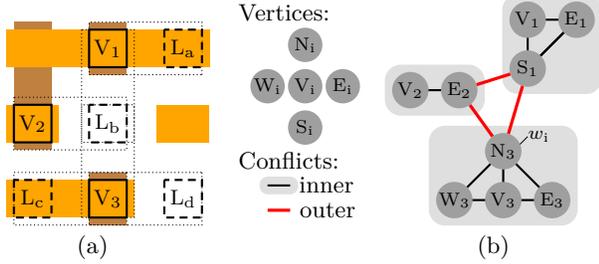


Figure 14: (a) Geometric intersections of redundant via candidates. (b) Transformation of geometry information into a conflict graph with internal and external edges. Internal edges link redundant via candidates of the same via location. External edges represent conflicts of redundant via candidates from different via locations.

The geometric intersections of these candidates are transferred into edges in the conflict graph. We distinguish between inner and outer conflicts (edges), as it was done in [21]. Inner edges are added between all possible redundant via candidates of the same via location. Outer edges are inserted to the conflict graph between redundant via candidates from different via locations.

Step 6: Calculate Weights in Conflict Graph

A very essential step in our approach is to assign weights to every vertex in the conflict graph. These values are crucial for rating the conflicting via candidates and inserting the most fitting candidate. In our approach, a *weight* is the previously defined load per via. As mentioned, the sum of all load per vias (weights) in a design is called total via load (z). The global objective is to minimize the total via load in the design.

As discussed in Sec. 3.4, current density, segment length, maximal stress and the time to reach the critical stress influence the segment load. The first two parameters are input values; the time-dependent stress is determined by Eq. (1).

A segment load consists of two main load factors representing void depletion (t_{\min}/t_i) and void growth ($(j^l)_i/(j^l)_{\max}$) phases, respectively. Both ranges are standardized to ensure a value between zero and one. Additionally, these values are adjusted by the linear scaling factors: α and β .

The factor of void depletion is a measure of time t_i at which the segment resistance starts to increase considerably. The longer it takes, the more robust the segment is. Therefore, the individual depletion time of the investigated segment is reciprocal standardized to the minimal depletion time of all segments in the design.

The factor of void growth is represented by the product of current density (j) and segment length (l). The higher the product, the faster the void grows. This product is also proportional to the maximum segment stress and standardized by the maximum occurring value.

The sum of both scaled segment load factors is finally divided by the number of vias each vertex utilizes. This means that a segment load is divided by one for a single via, by two for a double via, and so on. The load per via is based on the highest segment load of the connecting segments. The equation to calculate a weight (w_i) is formulated as follows:

$$w_i = \frac{\left(\alpha \frac{t_{\min}}{t_i} + \beta \frac{(j^l)_i}{(j^l)_{\max}}\right)}{n_i} \Rightarrow \frac{\text{load}}{\#\text{via}}, \quad (3)$$

where α was determined empirically to be 1 and β to be 2. (We value the influence of void growth speed more than depletion time). This assumption holds for today’s copper interconnects manufactured by the dual-damascene process.

Additionally, we adjust t_i for EM stable and EM critical segments depending on the maximum segment stress. In an EM stable segment, the maximum stress does not exceed the critical void stress and therefore the depletion time is set to infinity and the depletion factor becomes zero. Note that the void growth factor for an EM critical segment is always higher than the factor for an EM stable segment. Consequently, our algorithm focuses on redundant via insertion in EM critical segments.

$$t_i = \begin{cases} \infty & \sigma_{\max} < \sigma_{\text{crit}} \quad (\text{EM stable}) \\ t_{i, \text{crit}} & \sigma_{\max} \geq \sigma_{\text{crit}} \quad (\text{EM critical}) \end{cases} \quad (4)$$

Since our weight function is length dependent, our approach prefers on-track vias to off-track vias and non-wire bending candidates to wire bending candidates. Off-track and wire bending candidates prolong the segment length which is directly reflected in an increase in segment load.

Step 7: Set Up Constraints and Solve 0-1 ILP Problem

Having created the conflict graph, our approach transforms the vertex weights and edges into a 0-1 ILP problem to determine the optimal solution. (Our weight function can also be used in a MWBM problem formulation, because it is generally applicable.) As mentioned before, the objective function is to minimize the total via load (sum of all weights) in the design which can be expressed as:

$$\text{minimize: } z = \sum_{i \in V} w_i v_i, \quad v_i \in \{0, 1\}, \quad (5)$$

where V , IE and OE represent vertices, and inner and outer edges in the conflict graph ($G = (V, IE, OE)$), respectively. It should be noted that v_i can only be one or zero, which means this vertex is or is not taken, respectively.

The conflict graph edges are transformed as constraints which must be fulfilled. Inner edges represent a minimum of candidates to be taken and can be modeled as:

$$\sum_{j \in IE} v_j \geq 1, \quad (6)$$

which ensures that at least one configuration is included in the final design.

Outer edges represent vertex intersections. This means that only one vertex can be chosen in the final solution:

$$v_i + v_j \leq 1, \quad \forall i, j \in OE. \quad (7)$$

4.2 EM-Robust Via Configurations

Our approach reduces the total, average and maximum via load in the design because we utilize redundant via candidates with the lowest load per via if multiple choices exist. The general principle is: the higher the segment load, the more important it is to insert redundant vias in order to lower the load per via.

Illustrating this principle in Fig. 8 means that the location is taken by a redundant via in the west of via 2 belonging to net 2. The load of via 2 is higher than the load of via 1, because the segment load of net 2 is higher than the segment load of net 1 and the number of vias are the same. The segment load in net 2 is higher than the segment load in net 1, because segment 2 depletes faster than segment 1. In order to minimize the total via load, the optimal EM-robust solution is to divide the high segment load of net 2 by two vias and to retain the single via in net 1.

5. EXPERIMENTAL RESULTS

To verify our load-aware redundant via insertion for EM avoidance, we implemented our approach in C++ and applied it on the MCNC benchmark from [5], which is widely used in this research field. The details are subsequently explained based on the flow sequence depicted in Fig. 11:

- Step (1) uses the LEF/DEF parser from *Si2* [23] to read in the benchmarks.
- Step (2) requires the standard cell characterization. Unfortunately, the benchmark suite does not provide these look-up tables for output current characteristics and capacitance values. To overcome this issue, we used the open cell library files provided by *NanGate* [20] and mapped these standard cell values randomly to the cell pins of the MCNC benchmark suite. Since the technology dimensions of the MCNC benchmark suite are bigger than the *NanGate* 45 nm dimensions, we reasonably scale these values to achieve a comparable result.
- Step (3) utilizes a *boost* adjacency list [3] to represent the undirected current flow net graph.
- Step (4) fills a *boost* r-tree [3] with all interconnect elements and queries around each via. The query box measures the bounding box of the redundant via candidate plus the minimum layer space.
- Step (5) also represents all via candidates in an undirected graph as *boost* adjacency list [3].
- Step (6) reads in pre-calculated look-up tables to determine the maximal stress and time to reach the critical stress from current density and segment length. These look-up tables are generated by a *Python* script which solves Eq. (1) for multiple current density and segment length combinations.
- Step (7) employs the *Gurobi* library [7] to formulate and solve the 0-1 ILP representation. We also use the independent component computation from [21] to speed up the process.
- Step (8) replaces the vias in the original input DEF file and creates a new output file of the configuration which utilizes a minimum total via load in the design.

For the MCNC benchmark suite, we limited our load-aware redundant via insertion to single and double vias because the original technology contains only these via configurations.

Table 1: MCNC benchmark suite characteristics

Name	#nets	#layers	#segments	#vias
mcc1	802	4	6513	5948
mcc2	7118	4	36773	34376
primary1	904	3	7362	5536
primary2	3029	3	30088	23154
s5378	1694	3	10082	6739
s9234	1486	3	8638	5365
s13207	3781	3	22391	13972
s15850	4472	3	26527	16922
s38417	11309	3	65836	40942
s38584	14754	3	88368	55381
struct	1920	3	11719	7598

Table 2: Reduction of total, average and maximum via load in our designs compared to the designs from [5]

Name	Total via load		Red.: $\frac{\Delta \text{ via load}}{[5] \text{ via load}}$ in %		
	Design [5]	Our design	Total	Average	Maximum
mcc1	1147.1	1050.8	8.4	4.1	31.1
mcc2	6710.7	5978.7	10.9	5.2	4.5
primary1	446.9	436.4	2.4	1.5	19.8
primary2	1284.6	1255.5	2.3	0.7	0.1
s5378	554.1	509.1	8.1	5.2	21.1
s9234	477.0	441.1	7.5	4.9	15.4
s13207	903.9	837.7	7.3	4.7	0.2
s15850	1271.7	1168.1	8.1	5.3	28.2
s38417	2383.7	2192.6	8.0	5.5	11.3
s38584	2958.7	2703.5	8.6	5.8	9.9
struct	598.4	590.2	1.4	1.1	0.2

Table 1 depicts the number of nets, layers, segments, and vias for each benchmark.

All experiments were performed on a 3.4 Ghz Intel i7 Linux workstation with 8 GB of memory. Our implementation utilizes only one core but solving the biggest benchmark takes less than 2 min and requires about 200 MB of RAM.

Our evaluation is based on the total, average and maximum via load in the design according to Eq. (3). We compared our values to the original designs from [5].

Table 2 contains the total, average and maximum via load values of our and the original designs from [5], both based on Eq. (3). As shown, we were able to reduce the total, average and maximum via load on average by 6.6%, 4% and 13.9%, respectively. It should be mentioned that we achieved similar runtime and insertion rates while inserting redundant vias with the highest reliability gain.

We also modeled current densities in some via configurations prior to and after insertion. Figure 7(b,c,d) pictures an example where a marked reduction in peak current density within the vias can be observed. Our approach has also been evaluated by the reduction of via stress (Fig. 15).

6. SUMMARY AND CONCLUSIONS

We utilize the redundant via insertion process in order to make vias significantly more EM robust. This efficiently counteracts today’s increasing reliability issues due to technology downscaling.

We have shown that a comprehensive consideration of EM during redundant via insertion should not only consider current densities but also the segment length and the related time-dependent stress. We combined these EM-inducing factors into a “load per via” metric.

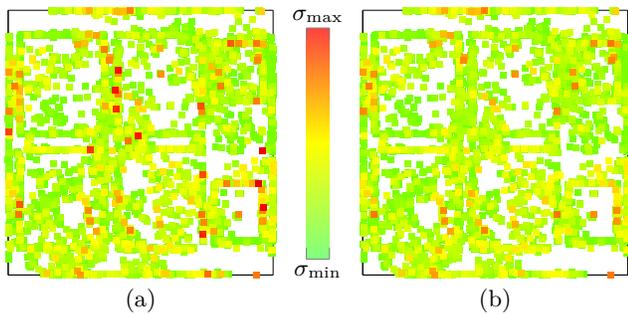


Figure 15: Via stress in the mcc1 benchmark before (a) and after (b) applying our approach. Numerical values range between 4.2% and 25% reduction in average and peak via stress, respectively.

To the best of our knowledge, this approach is the first that rates continuously all redundant via candidates based on their load per via. For this reason, we specially developed a weight function which determines the load per via representing the risk of void formation. This enables us to insert (local) redundant vias in order to minimize the (global) total via load in the design.

The verification of our approach on the MCNC benchmark suite showed a significant reduction in the total, maximum and average via load in a reasonable runtime. Subsequent modeling of current density and stress values within the vias verified this reduction. Our post-routing approach inserts load-aware redundant vias for EM avoidance during a single execution. It can also consider different kinds of vias, such as on- or off-track or multiple vias, as well as wire bending candidates.

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