An 8 bit to 12 bit Resolution Programmable 5 MSample/s Current Steering Digital-to-Analog Converter in a 22 nm FD-SOI CMOS Technology

Jeongwook Koh[1], Shishira S. Venkatesha[2], Sunil S. Rao[1], Marcel Jotschke[1], Jens Lienig[2], Torsten Reich[1]
[1] Fraunhofer Institute for Integrated Circuits IIS, Division Engineering of Adaptive Systems EAS, Dresden, Germany
[2] Dresden University of Technology, Dresden, Germany
e-mail: jeongwook.koh@eas.iis.fraunhofer.de

***Abstract*—We present a 5 MSample/s current steering digital-to-analog converter which has a programmable resolution between 8 bit, 10 bit and 12 bit. A selectable 2-D unary matrix architecture and a resolution programmable decoder are proposed for the resolution programmability. The proposed current steering digital-to-analog converter is implemented in a 22 nm FD-SOI (Fully Depleted Silicon-on-Insulator) CMOS technology. The simulation verifications of the CS-DAC at three resolution modes are made. The maximum DNL of 0.06 LSB is obtained at 8 bit resolution modes, and the maximum INL (Integral Non-Linearity) of 0.53 LSB is obtained at 12 bit resolution modes. The minimum SFDR (Spurious-Free Dynamic Range) of 47.93 dBc is obtained at 8 bit resolution mode.**

Keywords-component; current steering DAC, high resolution, resolution programmable, 5 MSample/s, 22nm FDSOI CMOS

I. INTRODUCTION

A digital-to-analog converter (DAC, D/A converter) is a device that converts digital signals to analog signals. DACs find many applications in various fields, for instance RF transmitters, audio amplifiers, video encoders and so on. Those are typical applications, where DACs are mainly used for a communication purpose. Otherwise DACs are used for a correction/calibration purpose. A sensor-actuator system is a typical example. A sensor collects analog information from the outside world and the information is converted to digital information by an analog-to-digital converter (ADC, A/D converter). A signal processor generates a correction/calibration signal for the DAC. The signal is converted by the DAC to corresponding analog signals, which drive an actuator for a better performance. Fields of applications including automotive, industrial and mobile device are good examples, where DAC needs to drive external actuator for correction/calibration purpose [1].

There are many different types of DAC architectures available. Examples are delta-sigma DAC (DS-DAC) [2], switched capacitor DAC (SC-DAC) [3], current steering DACs (CS-DAC) [4-11], [13], [15-16], which have been successfully developed to meet various application requirements. The CS-DACs have become effective solutions for the communication system applications, since they are fast, cost effective and have higher linearity [5]. The recent developments on the CS-DAC have been focused on the increase of the data-rate at a higher resolution of 10 or 12 bit. [8-11].

It is known from [6] that DACs in a sensor-actuator system do not need to have high-level performance in terms of speed, accuracy and linearity. Conversion speed of a few tens kilohertz and resolution of 6 to 8 bit are satisfactory in DACs for this application [6], [7]. DNL of less than 1 LSB (Least Significant Bit) is also good enough. In the case that a resistive actuator (load) needs to be driven, a DAC needs to have good output current driving capability. The CS-DAC is the most suitable architecture in this case, since it naturally provides current as an output variable. Especially, some sensor-actuator systems pose a challenge that the maximum output current needs to be correspondingly varied with a configurable resolution. This is a motivation of this work.

In this work, we present a resolution programmable CS-DAC that has the resolution programmability of 8 bit, 10 bit and 12 bit. A selectable 2-D unary-weighted matrix architecture and a resolution programmable decoder are proposed in the CS-DAC. The CS-DAC is designed to operate at three resolution modes at a data rate of 5 MSample/s in a 22 nm FD-SOI CMOS technology.

The outline of this paper is as follows. First, general design challenges of CS-DAC are identified in Section 2. In Section 3, the implementation issues of a resolution programmable CS-DAC are discussed and then we present a complete 8 bit to 12 bit resolution programmable CS-DAC. The simulation verifications of the CS-DAC at three resolution modes are presented in Section 4. The resolution programmability, the DNL (Differential Non-Linearity), the INL (Integral Non-Linearity) and the SFDR (Spurious-Free Dynamic Range) are simulated and analyzed. Finally, the conclusion of this work is made in Section 5.

II. CS-DAC DESIGN CHALLEGES

A. Architecture Considerations

Generally, three different CS-DAC architectures are popular which are the binary-weighted (BW), the unary-weighted (UW), and the segmented architecture [12]. In the BW architecture, the currents in current sources are binary-weighted and directly controlled by the number of N digital input codes. The BW architecture has area advantage based on its simplicity and smaller area-consumption. No decoding logic is necessary in the BW architecture. Otherwise, in the UW architecture, all current sources provide a unity current value and digital input codes need to be converted to thermometer codes in order to control switches in the UW architecture. The advantages of UW

Please cite as: J. Koh, S. S. Venkatesha, S. S. Rao, M. Jotschke, J. Lienig and T. Reich, "An 8 bit to 12 bit Resolution Programmable 5 MSample/s Current Steering Digital-to-Analog Converter in a 22 nm FD-SOI CMOS Technology," 2021 4th International Conference on Circuits, Systems and Simulation (ICCSS), 2021, pp. 102-107, doi: 10.1109/ICCSS51193.2021.9464215.

architecture are its good DNL error and the small dynamic switching errors, otherwise the BW architecture has a large DNL error and bigger dynamic errors [5]. However, the UW architecture has area penalty and more power consumption due to the enhanced complexity. A number of thermometer decoders are needed in the UW architecture [13].

The segmented architecture is a mixture of UW and BW architectures, where the advantages of both architecture are merged. MSBs (Most Significant Bits) conversion is realized using the UW architecture, while LSBs conversion is made by the BW architecture [14]. By an optimal segmentation, this architecture provides a good balance between static and dynamic performances with a reasonable complexity [13].

B. Segmentation Considerations

Most important factor for determination of a segmented level of a segmented architecture is "area optimization." Lin in [13] proposed an area optimization method for the best compromise between DNL and INL for a 10 bit CS-DAC. Figure 2 describes this graphical method for determining the segmentation level of the 10 bit CS-DAC, where an "Optimal Point" is found at 80 % segmentation level. This method is a good example to determination of a segmentation level of a high-resolution CS-DAC.

C. Mismatch Considerations

DNL is the worst-case deviation from an ideal one-LSB step between two subsequent input codes and INL is defined as the maximum deviation from a linear approximation to DAC real transfer function. Both INL and DNL are static nonlinearity specifications that determine the limit of DAC performance at a low frequency.

An important design concern with high resolution CS-DAC is to develop accurate current replicas of the current source for better INL and DNL. In real implementation of current replicas, inaccuracy due to random mismatch causes unavoidable accuracy degradation as described in (1) [15]. The random mismatch limits the static performances DNL and INL of DACs [5], [13].

$$\sigma^2_{I_D} = \frac{{A_\beta}^2}{W \cdot L} + \frac{4}{(V_{GS} - V_{TH})^2} \cdot \frac{{A_{VTH}}^2}{W \cdot L} \qquad (1)$$

In (1), A_{VTH} and A_β are mismatch constants that describe the variations of threshold voltage V_{TH} and the current factor β respectively.

III. Implementation of Resolution Programmable CS-DAC

A. Segmentation for Resolution Programmablity

The first step to design a resolution programmable CS-DAC is to determine how to configure segmentation levels. Table 1 illustrates the segmentation levels of three resolution (8 bit, 10 bit and 12 bit) in the CS-DAC. The resolution programmability is given to the unary-weighted part (MSBs), while the binary-weighted part (LSBs) remains unchanged at three resolution modes. In general, binary-to-thermometer decoders, unity current sources, MOS switches and digital logics like D Flip-Flops are necessary to the unary-weighted part. Those building blocks are designed to follow the resolution programmability rules which is shown in Table 1. In the segmentation level decision, three optimal points are found to meet the minimum chip-area and the same linearity performances at three different resolution modes. The proposed CS-DAC is designed to have DNL of 0.5 LSB and INL of 1 LSB at three different resolution modes.

TABLE I. Segmentation of the CS-DAC

Resolution [bit]	UW [bit]	BW [bit]	Segmentation [%]
8	4	4	50.0
10	6	4	60.0
12	8	4	66.7

B. 2-D Unary Martix for Resolution Programmablity

In a segmented CS-DAC, the most common problems are the arrangement of large number of current switching cells, distribution of data and clock to the respective cells. The 2-D matrix architecture in [15] is an elegant approach that arranges the switching cells in a compact way.

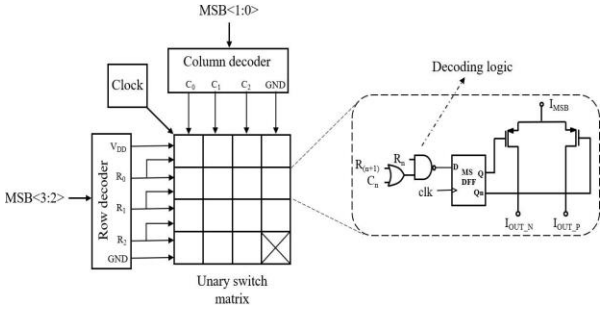

Figure 1. Example of 2D matrix architecture for 8bit resolution mode

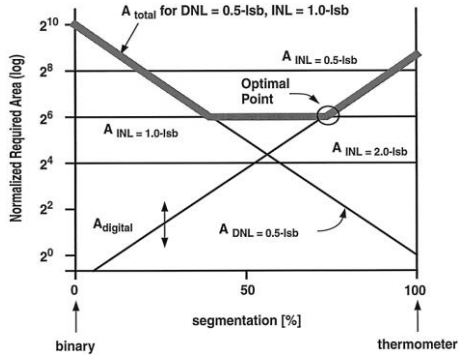

Figure 2. Normalized required area and segmentation levels from [8]

Figure 1 shows the 2-D unary matrix arrangement for 8 bit resolution mode. The 2-D unary matrix consists of a row decoder, a column decoder and 15 switch cells that corresponds to the number of unary switch cells from the segmentation. The switch cell consists of a decoding logic, a Master Slave D-Flip Flop and a PMOS switch pair. In Figure 1 the decoding logic senses the thermometer codes of two consecutive rows (R_{n+1}, R_n) and one column Cn and determines which switch in the differential pair should be

turned-on. The row decoder and column decoder are configured to have five outputs (VDD, R0, R1, R2 and GND) and four outputs (C0, C1, C2 and GND). The one extra output of the column decoder (VDD) is introduced for proper selection of a unary cell to be turned-on in the 2-D unary matrix.

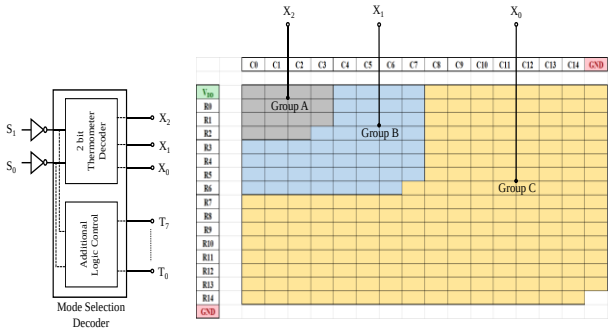

Figure 3. Conceptual view of the programmable 2-D unary matrix

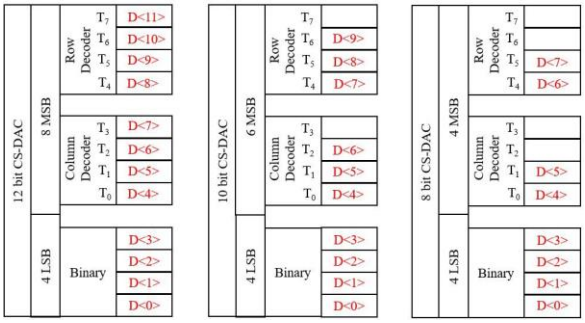

Figure 4. Proposed assignment of input digital codes

The resolution programmability is achieved by "grouping-selection" of the necessary unary cells in the 2-D unary matrix, where the grouping-selection is done by a resolution mode selector. Figure 3 illustrates how this grouping-selection works. A control signal from the resolution mode selector accomplishes the grouping-selection by turning off necessary cells according to a resolution setting. For example, when the CS-DAC sets for 10 bit resolution, the control signal X0 turns off all cells associated with group C. A 2-bit binary-to-thermometer decoder is used as the mode selection decoder in the implementation. The operation of the resolution selector is explained in Table 2 and Figure 4 shows digital signals assignment at three resolution modes.

TABLE II. LOGIC FOR RESOLUTION SCALABILITY IN 2-D UNARY MATRIX

Resolution [bit]	Selector		Control Signals			Segmentation [bit]	
	S1	S0	X2	X1	X0	Unary	Binary
8	0	1	0	1	1	4	4
10	1	0	0	0	1	6	4
12	1	1	0	0	0	8	4

C. Unity Current Source

The accuracy of CS-DAC current sources directly affects the static and dynamic performances of a CS-DAC [8]. In the implementation of the current source of the DAC, special cares are given to architecture choice and design methodology. A low-voltage high-swing SLVT (Super Low-VT) PMOS current source architecture is used (Figure 5). A mismatch-aware design has been made and verified by Monte-Carlo simulation (Figure 6). In the simulation, a standard deviation (1-sigma) of 54 nA is obtained. This is acceptable since the 3-sigma value of 162 nA is still below 0.5 LSB current (250nA).

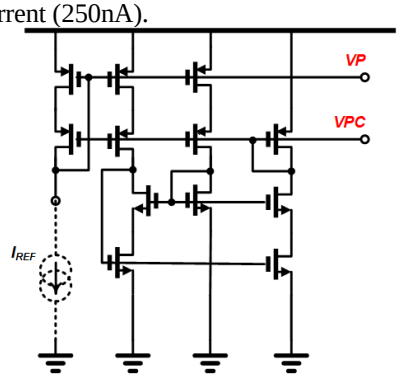

Figure 5. Unity current source. VP and VPC are used for current replica to unary and binary current elements.

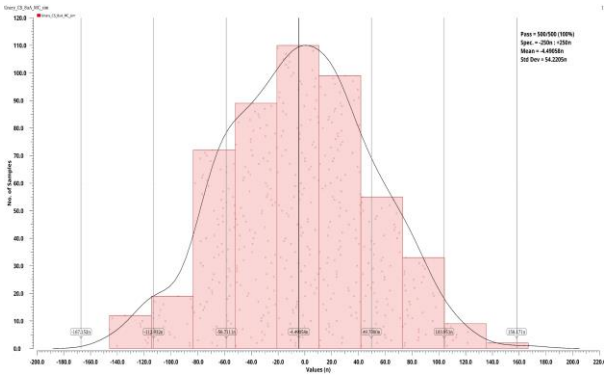

Figure 6. Monte-Carlo simulation result of the unary current source

Resolution programmability in the unity current sources is accomplished in a similar manner to the grouping selection of the 2-D unary matrix (Figure 3). In the implementation, gate-power down switches are introduced for the power-saving of the current sources which are not used at a certain resolution mode.

D. Completed Resolution Programmable CS-DAC

Figure 7 shows the completed resolution programmable CS-DAC. The CS-DAC has differential output currents and its outputs are terminated by load resistors for voltage conversion. A programmable 2-D unary matrix is implemented for the resolution programmability. The row and column binary-to-thermometer decoders of the 2-D unary matrix are designed to support 12 bit resolution mode and the resolution programmability is implemented as described in Section 3. Master-Slave D Flip-Flops (see Figure 1) are implemented for a better synchronization between the unary part and the binary part. The standard cells are used in the digital implementations of the CS-DAC.

The CS-DAC is designed to operate at three resolution modes (8 bit, 10 bit and 12 bit) with a conversion rate of 5 MSample/s in a 22 nm FD-SOI CMOS technology.

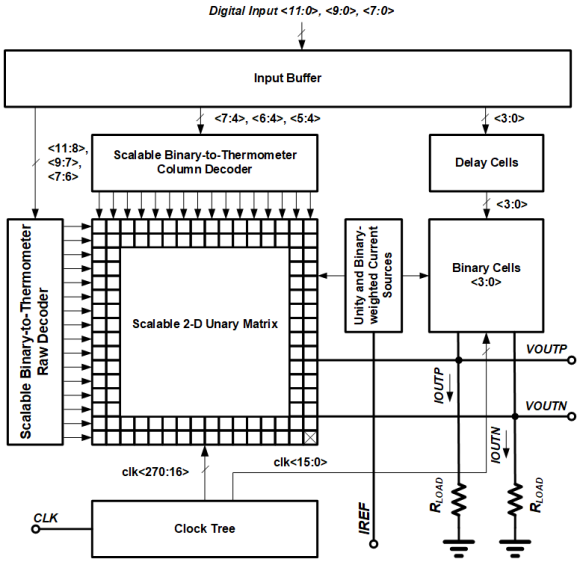

Figure 7. Proposed resolution programmable CS-DAC

IV. Design Results

In this section, the functionality and performance of the proposed CS-DAC is verified by simulations. The simulations have been performed using SPECTRE simulator of Cadence Design Systems [17].

A. Full-scale Output Current

For the verification of resolution scalability, the full-scale output currents of the CS-DAC at three resolutions modes (8 bit, 10 bit and 12 bit) are measured by simulation. Figure 9 shows the full-scale output current when the CS-DAC sets to have 8bit resolution. In the simulation, the differential currents I_{OUTP} and I_{OUTN} are plotted at load resistor R_{LOAD} of 250 Ω. The full-scale output current of 127.5 µA is obtained.

B. Static Performance

The static performances DNL and INL of the CS-DAC at three resolution modes are measured by SPECTRE simulations. In the simulation, digital codes for three resolution modes are generated using an ideal ADC using Verilog-A model [18]. Figure 8 plots DNL and INL of the CS-DAC at 8 bit resolution mode (left) and at 10 bit resolution mode (right). In both cases, the worst DNL happens at every code that makes all binary parts be zero. Odd symmetry is also observed in both cases, due to the differential operation of the CS-DAC. At 8 bit resolution mode, DNL of 0.06 LSB and INL of 0.04 LSB are obtained. DNL of 0.04 LSB and INL of 0.06 LSB are obtained at 10 bit resolution mode.

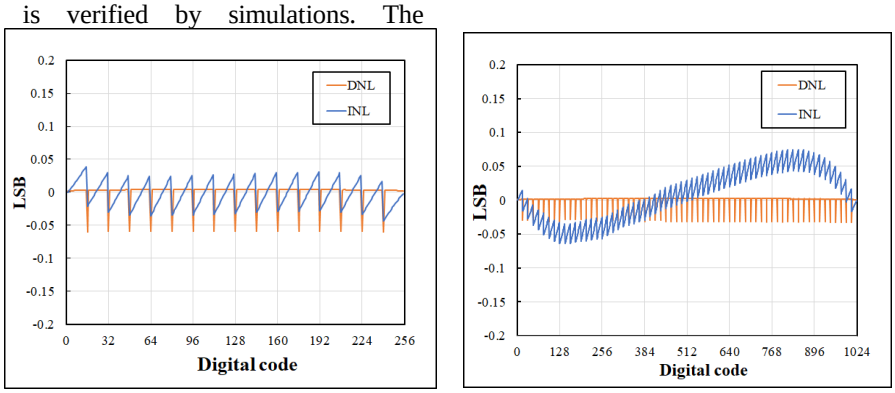

Figure 8. DNL & INL of the CS-DAC at 8 bit resolution mode (left) and at 10 bit resolution mode (right)

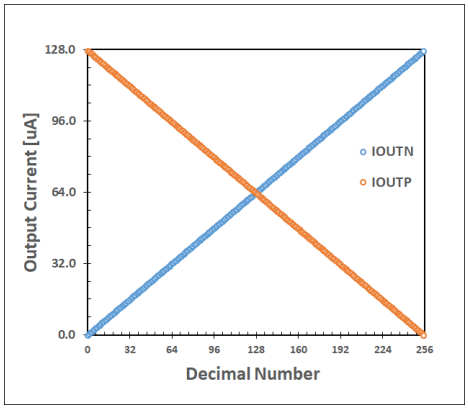

Figure 9. 8 bit full-scale output current of the CS-DAC

C. Dynamic Performamce

SFDR is selected for dynamic performance verification of the proposed CS-DAC. An ideal ADC using Verilog-A is used to generate the sinusoidal digital sequence to the CS-DAC, where the coherent sampling technique is used to evaluate the output spectrum [14], [17]. A sinusoidal signal with an amplitude of 400 mV is given to the SFDR measurement and the frequencies of input signals for three resolution modes are selected to follow coherent sampling condition for the simulations. Figure 10 shows the SFDR of the CS-DAC at 8 bit resolution mode (left) and 12 bit resolution mode (right). A fundamental at (556.41 kHz @ 8 bit resolution mode and 621.34 kHz @ 12 bit resolution mode) is observed and its third harmonic (1.699 MHz@8 bit

resolution mode and 1.864 MHz@12 bit resolution mode). 47.93 dBc for SFDR at 8 bit resolution mode and 52.49 dBc for SFDR at 12 bit resolution mode are obtained.

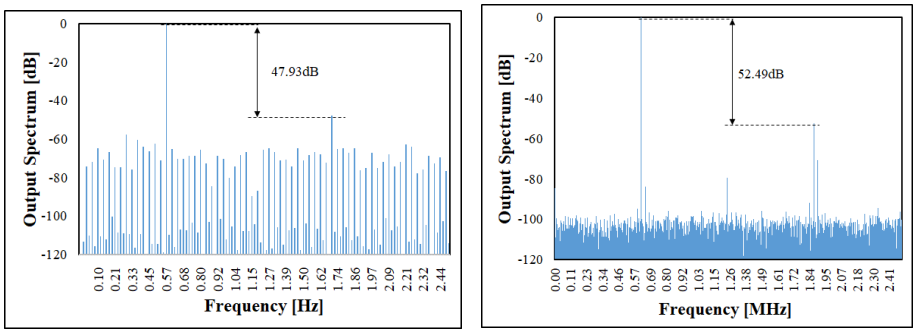

Figure 10. SFDR of the CS-DAC at 8 bit resolution (left) and at 12 bit resolution (right)

D. Performance Comparision

Performance comparison with recently published 8-bit [7], 10-bit [8] and 12-bit converters [9]-[11] is given in Table 3. The proposed CS-DAC has the maximum data rate of 5 MS/s, while the recently published 12-bit converters report the maximum data rates of a few hundred MSample/s. The CS-DAC targets for the sensor-actuator applications, where the speed requirement is much relaxed [6], [7]. Otherwise, the 12-bit converters mainly target for high speed applications in the communication systems, where the speed requirement is regarded as the highest priority. Thanks to the use of 0.8 V MOSFETs in a 22 nm FD-SOI process and the proper segmentation of the proposed CS-DAC, the CS-DAC shows the lowest power-saving in the comparison. The CS-DAC has 8 bit unary cells for the maximum resolution of 12-bit and the recently published 12-bit CS DACs have 8 to 7 bit unary-cells.

TABLE III. PERFORMANCE COMPARASIONS WITH OTHER CS-DAC

	This Work (simulation only)			**Ref. [7]**	**Ref. [8]**	**Ref. [9]**	**Ref. [10]**	**Ref [11]**
Year of Publication	2021			2012	2006	2005	2004	2001
Resolution [bit]	8	10	12	8	10	12	12	12
Segmentation[U:B]	4:4	6:4	8:4	6:2	0:10	8:4	7:5	7:5
Feature Size [nm]	22			350	180	90	180	350
Supply [V]	0.8			3.3	3.3	1.2	3.3	3.0
Rate [MS/s]	5			50	250	200	320	500
DNL [LSB]	0.06	0.04	0.05	0.04	0.1	0.2	0.3	0.25
INL [LSB]	0.04	0.06	0.53	0.025	0.1	0.85	0.4	0.35
SFDR [dBc]	47.93	73.94	52.49	50	60	56	60	62
Power [mW]	0.214	0.513	2.407	≤0.3	22	22	82	111

V. CONCLUSION

In this work we presented a 8 bit to 12 bit resolution programmable 5 MSample/s CS-DAC in a FDSOI CMOS 22 nm technology. As a first step, general design challenges and implementation issues of a resolution programmable CS-DAC are identified. In the implementation step, a selectable 2-D unary matrix and a resolution programmable decoder are proposed for the resolution programmability. The building blocks of the CS-DAC are implemented to have the resolution programmability. Especially mismatch-aware design has been made to the unity current source, where Monte-Carlo simulation is adopted for the verification.

For the verification of the resolution scalability, full-scale output current driving capability of the CS-DAC are presented. Static performances (DNL and INL) and dynamic performance (SFDR) of the CS-DAC are also presented for the performance verifications.

ACKNOWLEDGEMENT

This work has been funded within the project USeP under label 100317397 by the European Union and the Free State of Saxony as part of the European Regional Development Fund (ERFD).

REFERENCES

[1] Texas Instruments, Appl. Note, SNAA129, 2010

[2] P. Kiss, J. Arias, D. Li, and V. Boccuzzi, "Stable highorder delta–sigma digital-to-analog converters", IEEE Trans. on Circuits and Systems I, vol.51, No.1, Jan., pp. 200-205, 2004.

[3] Un-Ku Moon, J. Silva, J. Steensgaard, and G. C. Temes, "Switched-capacitor DAC with analogue mismatch correction", Electronics Letters, vol. 35, No. 22, Aug., pp. 1903-1904, 2002.

[4] W. Ni, X. Geng,Y. Shi, and F. Dai, “A 12-bit 300 MHz CMOS DAC for High-speed System Applications”, In Proc. IEEE International Symposium on Circuits and Systems 2006, pp. 1402-1405, 2006

[5] A. V. d. Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, “A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter”, IEEE J. Solid-State Circuits, vol. 36, no. 3, March, pp. 315 – 324, 2001.

[6] F. Maloberti, F. Tagliani, and G. Torelli, “Design of DAC-drivers for resistive actuators,” In Proc. IEEE International Symposium on Circuits and Systems, Sept., pp. 1713-1716, 1990

[7] G. Bertotti, A. Laifi, E. Di Gioia, “An 8 bit current steering DAC for offset compensation purposes in sensor arrays,” J. of Advances in Radio Science, Vol. 10, pp. 201–206, 2012

[8] Jurgen Deveugele and Michiel S. J. Steyaert, “A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC,” IEEE J. of Solid-State Circuits, Vol. 41, No. 2, pp. 320 - 329, 2006

[9] Takeshi Ueno, Takafumi Yamaji, and Tetsuro Itakura, “A 1.2-V, 12-bit, 200 MSample/s Current-Steering D/A Converter in 90-nm CMOS,” Proc. of IEEE Custom Integrated Circuits Conference, 2005

[10] Kevin O’Sullivan, Michael Hennessy, and Vincent Callaghan, “A 12-bit 320-MSample/s Current-Steering CMOS D/A Converter in 0.44 mm2,” IEEE J. of Solid-State Circuits, Vol. 39, No. 7.pp. 1064 – 1072, 2004

[11] A. Van Den Bosch;M. Borremans;M. Steyaert;W. Sansen, “A 12 b 500 MSample/s current-steering CMOS D/A converter,” Digest of Technical Papers, IEEE International Solid-State Circuits Conference, pp. 366 – 367, 2001

[12] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1998.

[13] C.-H. Lin, and K. Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6mm2,” IEEE J. of Solid-State Circuits, vol. 33, no.12, Dec., pp. 1948–1958, 1998.

[14] F. Maloberti, Data Converters, Dordrecht, Springer, 2008.

[15] M. J. M. Pelgrom, and A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching Properties of MOS Transistors,” IEEE J. Solid-State Circuits,vol. 24, no. 5, pp. 1433–1440, 1989.

[16] T. Miki, Y. Namkamura, M. Nakaya, S. Asai, Y. Akasaka, and Y. Horbia, “An 80-MHz 8-bit CMOS D/A Converter,” IEEE J. Solid-State Circuits, vol. 21, No. 6, pp. 983 – 986, 1986

[17] Cadence Design Systems, Spectre® Circuit Simulator Reference Product Version 19.1, 2020

[18] Cadence Design Systems, Cadence® Verilog®-AMS Language Reference, Product Version 5.5, 2005

Please cite as: J. Koh, S. S. Venkatesha, S. S. Rao, M. Jotschke, J. Lienig and T. Reich, "An 8 bit to 12 bit Resolution Programmable 5 MSample/s Current Steering Digital-to-Analog Converter in a 22 nm FD-SOI CMOS Technology," 2021 4th International Conference on Circuits, Systems and Simulation (ICCSS), 2021, pp. 102-107, doi: 10.1109/ICCSS51193.2021.9464215.