# Investigation of the Failure Mode Formation in BGA Components Subjected to JEDEC Drop Test

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**Abstract**

This paper is an investigation of the root causes for changing failure modes in different package types which are subjected to constant JEDEC drop test conditions. Drop test experiments applying memory BGA components show that there is more than one ultimate failure mode and that the failures created in the 2nd level interconnections are dependent on the package type. Thus the package geometry causes a redistribution of stress in the solder balls resulting in a stress concentration at the observed failure position. Stress analyses of the investigated packages are done by explicit finite element simulations in order to identify the significant stress distribution changes within the solder interconnections. These analyses prove different stress distributions resulting in the observed experimental failure modes. Additionally, these stress distributions justify the unexpected appearance of higher characteristic lifetimes for bigger packages.

## 1. Introduction

Electronic packages are more and more employed in mobile applications. Compared to classic electronic applications there are other critical load conditions, which may cause mechanical failures of the solder interconnections leading to a malfunction of these devices. In mobile applications electronic assemblies are subjected to high acceleration impulses caused by mistaken drops. The detailed effects of those drops on the solder joints are not completely understood, causing misinterpretations of the real drop performance of a new package.

The prediction of the characteristic lifetime of an electronic package subjected to drop loads is difficult because the severe stresses in the solder joints cause different failure mechanism. So far many researchers have presented their results of drop tests with varying failure modes between each investigation. But the acceptance of those experimental results is not sufficient. A precise knowledge of the failure mode formation in 2nd level interconnections is required in order to achieve substantial improvements of the lifetime characterization under these load conditions. This paper presents first insights into this topic by the application of the JEDEC drop test.

## 2. Experimental procedure

The investigation of the formation of different failure modes in BGA components is done applying the JEDEC drop test [1]. Among all mechanical tests the JEDEC drop test is the best suited method in order to investigate the characteristic behavior of components in terms of lifetime and failure formation due to its high reproducibility. This advantage is achieved by a guided impact of the specimen and reproducible drop impulses which result in similar PCB vibrations at each drop event.

The goal of this investigation is an analysis of the failure mode formation in 2nd level interconnections under drop test conditions. Since it is impossible to monitor the failure initiation in the solder balls during board vibration the root causes for different failure modes have to be analyzed by a combination of experimental observations and FEM simulations. For this purpose experiments have to get along with simple changes of components and experimental procedure in order to allow some easy comparisons with the simulations. That is why materials and their interfaces are kept constant for all package types since it is difficult to measure the mechanical behavior of their components under drop conditions. Thus only the different geometries of the packages have to result in changing failure modes.

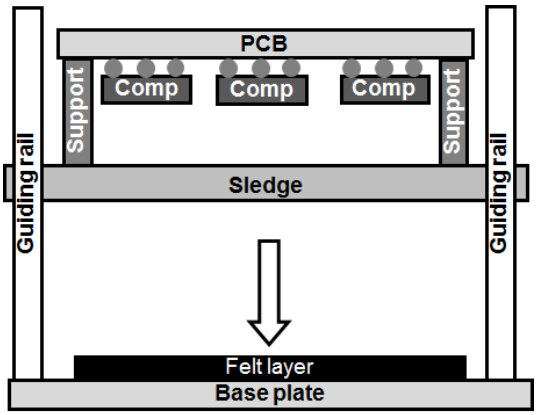


***Figure 1: Schematic representation of the JEDEC drop test***

Drop tests are executed applying the JEDEC drop condition `B` with a height of the drop impulse of 1500 *g* and a pulse duration of 0.5 ms. In contrast to the JEDEC standard the PCBs are fixed to the sledge at 6 positions by two additional supports in the middle of the long PCB edge [2,3]. This variation of the PCB´s degree of freedom changes the board vibration but it does not affect the

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ultimate failure modes of the package types. The JEDEC boards are equipped with all 15 daisy chain components which are monitored continuously by an event detector. Each board is subjected to 500 drops in order to create fails in at least 4 component positions. 6 boards are tested with each package type in order to validate a constant failure mode and derive the characteristic number of cycles to failure at different component positions. This way, solid and reliable results are gathered for the detailed simulation analyses.

The PCB vibrations caused by a drop impulse result in high mechanical stress within the BGA solder interconnections. As shown in figure 2, the high stress level and the alternating stress distribution are able to cause different failures which result in an ultimate interruption of the electrical connection [4]. Typical failures are IMC cracks [5] as well as broken copper traces to the PCB pads [6, 7]. Further optional failure modes are broken substrate pads [8] or failed solder balls [9]. However, a crack of the solder bulk represents a rather small stress level. Due to the complex and alternating stress distribution within the solder interconnection, finding the experimental failure formation and according FEM stress criteria is difficult.

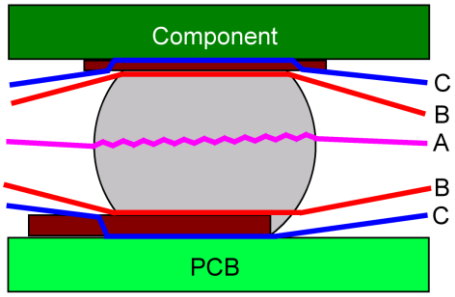


***Figure 2: Possible failure modes in a BGA solder ball. A: Solder crack; B: IMC crack; C: cracked copper pad***

The package types applied in this investigation are shown in figure 3. The test matrix includes 3 different types of daisy chain packages, which are designed for DRAM applications. As mentioned before, all packages are manufactured with equal materials for their components. Especially materials around the high stressed BGA interconnects are kept constant. The solder balls are SnAg1.0Cu0.5. The PCB side of the interconnections has n-SMD pads which are covered with Cu-OSP. All component copper pads are SMD with an electro-less nickel/gold finish.

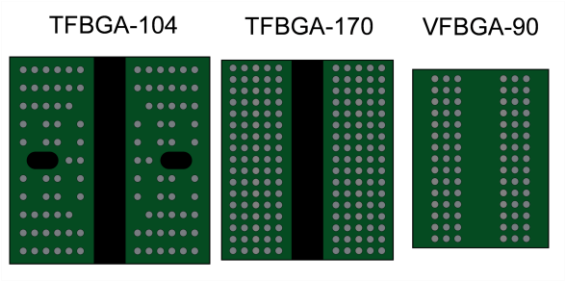


***Figure 3: Bottom view on the investigated package types TFBGA-104, TFBGA-170 and VFBGA-90***

The characteristic geometrical data of the packages are listed in table 1. The packages vary in the number of balls which result in different ball-out sizes due to equal contact pitches of 0.8 mm in both directions. Only the TFBGA-104 has an increased pitch parallel to the bond channel of 1.27 mm which results in a bigger ball-out area than the TFBGA-170. The VFBGA-90 has a smaller ball-out size and a reduced height than the TFBGA packages. Further geometrical differences between all packages are the chip sizes. However, these dimensions are of minor importance since all of them are much smaller than the total packages and thus do not influence the stresses generated at the critical corner solder balls.

***Table 1: Geometrical data of the investigated package types***

| Package type | Height [mm] | Package area [$mm^2$] | Number of balls | Ball-out size [$mm^2$] |
|---|---|---|---|---|
| TFBGA-104 | 1.2 | 14.5 x 14.0 | 104 | 12.7 x 12.0 |
| TFBGA-170 | 1.2 | 14.0 x 12.0 | 170 | 12.8 x 10.4 |
| VFBGA-90 | 1.0 | 12.5 x 9.5 | 90 | 11.2 x 6.4 |

## 3. Experimental results

The evaluation of the experimental results is split in two parts. In the first part the mechanical failure analysis is done by the dye and pry method for all tested and electrically failed components. Since all JEDEC boards are dropped 500 times, numerous failed solder joints can be found beneath the high stressed component positions. Thus the target of this failure analysis is the identification of those solder joints, which ultimately cut the daisy chain and can be related to the cycles-to-failure.

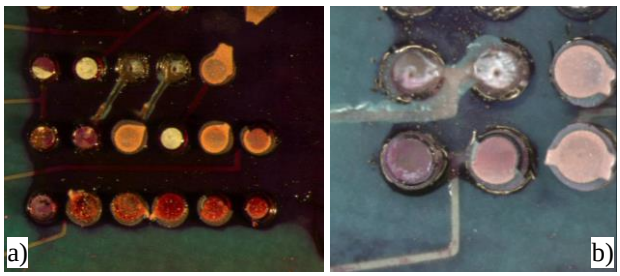


***Figure 4: Dye and pry failure analysis of package types TFBGA-104 (a) and TFBGA-170 (b). Ultimate failure mode of both packages are lifted substrate pads.***

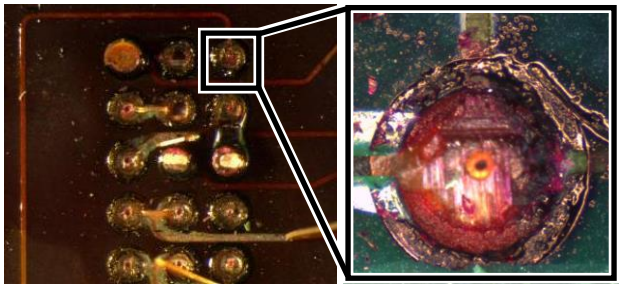

***Figure 5: Failure analysis of package type VFBGA-90. The failure of the daisy chain is caused by a broken copper trace connection to a PCB pad.***

The results of the mechanical failure analysis are shown in figure 4 and 5, respectively. Both figures show the PCB after the component is pried open. Figure 4 shows the failure analysis of the bigger packages TFBGA-104 (a) and TFBGA-170 (b). As expected, both figures show several failure modes but at the high stressed corner there are numerous broken and lifted substrate pads. Since these are the only failed solder joints, which may have caused the electrical cut of the daisy chain, these damages must be the ultimate failure modes. This result is confirmed for both packages at other failed component positions and for all tested PCBs.

Figure 5 shows a different result for the VFBGA-90 package. In this case, more lifted PCB pads are observed after the pry open of the components. However, at numerous joints these pad lifts can not cause any electrical cut since the pads are still connected to their according copper traces. But at specific positions broken copper traces are found at the edge of the PCB pads remaining in the PCB after prying open. Those copper traces indicate the cut of the daisy chain structure. Again this failure can be confirmed at all failed component positions on all tested JEDEC boards.

In the second step the statistical result analysis is done, in order to derive characteristic cycles-to-failure from the scattering experimental data. These characteristic lifetimes are derived at each critical component position separately for all package types. In this way sequences of failure are gained, which are used to identify the high stressed positions on the JEDEC board and to find relations between the sequence of failure and the failure mechanism.

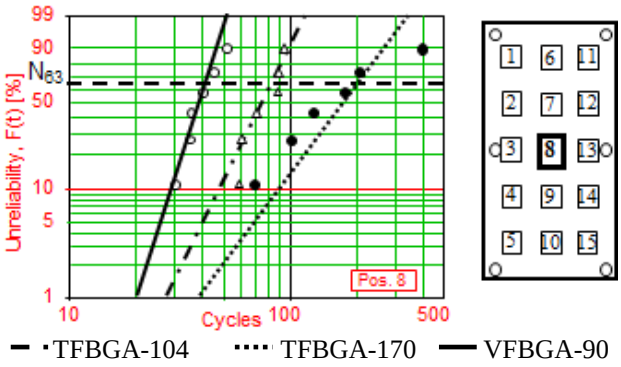


***Figure 6: Weibull plots of the tested packages at component position #8***

The experimental cycles-to-failure are analyzed by Weibull distributions, see figure 6. The main results of these analyses are the mean values. Figure 6 shows the Weibull distributions of the investigated packages at PCB position #08. Except for the TFBGA-170 the experimental cycles-to-failure can be fitted well by the Weibull distribution. The distributions of TFBGA-104 and TFBGA-170 have a lower slope indicating higher scatter of the experimental cycles-to-failure. The VFBGA-90 has the smallest characteristic lifetime of 41 cycles. Obviously the copper trace cracks are more critical under the tested conditions, since this failure mode is able to outbalance the higher solder joint stresses arising from the bigger package size. The cracks of the substrate pads appear with bigger scatter resulting in the aforementioned lower slope of the Weibull distributions and higher characteristic lifetimes, see table 2. However, the sequences of failure are not affected by the failure mode. In all cases, failures appear in the inner row of components (#06 - #10) and position #08 has the lowest characteristic lifetime.

***Table 2: Characteristic cycles-to-failure of the tested packages at component position #8***

| Package | TFBGA-104 | TFBGA-170 | VFBGA-90 |
|---|---|---|---|
| Characteristic lifetime [cycles] | 81.8 | 221.2 | 41.3 |

## 4. Simulation models

The failure analysis applying FEM simulations has to be split in two parts for every package type. An immediate investigation of the detailed solder joint stresses is impossible, since the required number of elements is too high and their size is too small in order to

achieve an acceptable calculation time. That is why the FEM sub-modeling technique has to be applied.

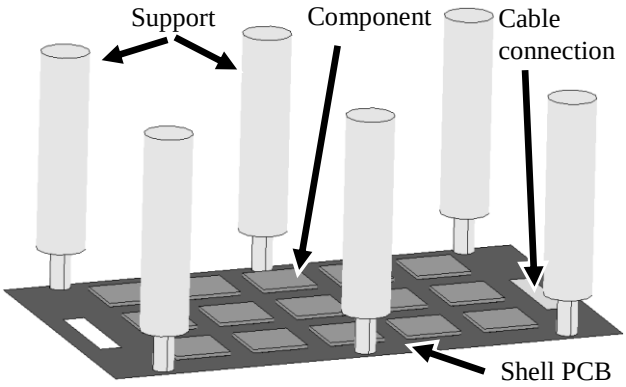


***Figure 7: Global simulation model of the JEDEC drop test setup including the PCB supports and the 15 components***

In the first simulation step the entire structure is modeled with the global model as shown in figure 7. The role of this global model is the representation of the board vibrations after the drop event, which is the input for the fine meshed sub-model. Previous papers [10] have shown that it is necessary to represent the PCB supports and the mechanical behavior of the PCB by the laminate theory in order to achieve a realistic vibration of the FEM model. For example the neglect of the supports results in a too stiff behavior of the structure, which causes too high vibration frequencies and too high amplitudes. Due to the role of the global model it is sufficient to model the components in a coarse way. The packages are represented as full mold compound bricks. The interconnections between PCB and component are modeled as simple solder bricks for the inner connections and solder barrels at the outermost high stressed connections. Thus, the global models require about 100.000 elements.

The second simulation step applies a fine meshed sub-model of a single component. This sub-model is set at the highest stressed PCB position #08, which was previously confirmed by the results of the global model. The sub-models of the packages represent all mechanically relevant parts, including the substrate and PCB solder masks. High attention is paid for the finite element meshes of the solder interconnections. The solder joint models include the copper pads on PCB and substrate side. According to the experimental setup the substrate pads are SMD and the PCB pads are n-SMD. However, the joint models do not include any IMC layers at the solder copper interfaces since their small size cause a considerable increase of simulation time and no appropriate material data are available. Additionally, the PCB pads of the outermost solder joints are connected to copper traces, which are routed according to the experimental design. The sub-model PCB is made of shell elements, similar to the PCB of the global model. This allows a convenient transition of the global model vibrations to the sub-model and keeps the mechanical PCB behavior. But this modeling technique requires contact elements in order to connect the component to the PCB. Since a direct contact connection of the result sensitive PCB copper pads may cause overstress, an additional PCB epoxy layer is set underneath the copper pads.

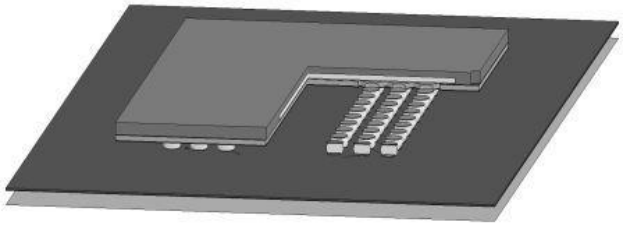

***Figure 8: FEM sub-model of a VFBGA-90 package including a cross-section through the component***

The high speed deformations during drop tests cause special requirements of the FEM material models. Mold compound, die adhesive, PCB resin and solder mask are far off their glass transition temperature and the deformation speed is too high in order to cause any visco-elastic effects. A pure elastic behavior is sufficient for these materials. Substrate and PCB are laminate materials. However, a laminate material behavior as presented in [11] can be applied only in combination with shell elements [12]. Due to the contact problem mentioned before, the complete laminate material model is applied for the PCB only. The substrate behavior is represented by an effective orthotropic-elastic model using the tensile strength of the laminate.

Copper cracks cause the ultimate failures of the experimental specimen. Thus, a plastic behavior is required for the copper. The plastic hardening behavior of copper tends to be isotropic [13]. This behavior is provided by LS-Dyna's material #18, which applies a power law hardening rule. In this load condition the solder shows a time dependent deformation behavior. Due to the high deformation speeds it has a strain-rate dependent yield behavior. According experimental data are provided in [14, 15] and its necessity is shown in [16]. With these simulation models at hand, a realistic FEM failure analysis gets possible.

## 5. Simulation results

The simulation results of the coarse global model show that within a single component the highest interconnection stresses and strains are created at the corner solder joints. Furthermore, the global model simulations prove the experimental finding that the highest stresses are created in the central component position #08. That is why all FE-sub-models are set at this position in order to analyze the individual failure formation in the solder joints.

The sub-model simulation results provide a diverse insight on the stress distribution in the solder joints. High stresses are generated where the differential movement of PCB and component is initiated to the solder joint. The resulting load of the joints is not a simple alternating tensile load. There is also a shear component since the packages are situated far off the neutral bending axis of the PCB. Thus a complex failure formation or even interacting failure modes are possible as seen in [17].

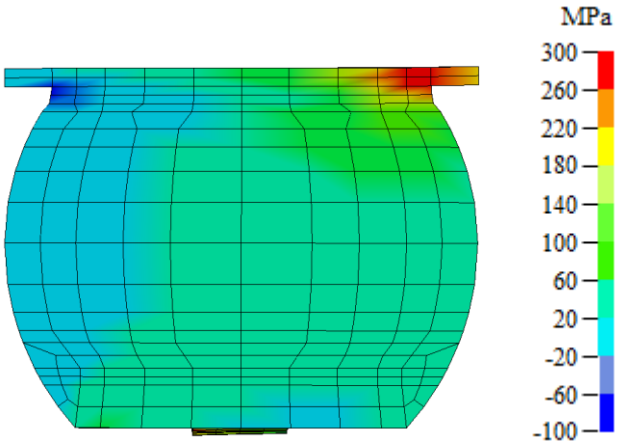


***Figure 9: Distribution of 1st principal stress within a corner solder ball of a TFBGA-104 package at the moment of first PCB deflection***

Figure 9 shows the distribution of the 1st principal stress in a corner solder ball of a TFBGA-104 package. This figure shows the distribution at the moment of the first maximum PCB deflection. This is the moment when the highest stresses are created, which may cause initial failures. Those failures are related to brittle cracks such as IMC cracks or pad delamination. However, the load at those interfaces is not uniformly distributed whereby complete cracks can not be created during a single PCB deflection. Those graphs indicate possible crack initiation areas, which may cause changed stress distributions during ongoing vibrations or further drop events. In case of figure 9 highest stresses are created at the substrate pad and the according IMC layer. Thus a pad delamination or an IMC crack may be initiated during this stress peak. However, previous investigations [17] have shown that higher stresses and strain rates are required in order to cause IMC cracks. A pad delamination seems to be more realistic, which proves the experimental findings. Similar load distributions are found at the corner solder joints of the TFBGA-170 packages.

Figure 10 shows another stress distribution during the first PCB deflection for a corner solder joint of the VFBGA-90 package. The solder joint model has a flaw already, which was caused by the bad orientation of the copper trace and the resulting stress on the solder on top of the PCB pad [17]. Although the solder joint is not ideal and the flaw causes a certain stress relief at the PCB side, the copper trace is stressed higher than the component side. This indicates that the copper trace tends to fail before any other part of the solder joint.

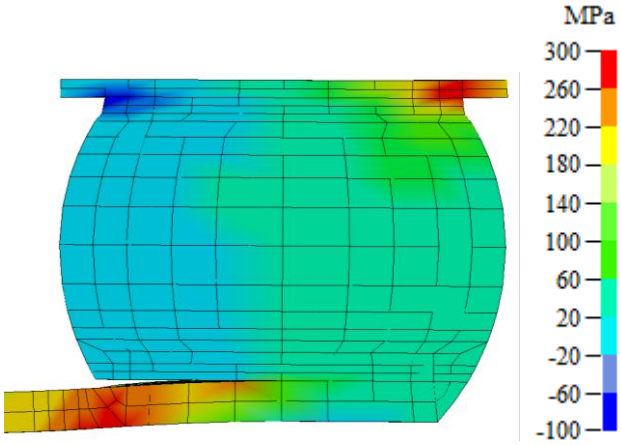


***Figure 10: Distribution of 1st principal stress at a corner solder ball of a VFBGA-90 package at the moment of first PCB deflection. The interconnection model includes a flaw between pad and solder due to the high stress orientation of the copper trace [17, 18].***

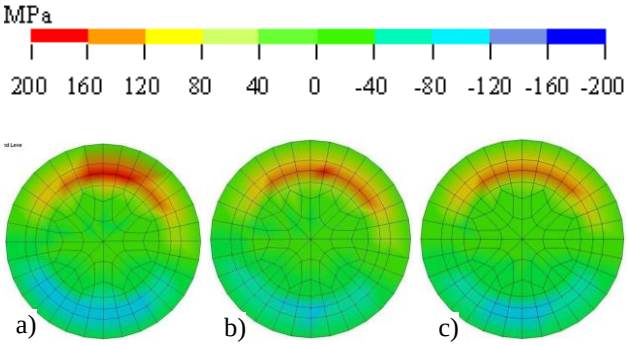


***Figure 11: Distribution of stress perpendicular to the substrate pad surface: a) TFBGA-104; b) TFBGA-170; c) VFBGA-90***

The stress generated perpendicular to the surface of the substrate pads may be a well suited indicator for the initiation of delamination. However, it is difficult to assess those values since there are no stress levels available which indicate the copper delamination. This way a qualitative comparison has to prove the tendency for those failures. Figure 11 compares the stresses at the most critical solder joints of each package. The figure shows the highest delamination stress at the TFBGA-104 package. The other packages TFBGA-170 and VFBGA-90 are almost at the same level. But in case of the TFBGA-170 there is no high stress at other critical parts of the interconnection. As described before the high stress region is limited to a small part of the pad. This region is just the place of the failure initiation, which results in changed stress distributions as soon as first flaws are created.

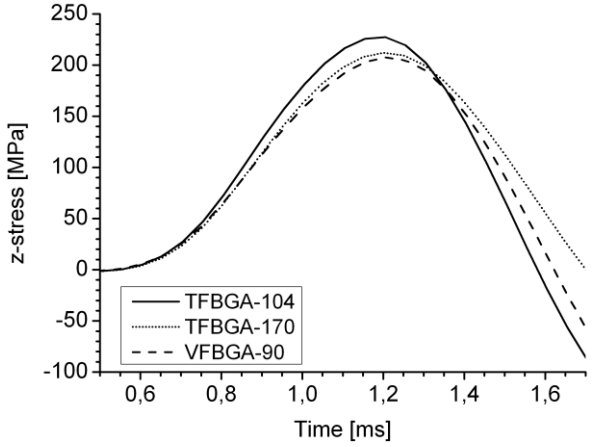


***Figure 12: Comparison of the maximum stress peaks in the substrate pads of the investigated packages***

Figure 12 shows the time-dependence of the stress perpendicular to the substrate pad surface for all packages. High tensile stresses are generated during the first PCB deflection. As soon as the PCB moves back the stress reduces and turns into compressive stress. However the tensile load causes cracks or delamination, which have major effects on the further failure formation. As shown in figure 11, clearly the highest stress appears in the TFBGA-104 package. A partial pad delamination or later cracks in the copper pad are possible under those load levels. As seen before, figure 12 shows the small difference in the maximum stress of the VFBGA-90 and the TFBGA-170 packages. The stress in the TFBGA-170 is marginally higher. Whether this is sufficient in order to pass a delamination threshold can not be proven. Obviously, a pad delamination requires more drops to propagate completely through an interconnection. That is why the characteristic lifetimes of the components failing by those defects are much higher than for the VFBGA-90 package. Furthermore, pad delamination can not be found at the VFBGA-90 packages because their solder joints fail at the PCB side before, which releases all the stress on the substrate side.

## 6. Conclusions

The JEDEC drop test causes severe stresses in BGA solder joints. These high stress levels are able to cause different failure modes in those 2nd level interconnections. But a correct prediction of the experimental failure mode by means of FEM simulations is difficult. However a failure mode prediction helps to identify basical weaknesses and thus simplyfy corrective actions to increase the lifeteime of the solder joints.

The experiments presented here reveal that the failure mode caused by the drop tests is dependent on the package type. All specimen are fabricated with same materials and processes. The solder joint geometry remains constant and the specimen are not exposed to thermal aging. But still the failure mode changes from PCB copper trace cracks to broken substrate pads with a growing package size. Beyond those bigger packages have longer characteristic cycles-to-failure than the smaller one although the test conditions are kept constant. These unexpected results are analyzed by additional FEM simulations.

The simulation results reveal the highest stresses at the corner solder joints. Within these solder joints there is a non-uniform stress distribution. This stress distribution has its maximum in a small area at the substrate pad pointing to the inner side of the ball-out. The stress level created there shall be sufficiently high to cause pad delamination but according to previous studies it is insufficient to initiate an IMC crack. This stress distribution is influenced by a PCB side copper trace pointing to the direction of highest PCB curvature. In this case the highest interconnection stress is created in the copper trace. Due to its small cross-section and the bad orientation those copper traces are prone to fail much earlier than the substrate pads proving the experimental observations. In this way the experimantal conflicts are explained. Furthermore this analysis finds reasons and effects of different failure modes. These results help to improve the prediction quality of the cycles-to-failure of BGA interconnections under drop test conditions.

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