Realistic Stress Representation in 2nd Level Interconnections of Productive BGA Components During Drop Test Simulations

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Abstract

Virtual prototyping is able to speed-up the development cycle of new products if based on exact models. In case of dynamic mechanical loads like JEDEC drop tests of BGA modules, broken copper traces at the PCB side are more and more often observed to be the ultimate failure effects. Straightforward FEM simulations showed unrealistic high stress and strain results not matching with the experimentally gained characteristic lifetimes of productive BGA components.

A comprehensive physical investigation of the failure formation during JEDEC drop tests has revealed the complex nature of the dynamic failure formation. In addition to the ultimate fracture of the copper trace, a flaw of the IMC layer on top of the PCB pad has been identified by 3-D X-ray tomography. Obviously, both failure mechanism are initiated during the consecutive drop events at different times propagating with different speeds. Both mechanisms are interacting with each other with no single mode alone dominating the failure evolution. Hence, FEM simulations have to account for both failure mechanisms in order to capture the ultimate copper trace stress realistically.

Simulation results dramatically gained realism after including the IMC crack. The plastic copper trace strain is reduced by 80 % compared to an interconnection without IMC flaw. Now the plastic copper strain has reached realistic values indicating possible lifetimes as seen in the experiments. The overall routing effect of the PCB copper traces was investigated applying this new simulation methodology. The resulting strain map clearly indicates the routing direction, which is parallel to the short PCB edges and leaving the component as the most critical, which is in agreement with experimental observations.

This very realistic 2nd level interconnection model has been used to assess the lifetime of the investigated packages. A lifetime model was derived, which is able to predict the experimental number of cycles-to-failure of all three packages at different PCB positions with less than 25 % deviation. The results presented here set the ground for virtual prototyping, which also includes the BGA drop test endurance.

Introduction

Virtual lifetime estimations require the precise knowledge of failure mechanism and failure position under all test and service conditions in order to predict reliable numbers of cycles-to-failure. This requires a close interaction between simulation and experiment during the model development and verification.

This paper presents the development of a trustworthy virtual lifetime model based on FEM for mechanical drops of microelectronic components on a PCB. The JEDEC drop test is the basic experimental methodology for this development. The main advantage of this test is its high failure reproducibility. Characteristic cycles-to-failure were obtained by this methodology for each of the 15 components on the well defined JEDEC board. The sequence of failing components at their board position is used to select a proper failure criterion and to evaluate the simulation methodology. Currently, the accuracy target is set to ±50 % for the prediction based on FEM. Of course this target can only be fulfilled if the dominating failure mode has been identified and transferred adequately to the simulation model.

Experimental setup

The JEDEC standard JESD22-B111 [1] is the best suited drop test experiment, which can be transferred to a FEM-based simulation model. The standard precisely specifies the drop test setup, the specimen and especially the load conditions of a drop test for 2nd level assemblies. This way, highly reproducible results can be achieved with this methodology, which is essential for detailed failure and lifetime analyses by FEM simulations. The schematic of this methodology is shown in fig.1.

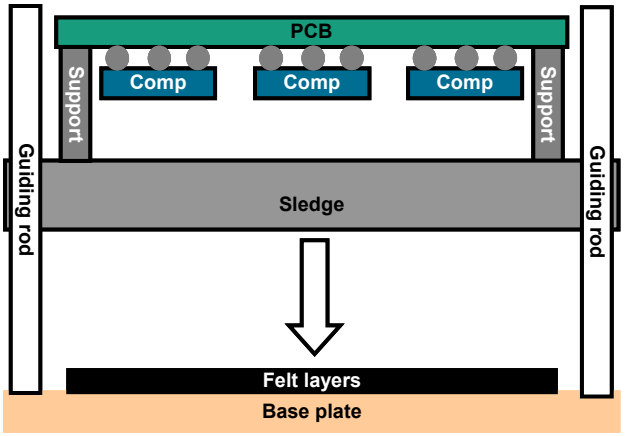

Figure 1: Schematic of the JEDEC drop test setup

In this study, JEDEC drop condition B was used, i.e. the 0.5 ms sinusoidal pulse had a peak acceleration of 1500 G on top of the sledge. This acceleration impulse was continuously measured proofing its conformity during all tests. In contrast to the standard the JEDEC PCB was fixed by 6-screws with additional screws at the middle of both long board edges. Due to these modified boundary conditions the eigenmodes and eigenfrequencies of the PCB were changed, resulting in different stress and failure distribution of all 15 components on the board. Applying this setup, electrical failures of the

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daisy-chained packages appeared after some 10 to a few 100 drops depending on the packages investigated.

The JEDEC PCBs were completely assembled with 15 BGA components, each. This investigation included 3 different packages, which are listed in tab. 1. These daisy-chained packages were designated for memory applications, resulting in a ball arrangement of two groups with 3 rows each around a central bond channel. The solder applied here was SnAg1Cu0.5. The SMD copper pads of the components had electro-less nickel/gold finish, whilst the N-SMD PCB pads were covered with Cu-OSP.

Table 1: Geometrical data of the investigated daisy-chain packages

Package type	VFBGA-90	VFBGA-60	TFBGA-60
Height [mm]	0.8	0.8	1.2
Package area [mm]	12.5 x 9.5	10.0 x 9.5	10.5 x 8.0
Number of balls	90	60	60
Ball-out size [mm]	11.2 x 6.4	7.2 x 6.4	8.0 x 6.4
Ball arrangement	15 x 6, full rows	10 x 6, full rows	11 x 6, partly populated

Failure detection was done by single in-situ resistance measurements of all 15 components separately. The measurements were done continuously throughout the test. As defined by the JEDEC standard [1], the failure flag is set when the event detector captured 1 kΩ or more in three consecutive drop cycles.

Experimental results and failure analysis

Cycles-to-failure were recorded for the at least 3 most critical package positions on every JEDEC board. These data were analyzed by Weibull distributions. Weibull plots were generated separately for each of these critical component positions of each package type. The outcome is a characteristic number of cycles-to-failure, N_{63}, for each package type at the most critical positions on the board. Applying these data, the drop endurance of the investigated packages can be derived for its individual stress level depending on its PCB position. A basic result is the derivation of a sequence of failing component positions. This sequence might be used to initially assess the accuracy of different simulation result criteria. Simulation criteria which can not follow the experimental sequence of failure are not suited for further lifetime estimations. The characteristic cycles-to-failure and the sequence of failing component positions is shown in tab. 2.

The results of tab. 2 show that the most critical component positions are situated in the central row of the JEDEC test board see fig. 7. This is caused by the deformation behavior of the PCB under 6-screws boundary condition, which is dominated by a bending along its small edges. The central position #8 always fails first, followed by neighbor positions. The package size has a strong influence on the characteristic number of cycles-to-failure. The bigger the package the smaller is the drop endurance. Due to this fact the biggest package VFABGA-90 failed earlier and at more component positions than the smaller packages with 60 I/Os.

Table 2: Characteristic lifetime, N63, and sequence of failure of the most critical component positions for all investigated package types

Package type	VFBGA-90	VFBGA-60	TFBGA-60
Comp 06	89 (4)	-	-
Comp 07	94 (5)	291 (3)	161 (3)
Comp 08	43 (1)	90 (1)	68 (1)
Comp 09	58 (2)	141 (2)	113 (2)
Comp 10	70 (3)	-	-

Failure analyses of the drop tested samples are done by dye & pry tests. This method is very effective and allows for the analysis of every failed package. As an example, figure 2 shows the result of a TFBGA-60 package. The red colored sections were damaged during the experiment, while the other sections were damaged during the lift-off of the component. The analysis reveals that electrical failures were dominantly caused by broken copper traces at the PCB pads. More detailed analysis shows that these cracks do only appear when the copper traces follow the direction of highest PCB bending. As shown in figure 2, electrical failures do not only appear at the corner joints of a package, which are the most stressed under drop test conditions. In this case the copper trace at the second joint follows the direction of highest PCB deflection and thus causes the failure.

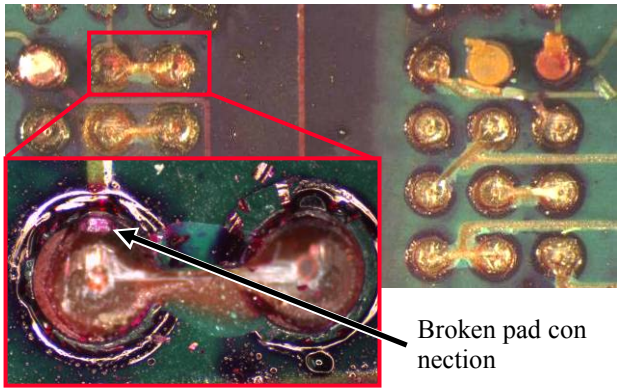

Figure 2: Failure analysis with dye & pry test. Broken copper traces at the PCB pads cause the electrical failures

More detailed failure analyses were done by 3-D X-ray tomography. A 3-D X-ray scan allows a deeper analysis of multiple failure mechanisms, which can not be found by the dye & pry tests. The procedure, however, is more time consuming due to difficult picture analysis and thus it is not applicable to scan every failed component of a batch.

The 3-D X-ray scan surprisingly revealed the complex nature of the failure formation in the investigated samples. In addition to the broken copper trace an IMC flaw at the interface between PCB pad and solder ball was detected, which is shown in fig. 3. Both failure modes seem to be initiated during the drop event at different times and propagate with different speeds. While the IMC crack was almost

stopped most probably due to reduced stress within the solder joint, the copper trace was further damaged with every drop event due to PCB bending and caused the ultimate failure.

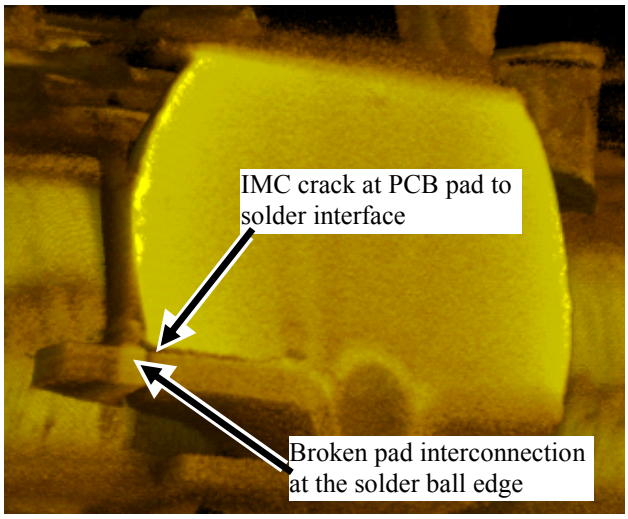

Figure 3: 3-D X-ray tomography analyses of a productive package

The precise knowledge of the failure modes and the failure position under all test conditions is absolutely required to develop precise lifetime models based on FEM simulations. The failure modes detected by the X-ray tomography are mutually interacting with each other with no single mode alone dominating the failure evolution. Hence, FE models need to account for both failure modes in order to capture the copper trace stress realistically.

Global FE simulations of the JEDEC drop tests

FE simulations were executed applying the explicit code LS-DYNA. In this code the transient shock response of the investigated structure is calculated by small time steps. The size of these time steps is dominantly influenced by the smallest element size of the entire model. In order to achieve a reasonable computing time for a drop event the coarse meshed global model is simulated first followed by a finer meshed sub-model.

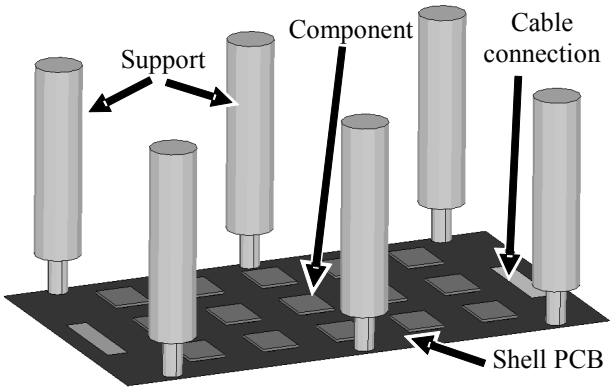

Figure 4: FEM global model of the JEDEC drop test assembly

The global model is a complete 3-D representation of the entire JEDEC test board including all 15 components. As shown in fig. 4, the model also accounts for the cable connection areas on the PCB and the supports. The steal supports transfer the acceleration impulse of the drop event to the PCB. Comparison between experimentally recorded and simulated acceleration curves has shown that the supports do not act absolutely rigid and thus influence the PCB motion [2]. A similar effect was detected for the cable connection areas which have an additional damping effect on the PCB.

The packages are modeled in a rather simple way. The hexahedral component bodies apply effective elastic material properties similar to those of mold compound. The solder joints are modeled as bricks without any copper pads within. The solder bricks apply a rate dependent plastic material model [3]. Only the most critical joints at the outermost rows are modeled as barrels replicating the actual dimensions at both pads as well as at the equator of the joint. The barrels are meshed by 24 elements, while 8 elements are sufficient for the solder bricks. These components are connected to the shell PCB by offset contacts. Shell elements are required for the PCB in order to apply the material model called composite matrix [4]. The resulting material properties of the PCB have to be calculated by the laminate theory [5]. This material model, however, is able to capture both tensile and bending stiffness of the PCB, which are typically differing a lot from each other.

The assumptions presented above are found adequate for the global model requirements. Its main task is to record the displacement data, which is the load input for the sub-model. Basic stress analysis is done with the solder barrels in order to quantify the load levels at the individual component positions.

Sub-model simulations

The sub-model is a detailed representation of a single BGA component. It substitutes the coarse mesh of the global model at an interesting subsection by a fine mesh in order to allow for a detailed failure analysis. It covers all mechanically relevant parts as shown in fig. 5. The component body includes the substrate, substrate solder mask, die attach film, die and the mold compound. The solder joints are modeled by the substrate pads, the solder ball, the PCB pads and the PCB copper traces. The PCB pads are non-solder-mask defined leaving the pads and a little bit of its trace uncovered. The copper traces may approach the PCB pad in any 45° direction, as shown in fig. 6. The influence of the routing on the copper trace stress can be investigated with this option. In order to capture the copper trace stress realistically, the IMC flaw detected by the X-ray scans has to be represented adequately. According to the results of the failure analysis twin nodes are generated at the pad-solder-interface in order to create separated elements. The flaw is covering half of the PCB pad starting from the copper trace. Penetration of the adjacent elements with separated nodes is prevented by contact definitions.

The PCB is meshed by shell elements again while all remaining parts of this model are meshed by solid elements. The bottom of the PCB pads and the solder mask are connected to the PCB by offset contacts. Potential model edge effects are minimized by a sufficient PCB size, which is about twice the length and the width of the component. According to the stress distribution, the outermost joints have fine meshes

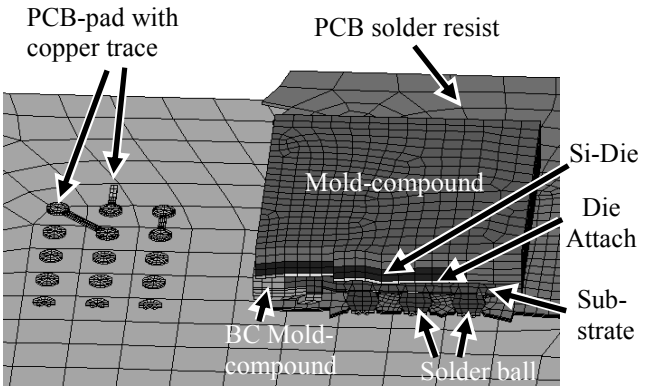

Figure 5: X-section of a TFBGA-60 sub-model with its characteristic constituents

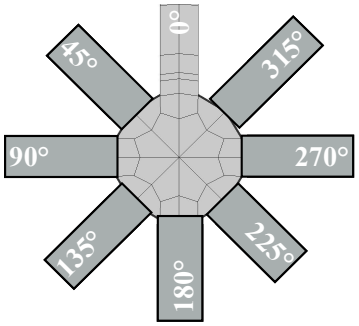

Figure 6: Copper trace orientations at the sub-model copper pads for the investigation of the routing effects

while a more coarse mesh is sufficient for the inner interconnections.

The material models of the parts within the component body are linear elastic. No large deformations and no or negligible non-linear material behavior is expected in these parts. The PCB material is modeled by the direct composite matrix, similar to the global model. Similarly, the solder applies the material behavior presented for the global model. The copper traces and pads use a plastic material with isotropic hardening [4] following the coefficients provided by [6].

A realistic copper trace strain map

The detailed stress analysis of the copper traces has been executed with the TFBGA-60 component at the most critical PCB position #8, see fig. 7. This component was chosen due to its distinct experimental failure distribution. The copper trace routing effect was evaluated by eight sub-models with changing routings at each of the outermost PCB pads. It is assumed that the routings of the outermost joints do not affect each other.

Different result criteria may be applied to assess the mechanical loading of the copper traces. The plastic strain accumulated in the copper trace between the pad edge and the solder mask was chosen due to the results of earlier work [2]. As detected in the failure analysis, maximum copper strain appears at the edge of the solder ball.

The copper trace routing effect is shown for interconnections A1 and L1 in fig. 8. As expected, there is a strong influence of the routing direction on the resulting plastic strain. The maximum plastic strain appears in 0° and 180° direction for joints A1 and L1, respectively. A plastic strain of about 3 % is created in these worst configurations. This is significantly lower than a value of up to 15%, which was reported in [7] without the consideration of an IMC flaw. Thus the IMC flaw is an important failure mode, which necessarily has to be considered in those simulations in order to yield in a realistic copper trace stress. Consecutive simulations of a single sub-model have shown that this initial amount of plastic strain per drop is even reduced by further 90 % within the fist four drops remaining in this stable growth rate. This way the strain increment per drop seems to be reasonable to pass about 70 drops until ultimate failure.

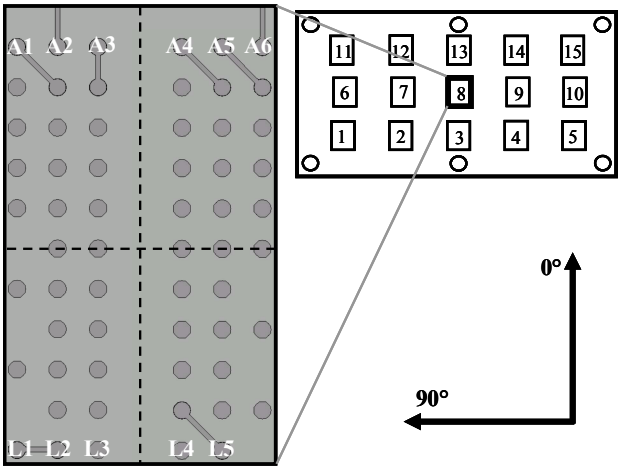

Figure 7: Sub-model orientation on the JEDEC board and experimental/initial PCB pad design of the TFGBA-60

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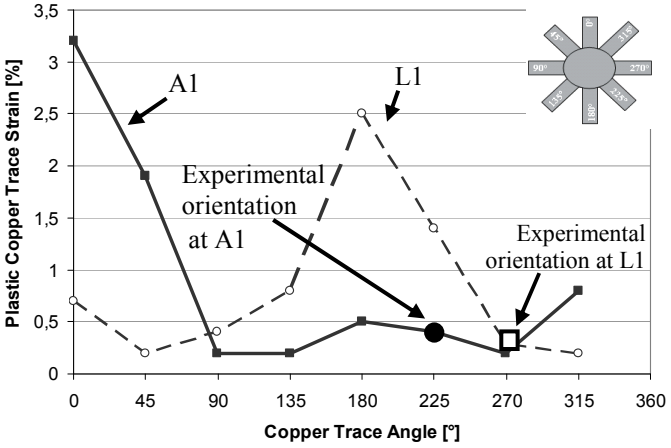

Figure 8: Copper trace routing effect

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The strain curves of A1 and L1 are very similar. They just have an offset of 180°. Highest strain appears when the copper traces are routed parallel to the PCB width leaving the component, which fits to the experimental observations. The plastic strain clearly declines the further the traces are routed differently. The most save option is a routing towards the component center.

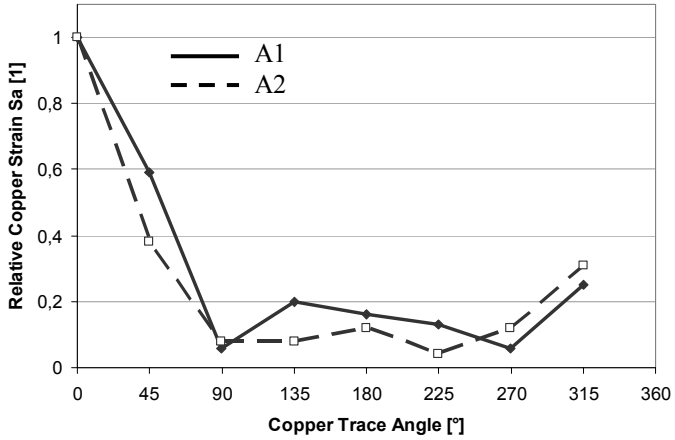

Figure 9: Relative copper trace routing effect

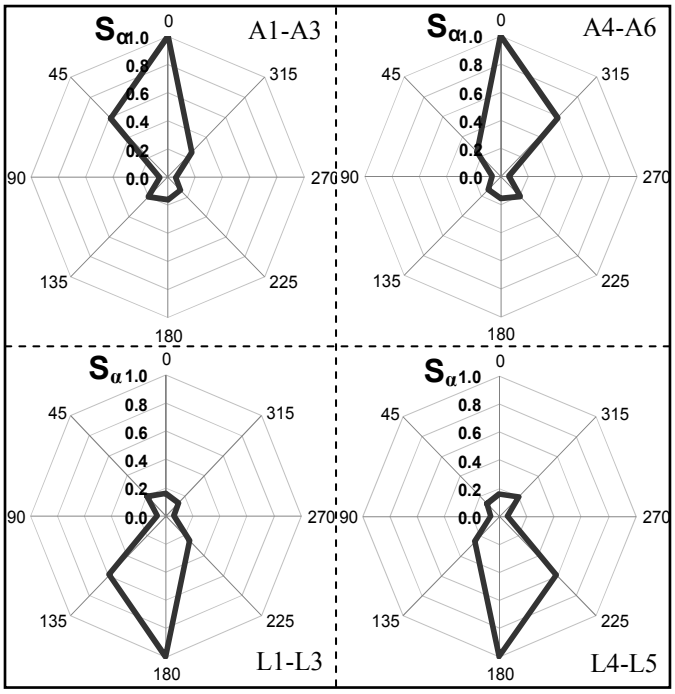

Figure 10: Strain map for 6-screws boundary condition of the Jedec PCB

The relative distribution of the copper trace routing effect is shown in figure 9. This relative strain distribution S_α is simply calculated by setting the plastic strain at any trace orientation in relation to the maximum plastic strain at this interconnection (1),

$$S_\alpha = \frac{\varepsilon_\alpha}{\varepsilon_{\max}} \qquad (1).$$

The comparison of the outermost joint A1 with its adjacent joint A2 shows only little differences of S_α between both interconnections. Thus both distributions can be combined into a single group for the upper left component quarter, fig. 7. Again the strong influence of the routing effect can be seen in this graph. Any other routings than the 0°-direction cause less than 40 % of the maximum plastic strain. All other routings are supposed to fail much later than those following the critical 0°-direction.

The combined relative strain distributions for all package quarters are shown in fig. 10. As stated during the introduction of S_α the relative distribution can be similarly found at every outermost interconnection. This way a symmetrical strain map was derived which is able to show the potential of a failing copper trace routing on the entire ball-out of the component.

The strain map introduced in fig. 10 is applicable to all component positions of the middle row on the JEDEC board (position #6 to #10), since the stress distribution is similar for all these packages if the PCB is supported in a 6-screws configuration. Furthermore this strain map can be applied for similar package types failing with broken copper traces. The routing effect will be considered with the pre-factor S_α in addition to the interconnection stress calculated by the global model. The lifetime estimation will be done applying a combination of these two criteria.

Lifetime model for JEDEC drop tests

The most important essence of a FEM-based lifetime model is a solid and reliable result criterion. As shown in previous studies [2, 7, 8] SEND (2) has proven to fulfill these requirements completely. High stress components can be identified precisely with this criterion on the entire JEDEC board. However this criterion is not able to identify the failing solder joint, which triggers the point of electrical failure in the experiments.

$$SEND = \int \dot{\varepsilon}_{pl} \cdot \sigma_{Pad}\, dt \qquad (2)$$

The combination of this basic global failure criterion $SEND_{bas}$ and the sub-model copper strain map S_α should be able overcome its limitations and identify the failing solder joint correctly, equation (3),

$$SEND_{corr} = S_\alpha \cdot SEND_{bas} \qquad (3).$$

The TFBGA-60 package was chosen again due to its distinct experimental copper trace routing, see fig. 7. The results of both failure criteria are shown in tab. 3.

The uncorrected energy values of $SEND_{bas}$ predict the first failure to appear at interconnection row L. Based on these values interconnection L5 should fail first and trigger the component failure. But experimental failures never appeared at this interconnection. The consideration of the copper trace routing effect is able to outbalance these experimentally uncritical interconnections and highlight the failing joints A2 and A6. Due to the correction of the energies applying S_α, the

values at all other interconnections are much lower. Joints with good-natured copper trace orientations are not suspected to fail at all. The new strain map resulting from the consideration of the IMC flaw highlights the critical interconnections even stronger, since the influence of routing is much higher in these conditions.

Table 3: Corrected and basic values of SEND at critical interconnections of a TFBGA-60 package at board position #8

Intercon-nection (fig. 7)	$SEND_{bas}$ [mJ/mm^3] eq. (2)	$SEND_{corr}$ [mJ/mm^3] (S_α) eq. (3)	Experimental failure analysis
A1	26.6	3.5 (0.13)	Pass
A2	22.6	**22.6** (1.00)	**Fail**
A3	23.7	3.8 (0.16)	Pass
A4	23.9	4.8 (0.20)	Pass
A5	23.3	4.7 (0.20)	Pass
A6	28.4	**28.4** (1.00)	**Fail**
L1	36.7	2.2 (0.06)	Pass
L2	30.5	1.8 (0.06)	Pass
L5	42.3	5.5 (0.13)	Pass

The failure energies gained with $SEND_{corr}$ can be applied for lifetime modeling. Typically an inverse power law is the basis for such a lifetime model. All available experimental and simulation data of the three investigated packages were assembled for this model. The resulting simulated cycles-to-failure are compared with the characteristic N_{63}-values as shown in fig. 11.

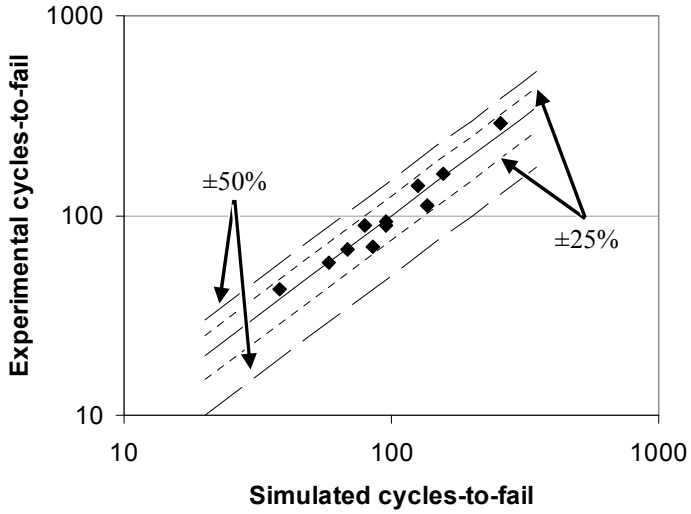

Figure 11: Results of the FEM-based lifetime model compared to experimental results

The comparison shows a close agreement between both curves. The difference between prediction and reality is less than ±25 %. This variation is well within the experimental scatter proving the sufficient accuracy of the combined lifetime criterion $SEND_{corr}$.

Conclusions

The development of a virtual lifetime model for the JEDEC drop test is presented in this paper. Industrially fabricated specimens were studied in the JEDEC drop condition B. All three different memory packages were tested with at least six JEDEC boards in order to determine the characteristic number of cycles-to-failure at several component positions on the board for each package type.

Failure analysis of all failed components revealed copper trace cracks as the dominating failure mode triggering the electrical cuts of the daisy chains. Detailed analysis showed that these copper trace only failed if the traces were routed along the direction of highest PCB deflection. This way, failure did not always occur at the most stressed corner solder balls.

Additional analysis was done by X-ray tomography. The failure analysis revealed the complex nature of the failure formation. Beside the copper trace crack, an additional IMC flaw at the solder-pad interface was detected by this technique. Both failure mechanisms seem to be generated during the drop events and both propagate with different speeds. None of the mechanisms is dominating the failure evolution alone but they are mutually interacting.

The new insights of the failure analyses were transferred to numerical simulations. The IMC flaw was represented at the interconnections of a detailed sub-model. The IMC flaw clearly reduces the stress on the copper traces. The maximum plastic strain only reaches up to 3 % per drop if the copper trace is routed in the worst direction. This value is well within the expected amount of plastic strain based on the characteristic number of 68 cycles-to-failure.

The copper trace routing effect was investigated with this model again. The resulting strain map highlights interconnections with a bad copper trace routing much stronger than in the case of disregarding the IMC flaw. Copper traces failing during experiments are highlighted much clearer now.

The final lifetime modeling applied a combination of the global energy criterion SEND and the copper trace routing. Critical interconnections, triggering the electrical failure during the experiments, were exactly indentified at each package. Having the correct energies of each failing interconnection at hand, the expected lifetime could be assessed very close to the characteristic number of cycles-to-failure. The inaccuracy between experimental and simulated lifetime was less than ±25 %. This is well within the experimental scatter and thus well within the original target.

Acknowledgments

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