The Need and Opportunities of Electromigration-Aware Integrated Circuit Design

(Invited Paper)

Steve Bigalke, Jens Lienig
Institute of Electronic Design
TU Dresden
Dresden, Germany
steve@bigalke.us, jens@ieee.org

Göran Jerke
Automotive Electronics
Robert Bosch GmbH
Reutlingen, Germany
goeran.jerke@ieee.org

Jürgen Scheible
Robert Bosch Center
for Power Electronics
Reutlingen, Germany
juergen.scheible.de@ieee.org

Roland Jancke
Fraunhofer Institute
for Integrated Circuits
Dresden, Germany
roland.jancke@eas.iis.fraunhofer.de

ABSTRACT

Electromigration (EM) is becoming a progressively severe reliability challenge due to increased interconnect current densities. A shift from traditional (post-layout) EM verification to robust (pro-active) EM-aware design - where the circuit layout is designed with individual EM-robust solutions - is urgently needed. This tutorial will give an overview of EM and its effects on the reliability of present and future integrated circuits (ICs). We introduce the physical EM process and present its specific characteristics that can be affected during physical design. Examples of EM countermeasures which are applied in today's commercial design flows are presented. We show how to improve the EM-robustness of metallization patterns and we also consider mission profiles to obtain application-oriented current-density limits. The increasing interaction of EM with thermal migration is investigated as well. We conclude with a discussion of application examples to shift from the current post-layout EM verification towards an EM-aware physical design process. Its methodologies, such as EM-aware routing, increase the EM-robustness of the layout with the overall goal of reducing the negative impact of EM on the circuit's reliability.

CCS CONCEPTS

• **Hardware → Physical synthesis**; *Hardware reliability*; Circuit hardening;

KEYWORDS

Reliability, Electromigration, Current Density, Thermal Migration

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1 INTRODUCTION

The International Roadmap for Devices and Systems (IRDS) [11] and the International Technology Roadmap for Semiconductors (ITRS) [12] predict that semiconductors scale and interconnect cross-sections will decrease further over the coming years. Accompanying this trend is a reduction in the necessary currents due to reduced gate capacitances. However, the currents are not decreasing to the same extent as conductor cross-sections, so that current densities (resulting from the quotient of the conductor's current and cross-section) are increasing.

High current densities are the main driving force of electromigration (EM). Therefore, the reliability of integrated circuits (ICs) is increasingly endangered by EM; hence, EM is one of the most important topics that design automation has to deal with nowadays. According to the ITRS [12], we have reached the point where EM must be considered in our design flows because the interconnects in up-to-date technologies encounter already severe EM degradations (Fig. 1). The forecast for the next few years is even worse, as the ITRS predicts a lack of EM solutions in approximately 5 years [20]. Consequently, EM damages, such as hillocks or voids, are expected to be observed more and more frequently, limiting the interconnect reliability.

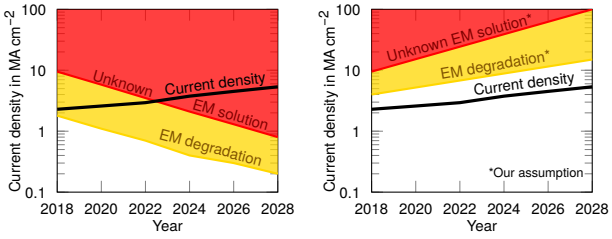


Fig. 1: (a) The need to consider EM in circuit design can be seen in the current densities projections (IRDS, ITRS), which has already entered the area of EM degradations and will develop into the range of unknown EM solutions [11, 12]. (b) EM-aware integrated circuit design tolerates the future current density and performance increases by hardening layouts against EM through raising the EM thresholds.

To make matters worse, the increase of current density takes place at the same time as the thresholds of current density decrease (see the yellow and red borders in Fig. 1a). The reason is that smaller interconnects are more sensitive to EM damages because, among others, the volume to change the interconnect's resistance decreases with its dimension. In other words, EM must move less material

in smaller interconnects than in larger ones in order to increase their resistance. In addition, the introduction of low-k ("softer") dielectrics further reduces the EM thresholds because their low stiffness weakens the surrounding's stability [27]. Interconnects can therefore withstand less mechanical stress than before.

The aggressive shrinkage of interconnects in recent decades has left only a few atomic layers within their smallest structures. A slowdown of the interconnect shrinking is expected in the future, as predicted in the ITRS [12]. With the introduction of FinFET transistors, we have already crossed the line where the transistor itself could drive higher current densities than the contact elements. This means that the back end of line (BEOL, the portion of IC fabrication where the individual devices get interconnected with wiring on the wafer) is becoming the limiting factor for future performance increases.

Another concerning aspect is that EM is accelerated by high temperatures. Specifically, the increase of currents densities, as well as frequencies, can cause local temperature hot spots within the interconnects. The resulting additional amplification of EM, known as "positive feedback loop" [19], leads to an even greater reliability degradation due to diffusion and void growth.

For all these reasons, *EM-aware design* has changed from something designers "should" think about to something they "must" think about, i.e., it is now a definite requirement. Since the number of EM violations will increase significantly in the verification step in future technology nodes, a post-layout repair step is no longer feasible. In other words, it is highly important that today's design flows change from the traditional (post-layout) EM verification towards a (pro-active) EM-aware design methodology, enabling the expected current density rise and ensuring reliable circuits (see Fig. 1b).

2 ELECTROMIGRATION AND ITS MITIGATION IN TODAY'S DESIGN FLOWS

2.1 Fundamentals

Electromigration (EM) is a process of material dislocation mainly driven by high current densities. This process also depends on temperatures, interconnect geometries, material parameters and manufacturing processes. However, the main cause of EM remains the movement of electrons driven by an electric field, which collide with the lattice atoms (Fig. 2). This momentum exchange creates an electron wind force in electron flow direction, which is much greater than the (opposite) force of the electric field. The current flow also heats the interconnect by Joule heating, which, in turn, increases the EM effect and can cause thermal migration (TM, also labelled as thermomigration). As a result of the material dislocation, the atomic concentration at the anode increases, causing compressive stress (and tensile stress at the cathode) to occur. The resulting stress gradient might cause a back flow called stress migration (SM).

Figure 3 shows a typical stress development over time within an interconnect with blocking boundaries at both ends. This interconnect structure is common for the widespread *dual-damascene technique*. The stress is slowly building up because EM moves atoms from one side to the other and, therefore, changes the concentration within the interconnect. The balance between EM and SM, also called *steady-state condition*, defines the maximum and minimum

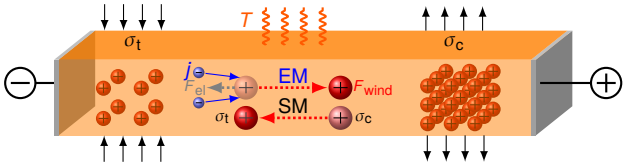


Fig. 2: Conduction electrons (blue) collide with atoms (red) creating a momentum exchange and, therefore, driving atoms towards the anode. This reduces (increases) the atomic concentration at the cathode (anode) and introduces tensile (compressive) stress σ_t (σ_c).

stresses within the interconnect. If the maximum (minimum) stress is higher (lower) than a technology-dependent EM-threshold value, then a void (hillock) might form. (Note that we use "might" because EM is a statistical process with a certain degree of uncertainty.) If voids or hillocks occur, the interconnect might fail as the damage expands. The EM threshold for voids is usually lower than for hillocks due to a residual stress within the interconnect caused by the manufacturing process.

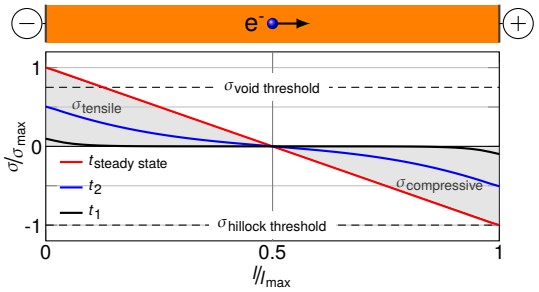


Fig. 3: Stress development over time in a confined interconnect. The final steady-state condition is the balance between EM and SM, defining the maximum and minimum stresses.

The difficulty in this migration process is that the current density, stress and temperature gradient can each cause an atomic flux $\vec{J}$ by themselves (called EM, SM and TM, respectively) described by

$$\vec{J} = \vec{J}_{\mathrm{EM}} + \vec{J}_{\mathrm{SM}} + \vec{J}_{\mathrm{TM}} = \frac{CD}{kT} eZ^* \vec{\rho j} + \frac{CD}{kT} \Omega \vec{\nabla} \sigma + \frac{CD}{kT^2} Q \vec{\nabla} T, \quad (1)$$

with the concentration C, diffusivity D, Boltzmann's constant k, temperature T, electric charge e, effective charge number Z^*, resistivity ρ, current density j, atomic volume Ω, hydrostatic stress σ and transported heat Q [28]. Therefore, we have three different driving forces but one problem – the (undesired) migration of atoms. All three kinds of material migration can mutually amplify or compensate each other, making the distinction even harder. The total atomic flux is subjected to the mass balance equation given by

$$\frac{\partial C}{\partial t} = -\vec{\nabla} \cdot \vec{J}, \quad (2)$$

which describes that a divergence of the atomic flux causes the concentration to change over time t [26]. This concentration change is then related to the development of stress in single and multibranch interconnects [7][16].

For many years, the current density has been the main indicator and design parameter for EM. Today, more and more approaches are also taking the interconnect geometry into account (e.g., [4][7][25]). The EM parameter of interest is therefore no longer only the length-independent current density but also the length-dependent stress [5].

2.2 EM-Mitigating Effects in Physical Design

While the aforementioned physical process of EM has been known for a long time, it only has gained importance over the last two decades, due to increased current densities related with IC down-scaling. Well-known options for mitigating EM in today's design flows are:

Interconnect material: Pure copper used for interconnect metallization is more EM-robust than aluminum at low temperatures.

Interconnect temperature: Interconnect MTF is greatly impacted by conductor temperature, as evidenced by Black's Equation [6] where it appears in the exponent. For an interconnect to remain reliable at high temperatures, the maximum tolerable current density of the conductor must necessarily decrease. On the other hand, lowering the temperature supports higher current densities while maintaining the reliability of the interconnect.

Interconnect width: Given that current density is the ratio of current and cross-sectional area, and that most process technologies assume a constant thickness of the interconnects, the width has a direct bearing on current density. The wider the interconnect, the lower the current density and the greater the resistance to EM.

The above mentioned three options have been discussed in detail in [17]. They are of limited use in today's technologies because they have been largely exploited and/or their application would be counter-intuitive to the new technology nodes that further reduce structure sizes [15]. Therefore, tolerable current density limits need to be maximized by exploiting other EM-inhibiting measures, which are discussed in detail in [18, 19] and are summarized next [20].

Bamboo effect: Diffusion typically occurs along the grain boundaries in an interconnect. High EM resilience can be achieved with conductor cross-sections smaller than grain sizes. In this case, grain boundaries are perpendicular to the direction of diffusion.

Short-length effect: Any interconnect length below a threshold length ("Blech length") will not fail by EM. Here, mechanical stress buildup causes a reverse stress migration (SM) which compensates for the EM flow.

Reservoirs: Reservoirs increase the maximum permissible current density by supporting the aforementioned SM effect to partially neutralize EM. Reservoirs can, however, have an adverse effect on reliability in nets with current-flow reversals, as the (useful) SM is reduced in this case.

Via configurations: The robustness of interconnects fabricated with dual-damascene technology depends on whether contact is made through vias from "above" (via-above) or "below" (via-below). It is easier to avoid EM in segments with via-below configurations than with via-above configurations, as the former tolerate higher current densities due to their higher permissible void volumes.

Redundant vias: Multiple vias improve robustness against EM damage. They should be placed "in line" with the current direction so that all possible current paths have the same length. Current distribution is then uniform and there is no local detrimental increase in current density between vias.

Frequencies: The high frequencies normally encountered in signal nets reduce EM damage more than in power supply nets or very low-frequency nets under otherwise comparable operating conditions. Hence, different current-density limits must be assigned to these "net classes" in EM analysis.

3 EM-AWARE LAYOUT DESIGN AND MISSION PROFILES IN INDUSTRIAL PRACTICE

3.1 Obtaining EM-Aware Design Rules Using Mission Profiles

The key for EM-aware design is to prevent the EM failure mechanism from causing a permanent damage or an excessive degradation of the interconnect metallization. This is achieved by obeying EM-aware design rules (subsequently "design rules") for the dimensioning of interconnects, contacts/vias and their local surroundings.

EM failures are greatly reduced in short connections due to the aforementioned short-length effect, but they must be considered for interconnects exceeding this layer-specific length limit. Design rules for these (long) interconnects are defined by maximum, average and DC current-density limits that depend on temperature, layer and quality goals. The design rules for interconnects must also account for root-mean-square and peak currents in order to prevent excessive Joule heating in interconnects by limiting the self-heating to a maximum permitted temperature increase.

Relevant design rules for a particular interconnect segment depend on a variety of technology-, design- and use-case-specific factors. In any case, the design rules which result in the largest interconnect dimensions or via numbers, must be considered during layout design. In the remainder of this section, we will discuss how design rules are derived for interconnects that do not benefit from the short-length effect. We also assume here that self-heating is considered separately.

Modern semiconductor technologies are typically applicable to a wide variety of applications for consumer, industrial, automotive and other safety-critical use cases. Applications targeted for different use cases face different environmental conditions and quality goals. Among others, the JEDEC Solid State Technology Association (JEDEC) [13] and the Automotive Electronics Council (AEC) [2] released several standards on (1) how to characterize and to qualify a semiconductor technology with respect to intrinsic and extrinsic failure mechanisms and (2) how to scale technology and design parameters for specific use cases. With respect to EM, these standards include JEP001A, JEP119A, JEP122H, JESD63, JESD87, JESD202 and AECQ-100.

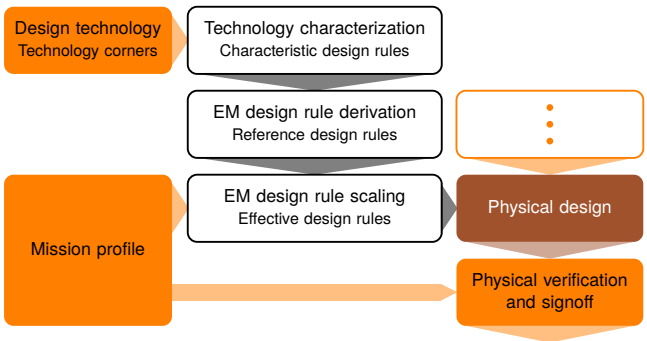


Fig. 4: General flow for technology characterization and the derivation of EM design rules [14, 19].

The derivation of the parameters of the EM-failure model during technology characterization is done under temperature-accelerated conditions (JESD63, JESD202 [13]). Next, the current density j_{char}

used during the characterization of a particular layer and temperature T_{char} must be scaled (using Black's Equation [6]) to one or more technology-specific reference conditions $j_{\text{max,ref}}$ at T_{ref} while considering reliability goals (Fig. 4). These goals are, for example, the permitted cumulated percentage of failed interconnects (typically CDF = $1e^{-8} \ldots 1e^{-11}$) over the targeted application lifetime. These values, including their scaling factors, are typically provided in the design rule manual of a semiconductor technology. For automotive applications, the AECQ standards [2] define several grades of maximum operating (junction) temperatures, application lifetimes and reliability goals. They are used to validate and qualify a technology and to provide fixed boundaries for the design rule derivation.

For the design of an individual application, all relevant use cases and operating phases must be taken into account to (1) choose the correct technology-specific reference condition (and subsequently the corresponding reference design rule $j_{\text{max,ref}}$ at T_{ref}) or (2) to derive application-specific "effective" design rules $j_{\text{max,eff}}$ at T_{eff} (see Fig. 4). These use cases and operating phases are defined in so-called "mission profiles". A mission profile describes and links all environmental and operating conditions as well as functional loads which an application has to sustain during production, storage, shipping, assembly and operation [14, 24]. For EM, the combinations of ambient temperature and the cumulated duration (e.g., 1000 h at 398 K + 300 h at 423 K) describe the relevant environmental conditions, whereas the terminal currents of a net represent functional loads.

The general approach for deriving "effective" design rules ($j_{\text{max,eff}}$ at T_{eff}) for a particular layer is given as follows. The technology characterization provides the models and factors to scale the permitted current-density limit under consideration of reliability goals (CDF, lifetime) and varying operating temperatures (JESD63, JESD202 [13]). First, the particular temperatures and durations of all operating phases are used to calculate an EM-specific *effective* temperature T_{eff} using Black's Equation [6]. Second, the *effective* current-density limit $j_{\text{max,eff}}$ at T_{eff} is then derived from the reference conditions $j_{\text{max,ref}}$ at T_{ref} using the given or derived EM-failure model scaling factors. This approach ensures that the statistical number of interconnect failures due to EM are identical for the application-specific use cases and the technology-specific reference conditions.

The detailed procedure to derive and scale current-density limits is beyond the scope of this tutorial paper due to space limitations. The procedure and the general mission-profile-aware design approach is discussed in detail in [14] and [19].

3.2 EM-Aware Layout Design in Industrial Practice

In general, layout designers consider EM requirements through sufficient dimensioning of interconnect widths and using adequate via numbers with respect to maximum allowable values of current density and specified chip temperature. However, the optimal solutions are not always obvious in real layouts. This subsection provides some useful advices on how to improve the EM robustness of metallization patterns in typical layout situations. While the examples consider analog layout (where manual intervention is common), most of the advices are applicable to digital layout patterns as well.

First, we want to raise the attention on inhomogeneous current flows, which always happen if currents have to change their direction. This leads to unequally distributed current densities over the cross section of an interconnect, causing locally increased current densities.

Interconnects are "drawn" in horizontal and vertical directions in typical routing structures. For changing the direction within one metal layer, the interconnects have to be bent. The current density in the corners of such bends shows an increase by a factor K compared to the homogeneously flowing current in a straight interconnect, as illustrated in Fig. 5. Due to limited accuracy of patterning techniques, corners are (fortunately) not sharp, but exhibit a certain rounding. Analytical calculations (based on conformal mapping) in [8] and [9] show that K depends (1) on the angle of the bend and (2) on the normalized rounding radius $R = r/w$, where r is the rounding radius and w the interconnect width. Based on the formula for right-angled bends and values of $r \ll w$ from [9], the factor K_{90} can be approximately quoted to 3, 6, and 13 for $R = 0.1, 0.01$, and 0.001, respectively. If minimal interconnect widths are used (as in digital circuits), K_{90} can be assumed to be smaller than 3, because we are there in the scale of the technology feature size and thus an $R > 0.1$ can be expected.

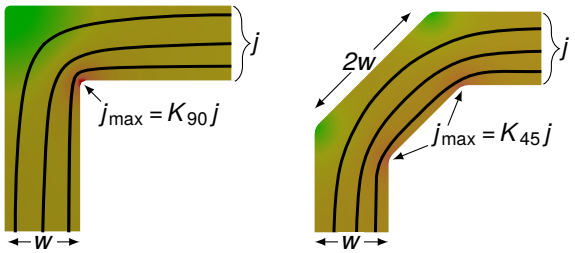


Fig. 5: Increase of current densities in interconnects bent in angles of 90 degrees (a) and 45 degrees (b). The current density *j* is indicated by the distance of current flow lines (in black) and the shading from green (low *j*) to red (high *j*).

The discussed current-density increase must be taken into account if the dimensioning of an interconnect width must be close to the EM-critical value. This is especially critical for power lines, which can have extensive widths and thus very small $R < 0.01$. A significant improvement can be achieved by inserting an intermediate diagonal step into the bend as shown in Fig. 5b. Applying the method presented in [8], it can be seen that the factor $K_{45}(R)$ is reduced to about half of $K_{90}(R)$. We recommend to size the length of the diagonal path segment at least twice as long as the width w. Otherwise, the desired effect cannot be achieved. If this measure cannot lower the current density sufficiently, the corner should be rounded manually with $R \approx 1$.

If the change from vertical to horizontal interconnect direction is (1) combined with a change of the metal layer and (2) the total current requires a via array, a similar problem can occur. Vias are uniformly shaped in today's technologies. Thus, a maximum allowable current $i_{\text{via,max}}$ for one via can be enforced in order to ensure EM-robustness. If a via array of n vias is located directly at the crossing of the horizontal and vertical interconnects as shown in

Fig. 6a, the layout designer should be aware that the "innermost" via has to conduct a multiple of the total current divided by n. This can easily lead to an EM problem if the layout designer has erroneously assumed that a number of n vias is enough for a total current of $n \times i_{\text{via, max}}$. Therefore, a number of redundant vias should be spent as shown in Fig. 6b. If there is not enough space for an enlarged via array, the change of layers and directions should be uncoupled as shown in Fig. 6c. In this solution, the current is distributed uniformly over the via array because the current paths through all vias have similar lengths and, thus, similar overall resistances.

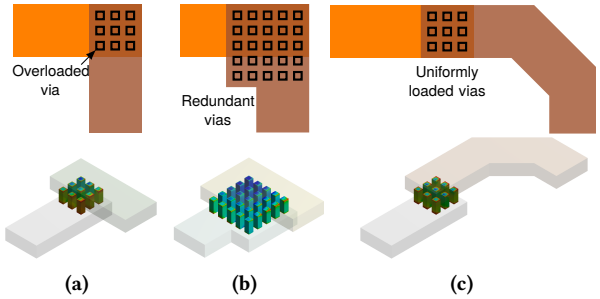


Fig. 6: Via arrays (black) connecting two neighboring metal layers (orange and brown). If this array connects perpendicularly arranged interconnects, the "inner" via(s) can be affected by EM through current overload (a). EM robustness can be achieved by enlarged via arrays (b) or by placing the via array such that the current does not change the lateral direction (c).

Our third example shows that even the often followed rule of thumb "the more metal and vias, the better" can sometimes be misleading due to EM. Figure 7 illustrates two MOS transistors T_1 and T_2 sharing the same source potential. Their source currents I_1 and I_2 are led away in an upper metal layer (metal 2 in brown), which might have a lower sheet resistance. The total current $I_1 + I_2$ flows to the right as indicated by the arrows. In case (a), the two sources are connected using as much as possible metal 1, vias, and metal 2 areas. However, the result of this layout is that a remarkable portion of I_1 is flowing through the metal 1 source pin of T_2, which is in parallel to the metal 2 line. This can exceed the EM critical value of metal 1 causing EM damage. This problem is mitigated in case (b) by punching out metal 1, vias and metal 2 between the two source pins of T_1 and T_2. This leads to a routing of T_1 and T_2 where the upper right metal 2 region acts as star point, collecting the separated currents I_1 and I_2.

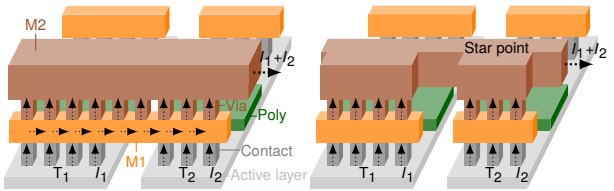


Fig. 7: Two MOS transistors with common source potential. In (a), the current of T_1 partly flows through the metal 1 layer of T_2's source pin, causing an EM risk there. Cutting out metals and vias between the source pins enables a star routing constellation, reducing the problem in (b).

4 INTERACTION OF THERMAL EFFECTS, THERMAL MIGRATION AND ELECTROMIGRATION

Temperature is strongly influencing the different migration mechanisms in metal material. The probability of issues due to thermally activated migration effects becomes more prominent with ongoing technology development [1]. Areas with increased local temperature suffer from higher probability of dislocation than cooler areas.

One important aspect is temperature gradients within interconnects. Significant temperature differences drive the effect of TM, which is a material migration towards cooler temperature regions. The root cause for a temperature gradient, on one hand, is internal Joule heating in the metal interconnects, due to the current flow and a non-zero resistance. On the other hand, external heat sources or sinks contribute to the gradients due to power dissipation in the active devices or nearby cooling metal, like thermal vias and thorough-silicon vias (TSVs).

Even uniformly distributed heating may cause issues due to different coefficients of thermal expansion (CTE mismatch), as this leads to mechanical stress gradients that induce SM.

Local temperatures are also of central influence for the EM effect as the required activation energy needed to dislocate atoms is lowered at higher temperatures. Therefore, the maximum permissible current density drops down by a factor of 10 when increasing the temperature by 100K [19] (Fig. 8).

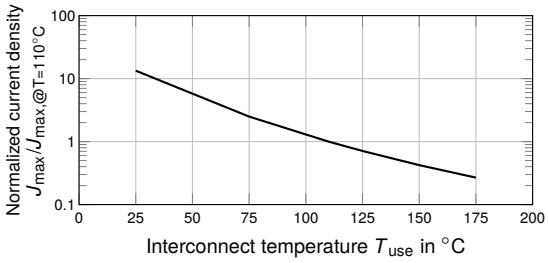


Fig. 8: Temperature dependency of the maximum current density of an AlCu interconnect structure, normalized to a maximum current density initially determined at 110°C.

Lloyd [23] suggested two separate current density exponents n in Black's equation [6] for the two different mechanisms, void nucleation and void growth. Hauschildt et.al. [10] found that both exponents show individual thermal characteristics.

TM and EM are characterized by complex mutual dependencies, as depicted in Fig. 9. Current density and the resulting temperature increase directly amplify EM. Thermal gradients induce TM, leading to differences in the atomic concentration. Thereby TM indirectly influences EM as another source of material migration. As a result, TM and EM may either self-amplify or compensate each other, depending on the initial driving force(s).

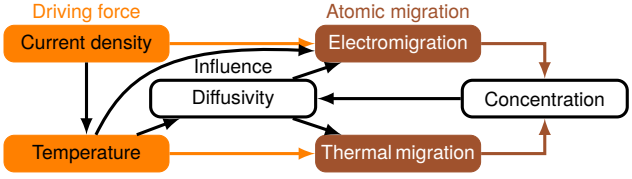


Fig. 9: Mutual dependencies and influences of EM and TM.

Increased local heating directly results from higher device density due to smaller technology nodes. It also corresponds to higher power density if voltage and current levels are not decreased at the same amount as the technology shrinks. New device types, like FinFETs, gate-all-around, and nanowires, hinder heat removal from the active devices. Using buried oxides as an alternative technology path to minimize leakage currents also prevents heat dissipation through the substrate and, hence, increases interconnect temperature. The same is true for advanced packaging technologies, like flip-chip, where heat has to be transported through the metal stack to heat sinks on the PCB, or 3D integration where heat might be trapped in the die stack, resulting in local overheating.

Predicting accurate local temperatures and gradients at different heights of the technology stack is therefore crucial for a meaningful assessment of failure probability. Ideally, this evaluation is carried out "full chip" in order to identify thermal hot spots, determine mutual electro-thermal interactions, and calculate the overall failure rate. Moreover, this allows assessing the on-chip temperature distribution based on realistic application scenarios as well as thermal boundary conditions of the package. The awareness for these topics is currently increasing. However, true thermal simulation at chip level, coupled with an electrical simulation and including package level conditions, is not yet part of today's design flows.

5 METHODS FOR EM-AWARE DESIGN IN FUTURE TECHNOLOGY NODES

Shifting from a traditional (post-layout) EM verification towards a robust (pro-active) EM-aware design requires adjustments and new approaches for the various physical design stages. This section provides some potential EM countermeasures, focusing on routing methodologies that designers can apply to increase the EM robustness of the layout.

5.1 Towards a Robust EM-Aware Design

As one can see from history, EM has already endangered the IC future once, when aluminum was the main interconnect material. At that time, EM problems were solved by a technology change (alloying the aluminum interconnects with copper) [22]. However, such a technology change remains very expensive, hence layout solutions are preferred. This is why the electronic design automation (EDA) community has a good potential to reduce costs and improve sustainability by compensating EM.

Nowadays, EM is only addressed if EM violations are detected in the verification step. However, post-layout repairs of these violations are becoming too time consuming. Therefore, a shift is needed from "verify" to "create" EM-robust solutions for critical nets. (Nets with the highest currents and longest wire lengths are considered *critical nets*.)

EDA tools have been able to include timing or manufacturability aspects in physical design for many years. The next needed functionality is a hardening of layouts against EM. This functionality probably requires additional die area or routing resources. However, this is worth the price to ensure reliable ICs in future, as it is still cheaper than frequently failing electronic devices. Nevertheless, any EM countermeasures should not simply be applied to all nets, but only to the most critical.

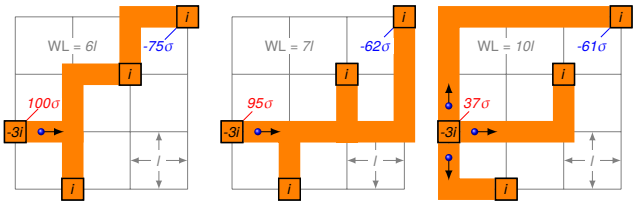
Especially, the placement and routing steps have a high potential of generating EM-robust solutions because they strongly influence the EM parameters, temperature, interconnect geometry, and current density [3].

In the placement step, one could reduce the wire length of critical nets to mitigate EM, as a shorter net has a higher chance to generate a low-stress solution in the subsequent routing step. Another opportunity is to move critical cells out of hot temperature regions because high temperatures amplify the EM impact.

An obvious solution for EM-aware routing would be to increase the interconnect width, which, however, would counteract interconnect shrinking. Hence, we propose to focus on the reservoir and length effects (see Sec. 2.2), as well as the increased EM-robustness of special via configurations. An extended investigation of these effects follows in the next section helping to understand the benefit of each of the proposed routing methodologies.

5.2 EM-Aware Routing Methodologies

Net topologies: Nowadays, the rectilinear Steiner minimum tree (RSMT) and trunk tree are the main net topologies used in routers to minimize both the wire length (WL) and routing congestion. However, net topologies can be further optimized regarding EM robustness by reducing EM-induced stress [5]. Obviously, these solutions need more routing resources than the traditional ones. Figure 10 contains examples of three different net topologies, each characterized with stress (σ) and WL.



(a) (b) (c)

Fig. 10: A four-pin net containing one output driving three inputs with current *i*. The RSMT net topology in (a) results in the lowest WL, but highest stress. The trunk net topology in (b) enables slightly less stress than (a) but increases the WL. The net topology in (c) leads to the greatest EM robustness (i.e., the least stress) but results in the longest WL.

Reservoirs: Reservoirs are known to influence EM. However, their principle physical behavior is often misunderstood. Figure 11 visualizes with three examples the influence of reservoirs on the EM-induced stress within the interconnect in the steady-state condition. The following basic rules can be derived from Fig. 11 and applied when handling reservoirs:

(a) Reservoir locations affected by tensile (compressive) stress shift the interconnect stress towards compressive (tensile) stress,
(b) the higher the interconnect stress at the reservoir location, the greater the shift of the interconnect stress caused by the reservoir, and
(c) the longer the reservoir, the greater the shift of the interconnect stress.

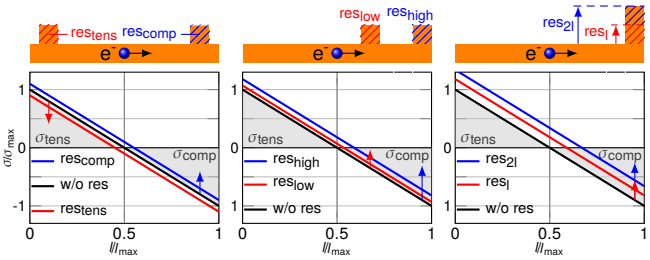


Fig. 11: (a) The shift of the interconnect stress caused by a reservoir (res) depends on whether tensile (tens) or compressive (comp) stresses occur at the reservoir location. The shift of the interconnect stress increases with the stress at the reservoir location (b) and the reservoir length (c).

Length limitations: The limitation of the interconnect length can be very effective to avoid EM damages. Usually, the goal is to divide a long interconnect into several short interconnects below the Blech length (see Sec. 2.2) as shown in Fig. 12. Therefore, all segments become "EM immortal," thus, preventing the formation of voids or hillocks. The disadvantage is that much more routing resources are needed due to the additional layer changes.

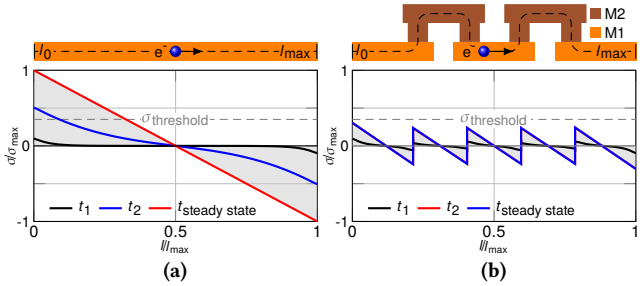


Fig. 12: (a) Stress within an interconnect on a single routing layer, cf. Fig. 3. (b) Dividing the interconnect from (a) into several small interconnects below the Blech length is keeping their stress levels below the critical EM threshold.

The high demand for routing resources can make the use of only short segments impracticable. An alternative approach is to balance the length per routing layer. This saves routing resources and compensates for the load on each part of the connection, as shown in Fig. 13.

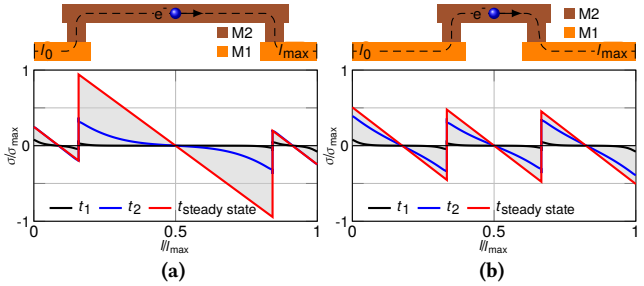


Fig. 13: The unbalanced lengths between routing layers in (a) causes greater stress than the balanced interconnect lengths in (b) with the latter not increasing the demand for routing resources as in Fig. 12.

Cross-section widening: The reduction of EM-induced stress by increasing the interconnect cross section might be an obvious solution as it reduces the driving force of EM, i.e., current density. Unfortunately, this counteracts the desired shrinking of the IC structures. One way of using this effect without counteracting the structural reduction is to exploit the different interconnect dimensions within a metal stack. Usually, higher routing layers (e.g., M8) use larger cross sections than lower ones (e.g., M1). The aim here is to shift EM-critical interconnects to higher routing layers in order to reduce the current density and, thus, the EM-induced stress. This can significantly reduce the stress and, therefore, improve the EM-robustness, requiring only few additional routing resources (Fig. 14).

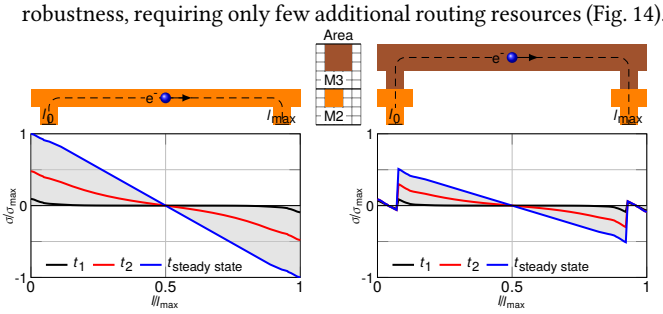


Fig. 14: (a) Stress within an interconnect on a routing layer with a relatively small cross-sectional area. (b) Stress reduction within the interconnect of (a) when shifted to a higher layer allowing a larger cross-sectional area.

Redundant vias: The initial objective of redundant via insertion is to insert as many vias as possible. In order to harden layouts against EM, the objective should be expanded by the stress-related consequences of the insertion [4] because interconnects under high stresses tend to fail earlier than interconnects under lower stresses. For this reason, interconnects under high stresses benefit more from redundant vias than interconnects under low stresses (Fig. 15).

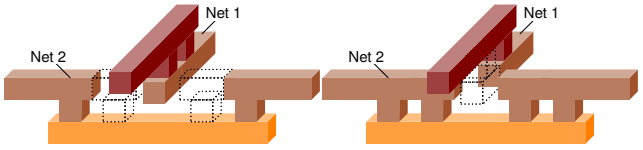
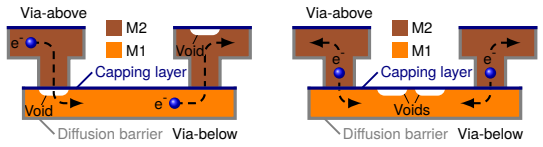


Fig. 15: (a) One redundant via inserted in net 1 blocks redundant vias of net 2 due to spacing rules. (b) Two redundant vias inserted in net 2 hinder an insertion in net 1. Consequently, if net 1 experiences greater stress than net 2 (and, hence, net 1 is more likely to suffer from EM damage), solution (a) should be preferred to solution (b) (and vice versa).

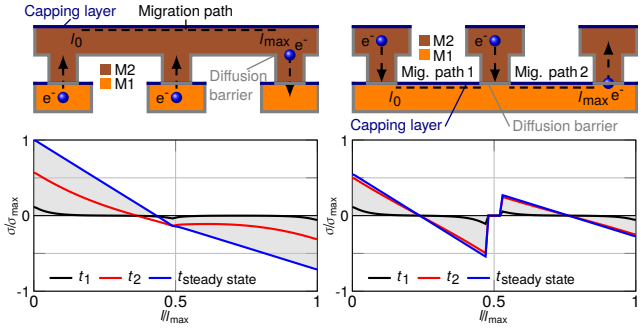
Via-above and via-below configurations: As mentioned in Sec. 2.2, via-below configurations enable a longer lifetime than via-above configurations because the critical void volume is significantly larger in via-below configurations. In the dual-damascene technology, voids are mainly formed between the interconnect and its capping layer. Therefore, direct currents (e.g. in power nets) form voids well above or directly below vias (Fig. 16a). However, alternating currents (e.g. in signal nets) form voids close to the middle of interconnects [21] eliminating the difference between via-above and via-below configurations (Fig. 16b).



(a) (b)

Fig. 16: (a) Via-below configurations enable a greater critical void volume than via-above configurations in case of direct currents. (b) Via configurations are not relevant when applying alternating currents due to the void location(s) in the middle range of the interconnect.

Upper and lower lead: A countermeasure against EM for both direct and alternating currents are additionally introduced diffusion barriers from vias connecting the interconnect "from above". The authors in [25] show that lower leads (interconnect contacted by vias from above) allow a longer lifetime than upper leads (interconnect contacted by vias from below), as show in Fig. 17. The reason is that the migration of atoms mainly occurs between the capping layer and the interconnect in the dual damascene technology. Therefore, a via from a routing layer above interrupts this main migration path, resulting in an lower stress profile and an increase of EM robustness (see Fig. 17b). Consequently, an insertion of additional vias from higher routing layers increases the robustness of the underlying interconnect. This effect is independent of whether these vias carry current or not. Therefore, this methodology needs only a few additional routing resources to mitigate EM.



(a) (b)

Fig. 17: (a) The upper lead case results in greater stress than the lower lead case in (b) because the main migration path is blocked by the via diffusion barrier in (b).

6 SUMMARY

According to current forecasts, up-to-date technologies are only partially reliable against the expected circuit degradation caused by electromigration. Even worse, future technologies smaller than 8 nm will be completely unreliable if effective countermeasures are not put in place in time [12]. EM-aware IC design methodologies are therefore required in future technology nodes.

The objective of this tutorial has been to present measures that can be exploited in present and future technologies in order to curtail the negative impact of electromigration on circuit reliability, and overcome an increasingly severe VLSI problem.

After introducing the fundamentals of EM and its mitigating effects in physical design, we presented how EM-aware design rules can be determined and discuss application examples of EM-robust metallization patterns. Furthermore, IC designers must be especially aware of thermal effects and thermal migration; both have been introduced and investigated as well. Finally, we presented methodologies for layout synthesis, which are EM robust by construction, in order to support shifting from a traditional (post-layout) EM verification towards our goal of an EM-aware design methodology.

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