Fakultät Elektrotechnik und Informationstechnik
Institut für Feinwerktechnik und Elektronik-Design

TECHNISCHE UNIVERSITÄT DRESDEN

Einladung zum Gastvortrag

Thema:	**Voronoi Diagram-based Multiple Power/Ground Plane Generation on Redistribution Layers in 3D IC**
Vortragender:	**Prof. Mark Po-Hung Lin, National Yang Ming Chiao Tung University (NYCU), Taiwan**
Leitung:	**Prof. Dr.-Ing. habil. Jens Lienig**
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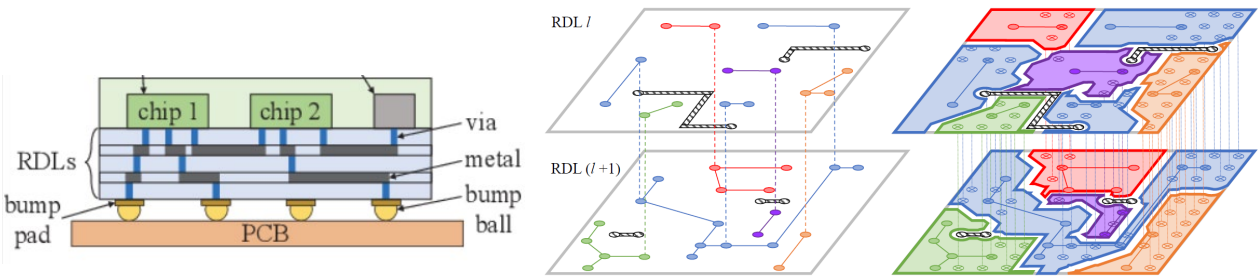
In 3D ICs, the interconnection design among chiplets on redistribution layers (RDLs) is crucial for achieving high-performance computing systems. To optimize the inter-chip connections, most of the previous works focused on automatic signal net routing and pin assignment. The power/ground plane generation is still a manual and time-consuming task, especially when generating the power planes of more than ten power supplies on a limited number of RDLs.

This talk introduces a novel Voronoi diagram-based multiple power/ground plane generation methodology that simultaneously optimizes the power/ground planes of all power/ground nets by utilizing the white space of given RDLs, while considering the signal routing blockages, power integrity, and complex design rules. Experimental results show that the presented approach can achieve not only optimal area utilization but also the best cross-layer power integrity in terms of the total number of redundant vias.



Mark Po-Hung Lin received the B.S. and M.S. degrees in the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University (NCTU). He received the Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University (NTU). He is currently a professor with the Institute of Pioneer Semiconductor Innovation, Industry-Academia Innovation School (IAIS), and the Institute of Electronics, College of Electrical and Computer Engineering (ECE), NYCU.