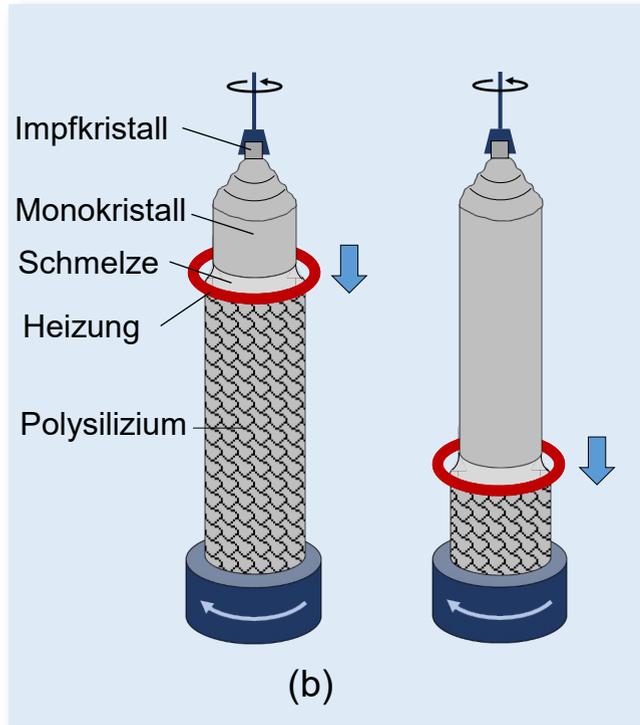
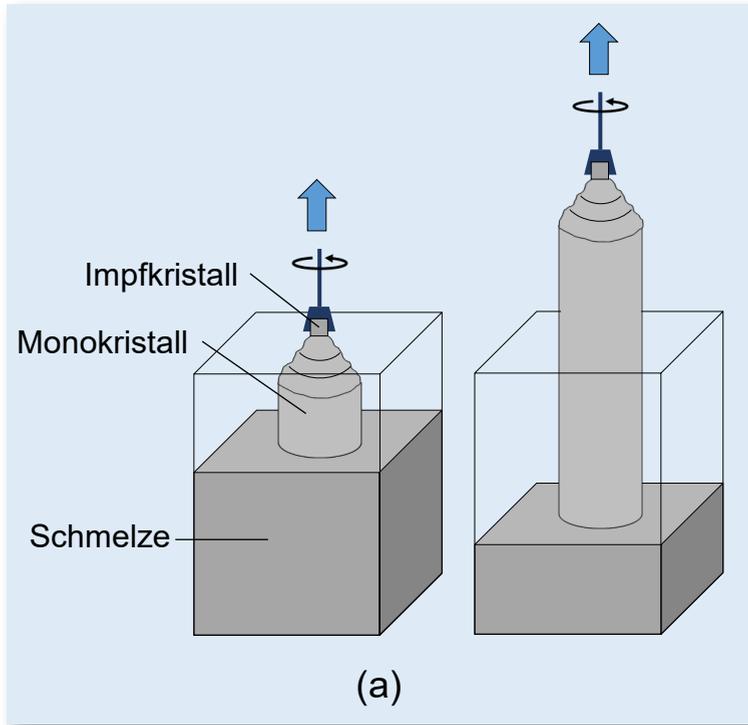
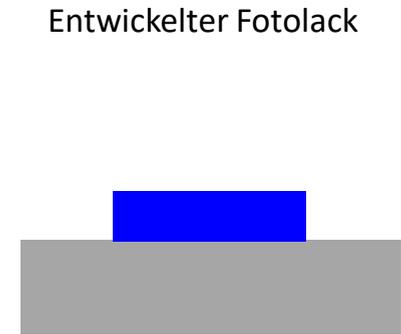
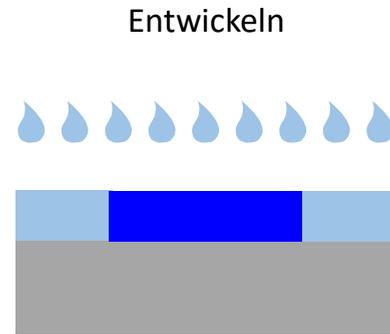
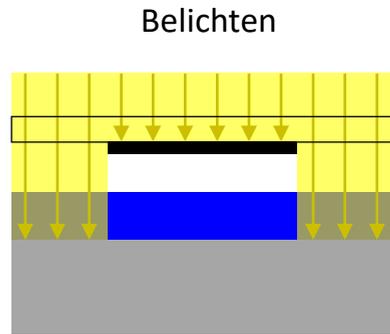


- 2.1 Grundprinzip der IC-Fertigung
- 2.2 Grundmaterial Silizium
- 2.3 Fotolithografie
- 2.4 Abbildungsfehler
- 2.5 Auftragen und Strukturieren von Oxidschichten
- 2.6 Dotierung
- 2.7 Aufwachsen und Strukturieren von Siliziumschichten
- 2.8 Metallisierung
- 2.9 Funktionsprinzip des Feldeffekttransistors
- 2.10 CMOS-Standardprozess





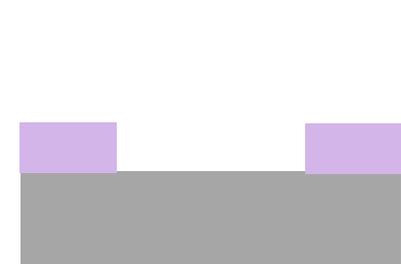
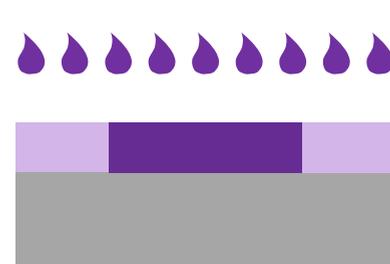
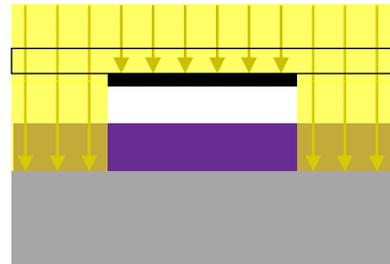
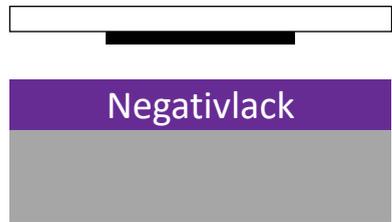


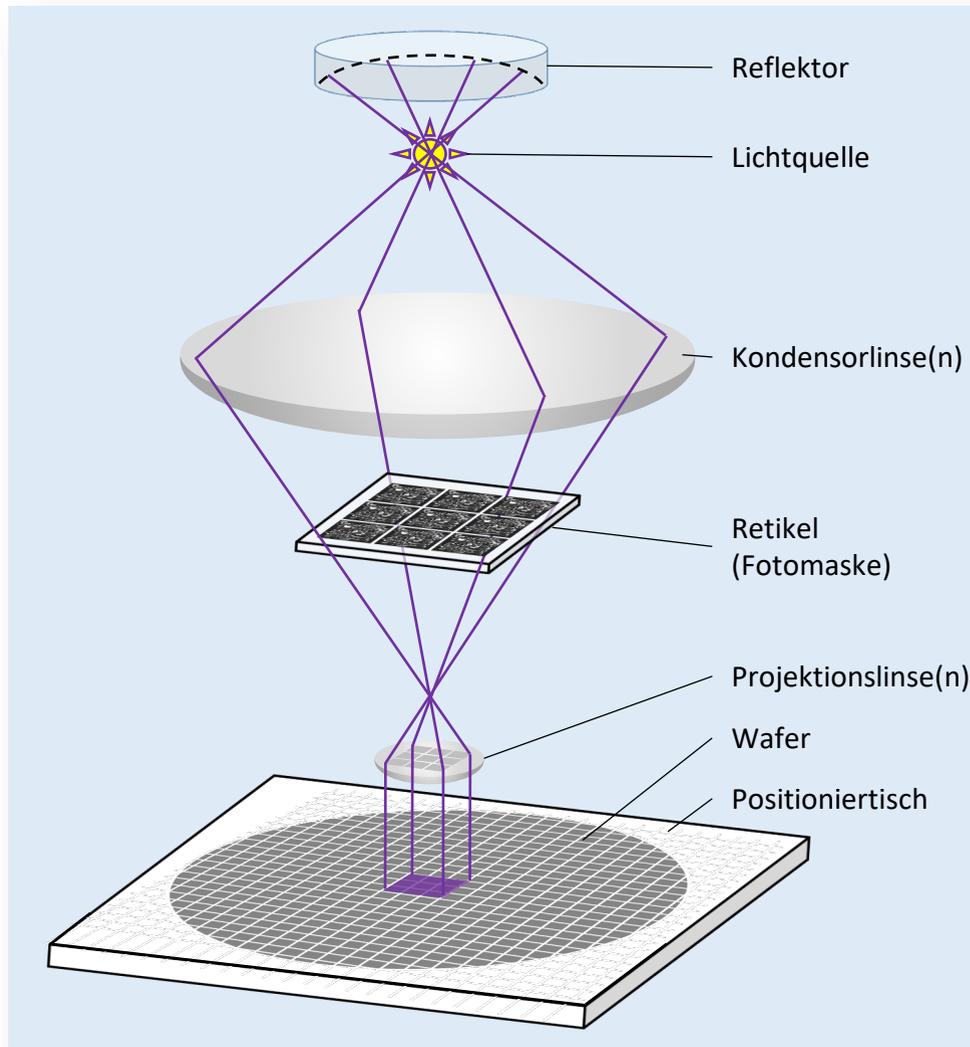
(a)

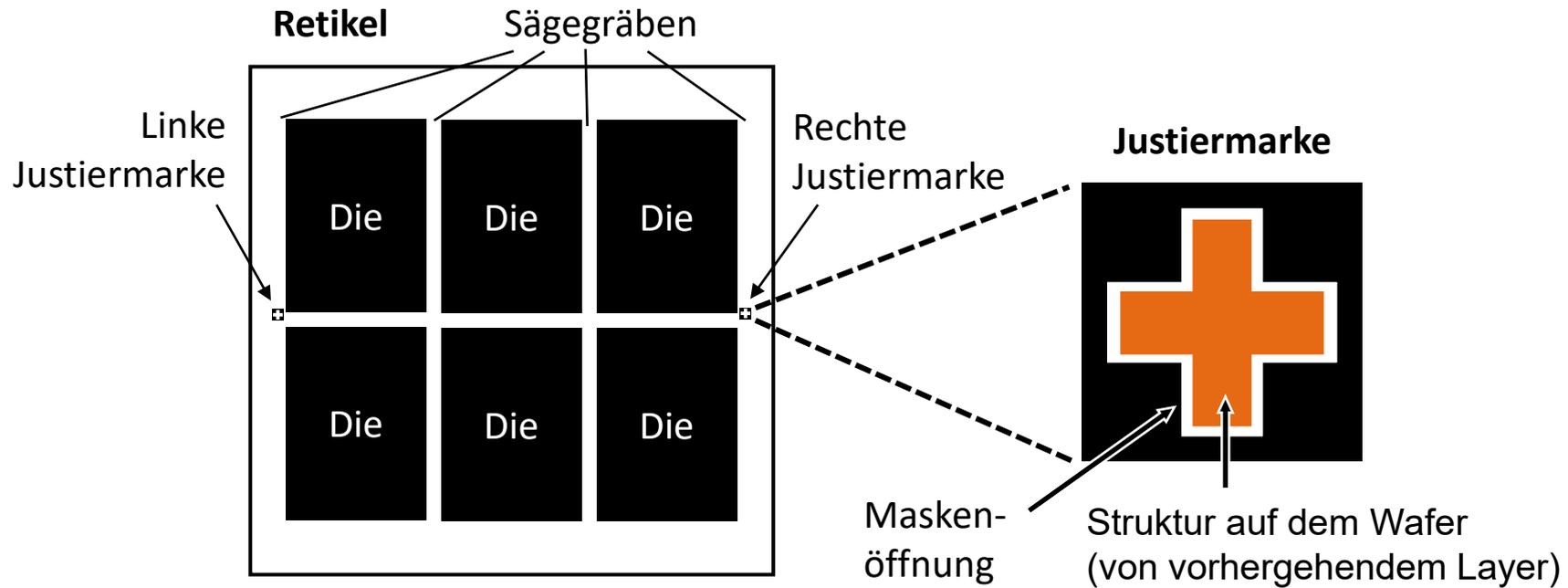
(b)

(c)

(d)

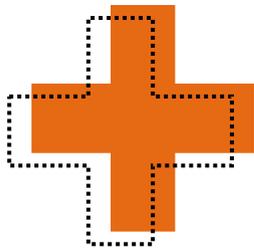






Layer 1

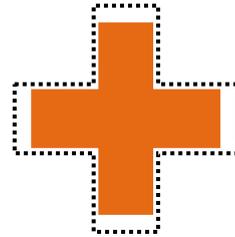
Layer 2



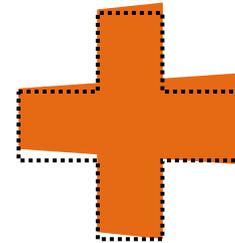
(a)



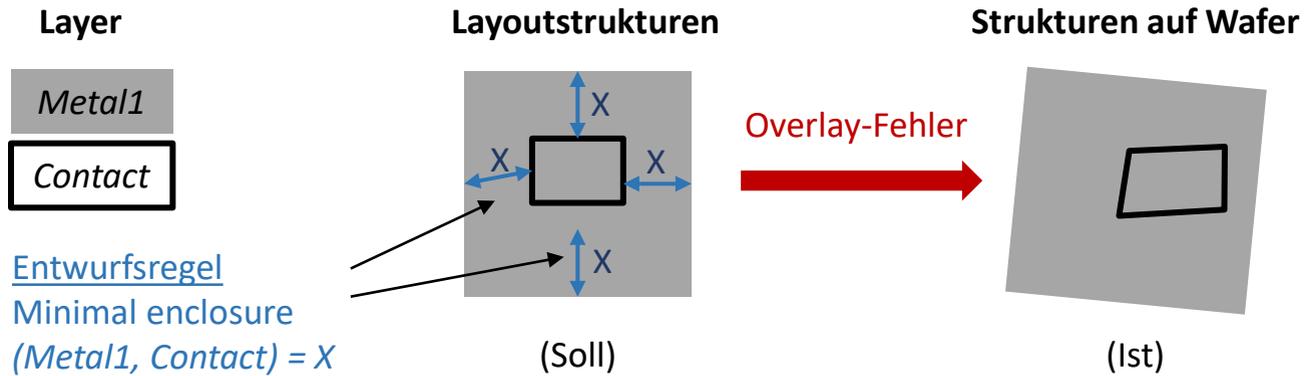
(b)



(c)



(d)



Struktur im Layout

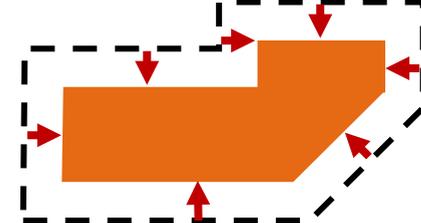
Struktur auf Maske

Struktur auf Wafer

(a)



Kopie
→

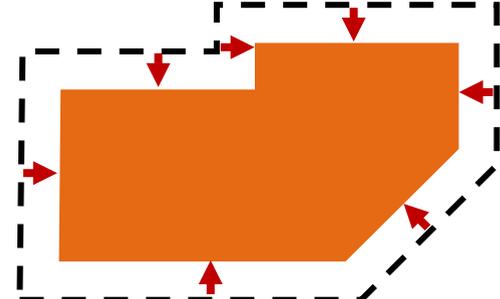
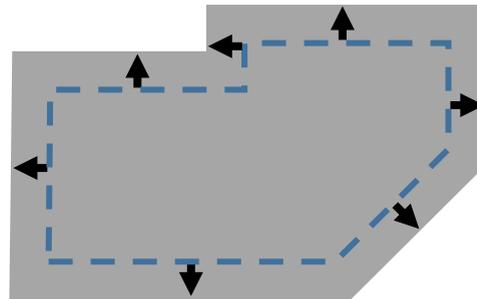


wird kleiner als im Layout

(b)

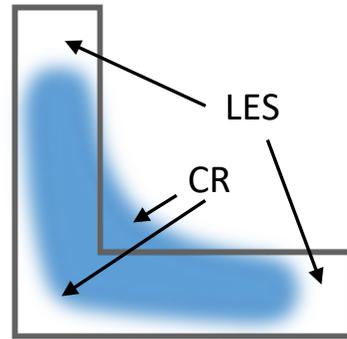
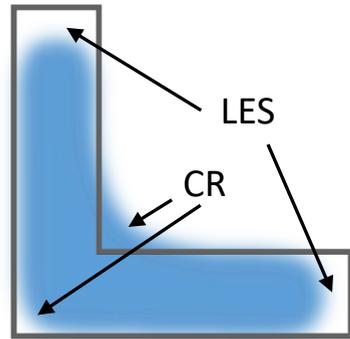
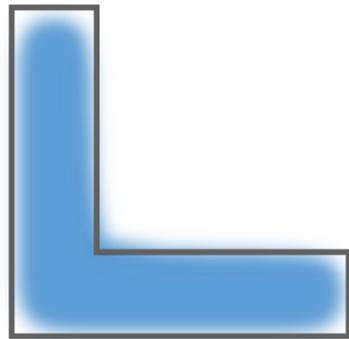


Oversize
→



wird gleich wie im Layout

Abnehmendes Verhältnis $\frac{\text{Strukturgröße}}{\text{Wellenlänge}}$



Gewünschte Layoutstruktur

Struktur in Fotoresist

Beugungseffekte:

„Line end shortening“ (LES)

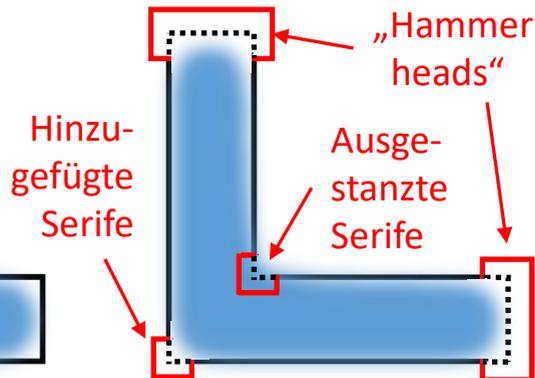
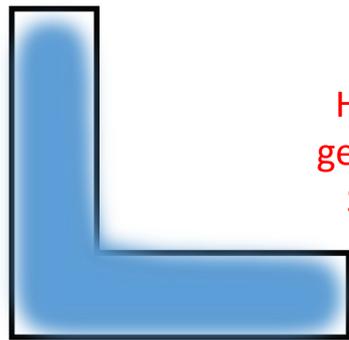
„Corner rounding“ (CR)

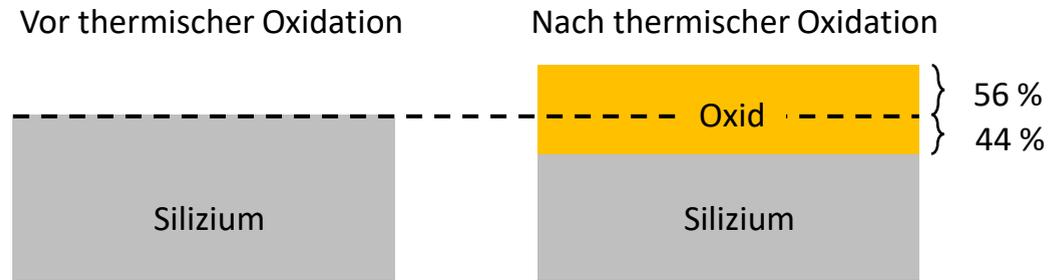
Optical proximity correction (OPC)

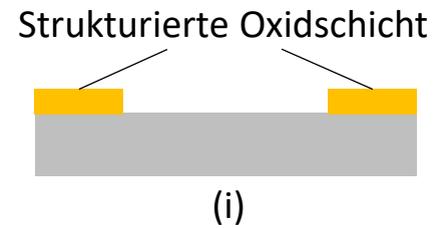
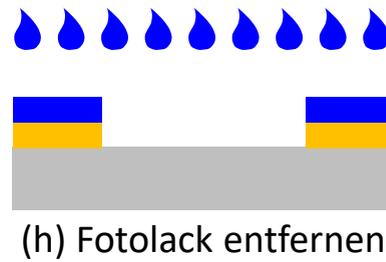
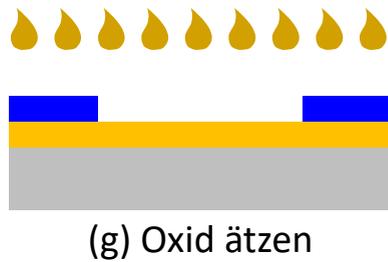
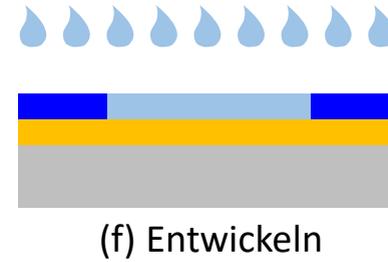
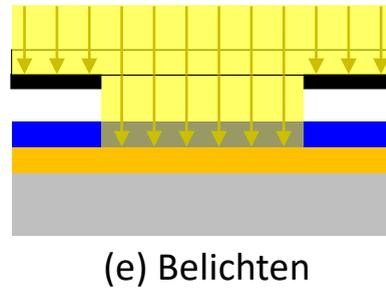
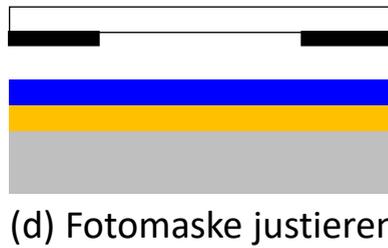
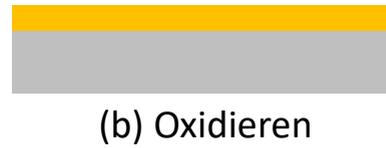
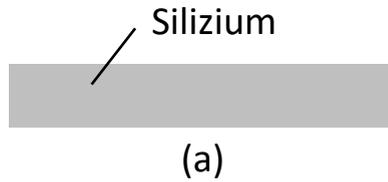
Keine OPC

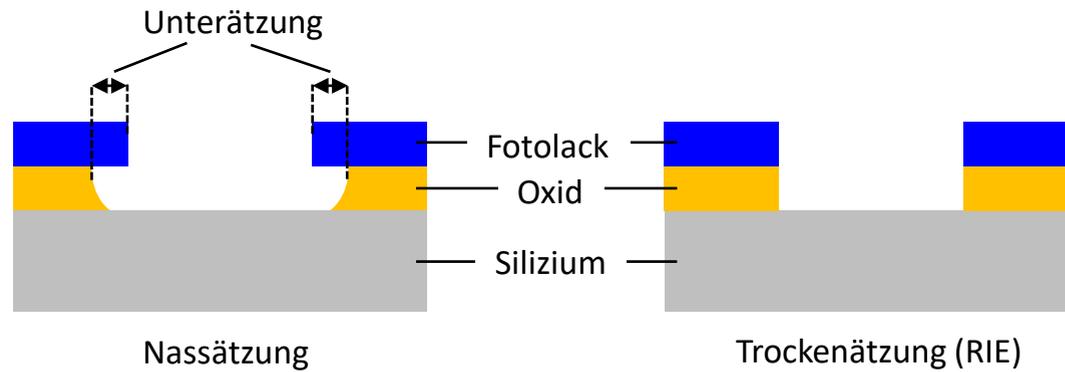
Regelbasierte OPC

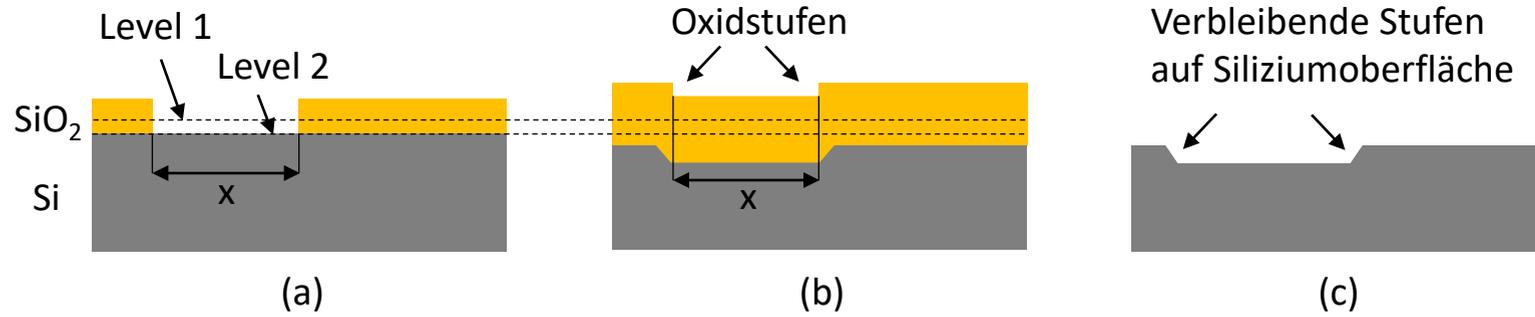
Modellbasierte OPC

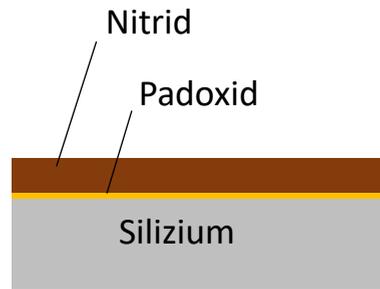








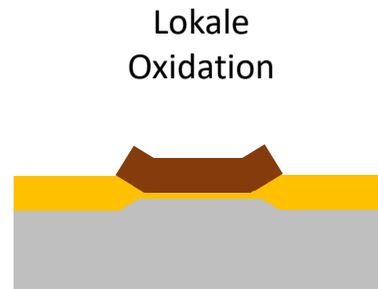




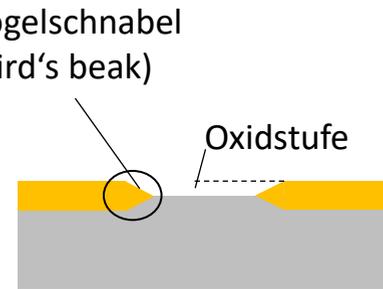
(a)



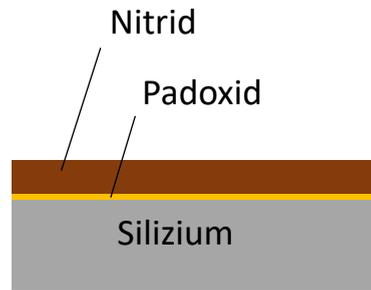
(b)



(c)

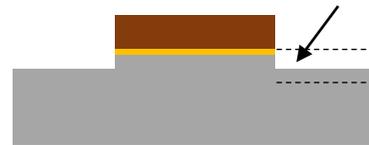


(d)



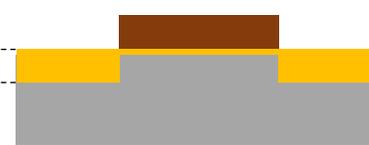
(a)

Strukturierte Nitridmaske
Silizium um 56% der
Oxidschichtdicke abtragen



(b)

Lokale
Oxidation

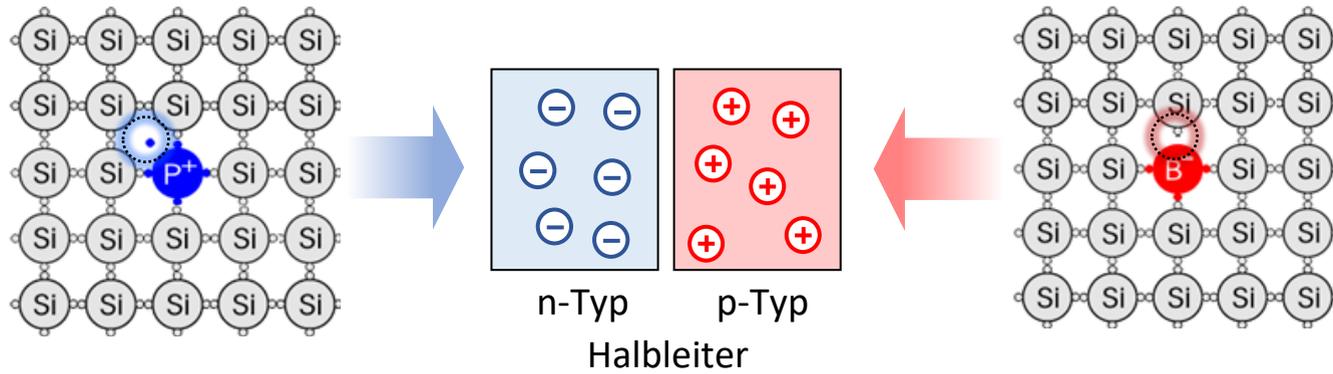


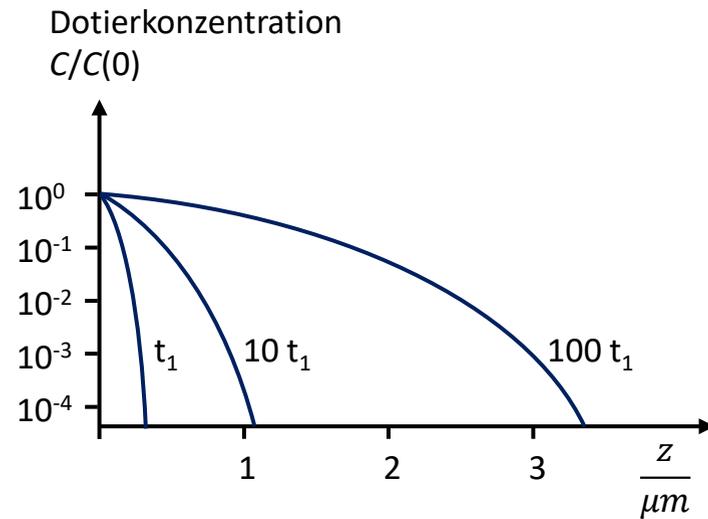
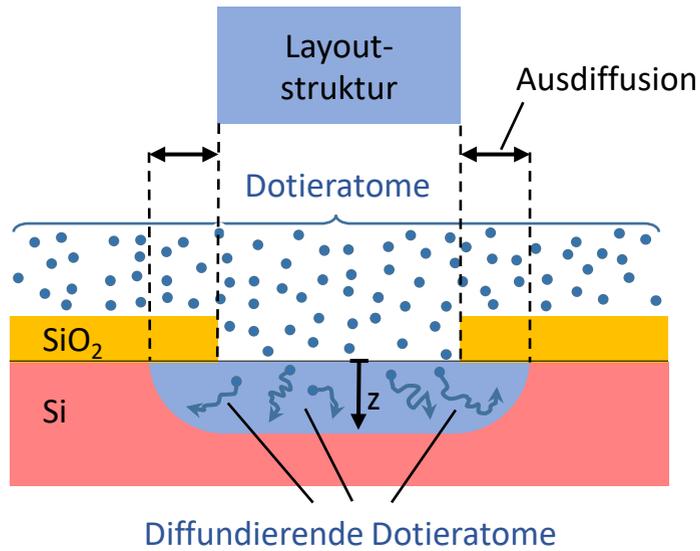
(c)

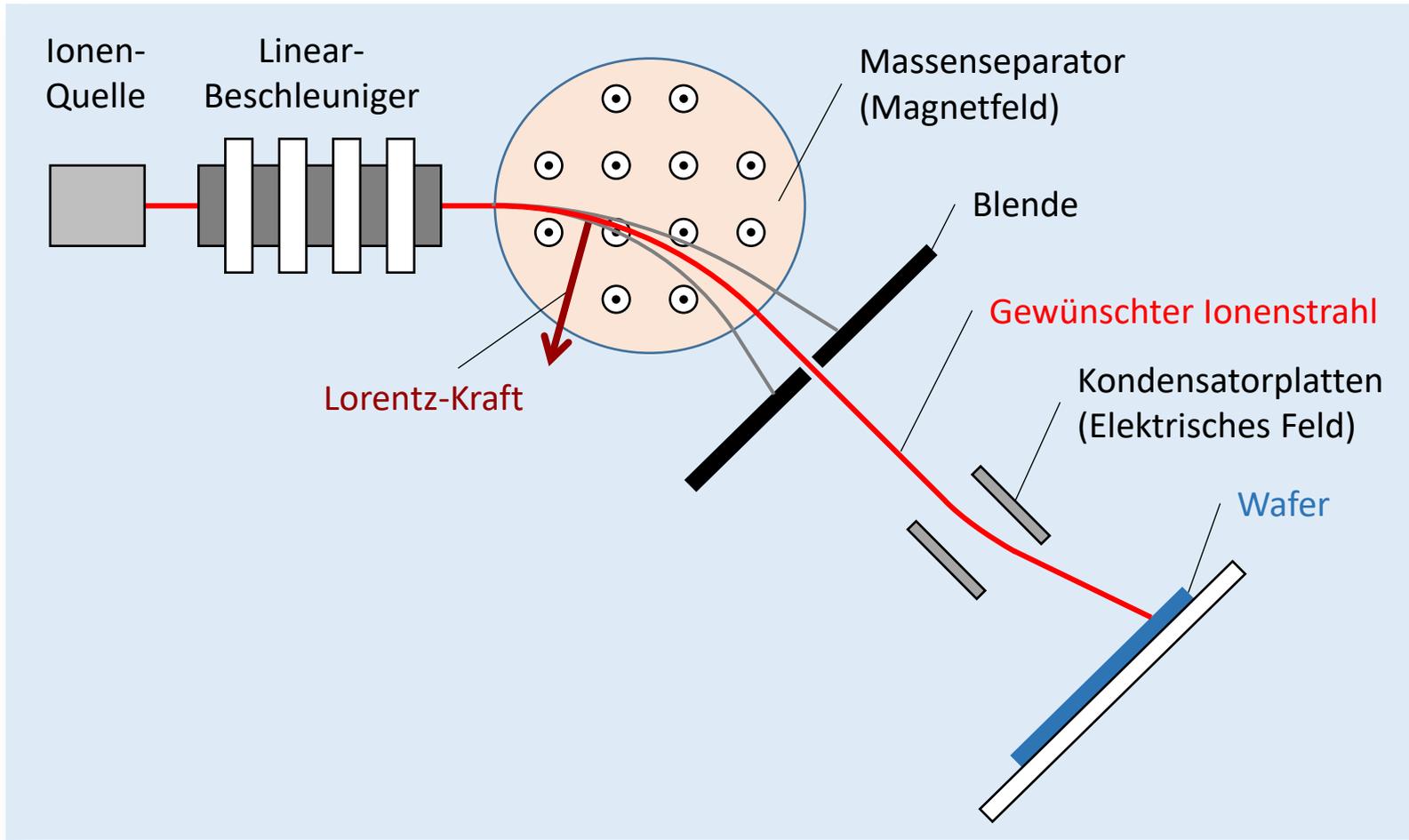
Nitrid entfernen
Oxid blankätzen

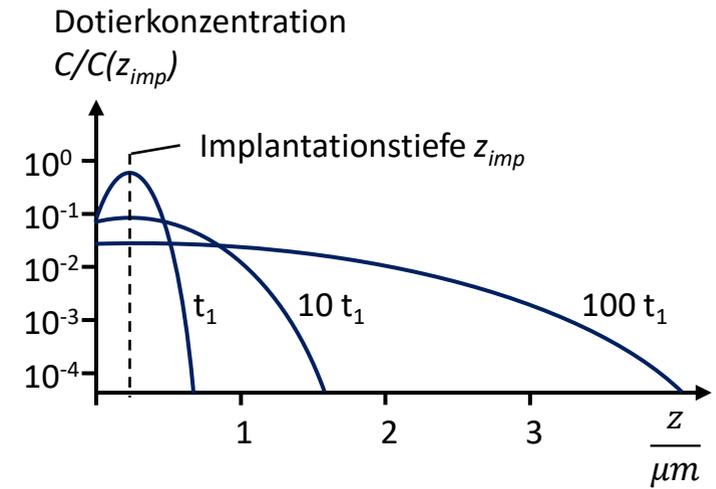
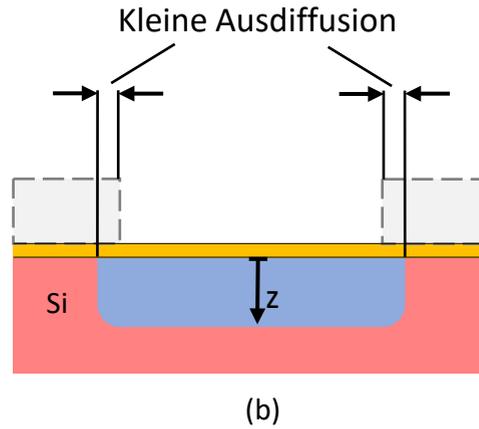
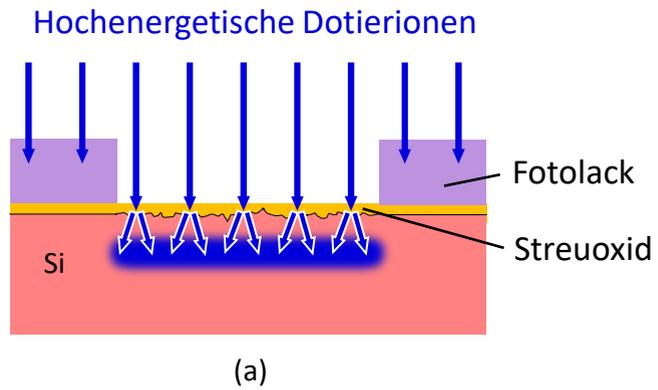


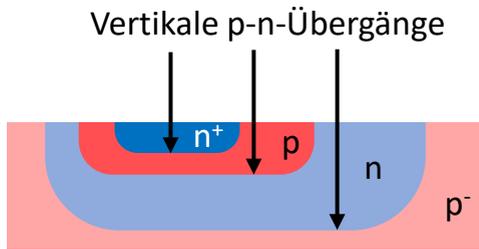
(d)



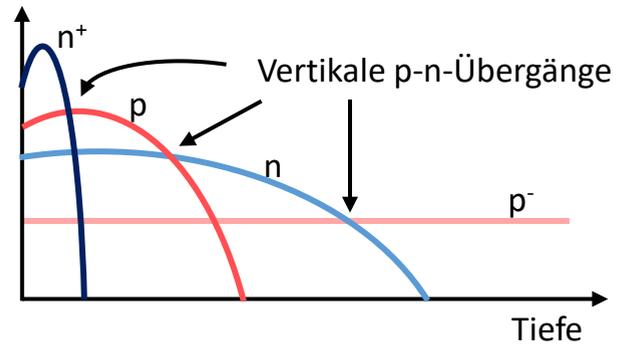


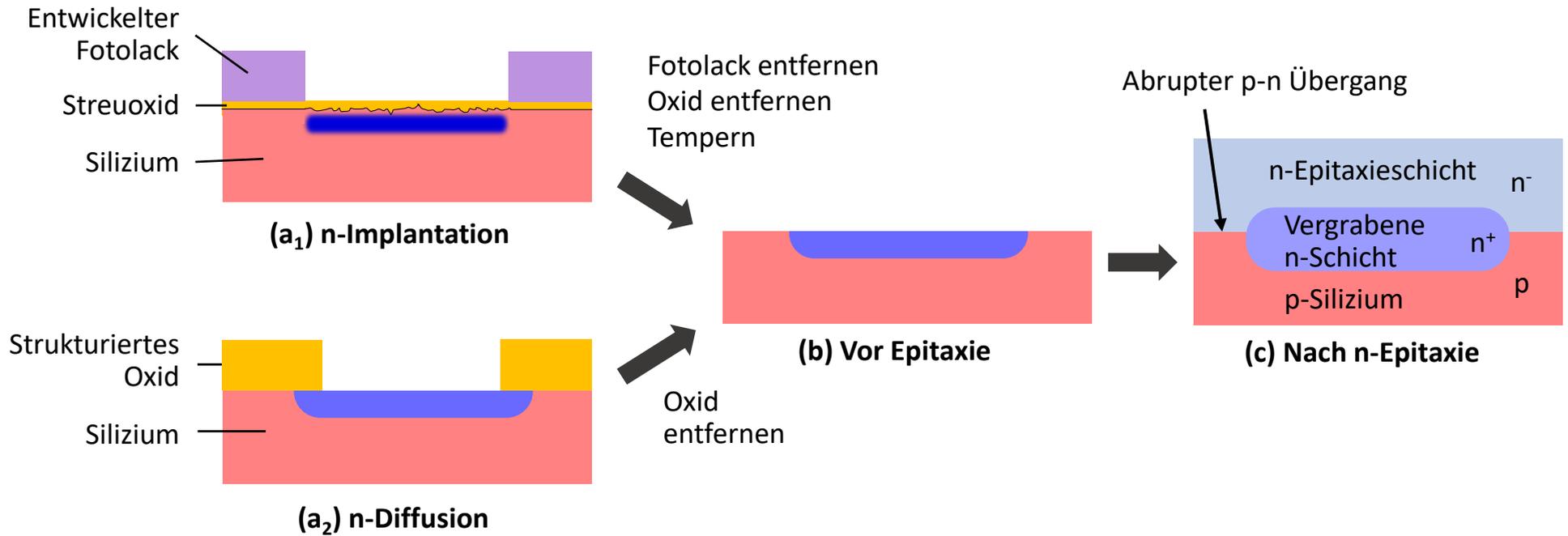


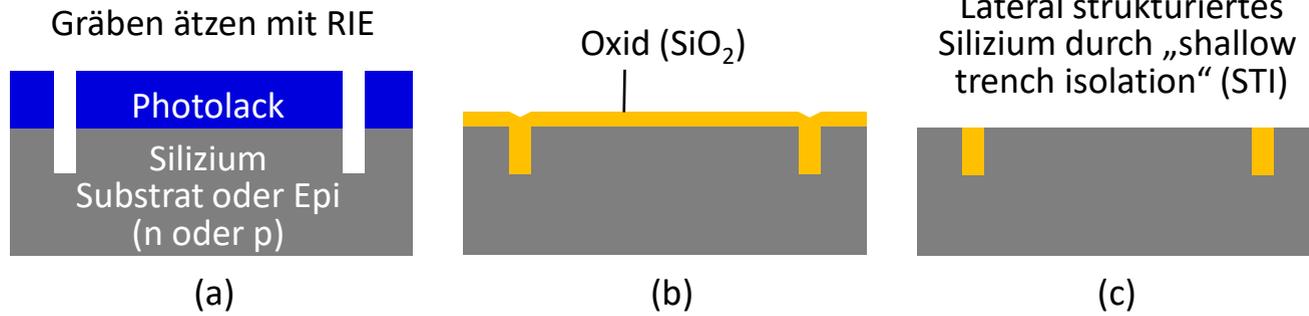


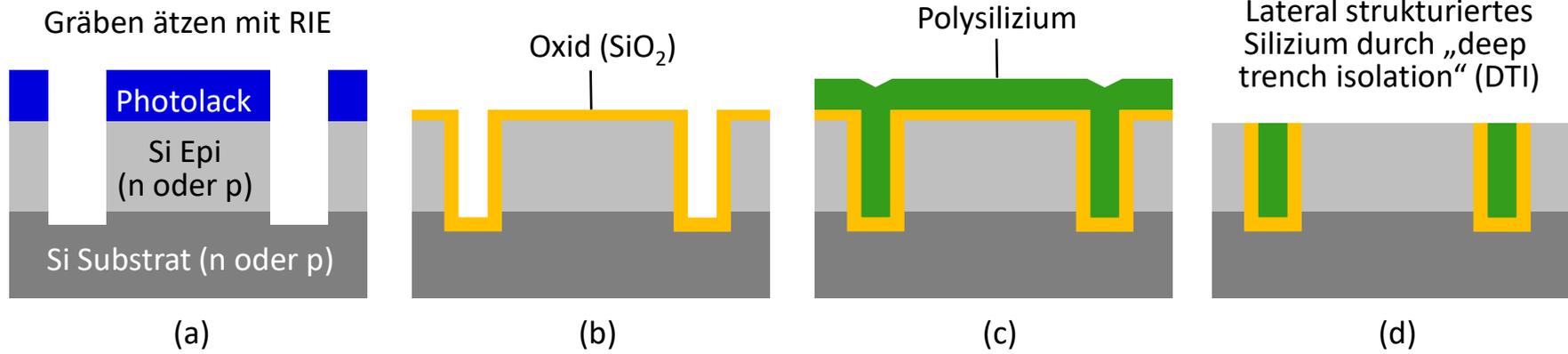


Dotierkonzentration (logarithmisch)



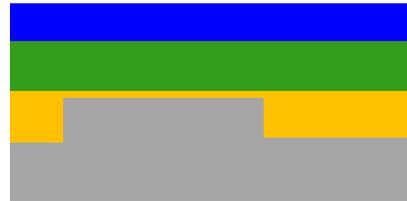




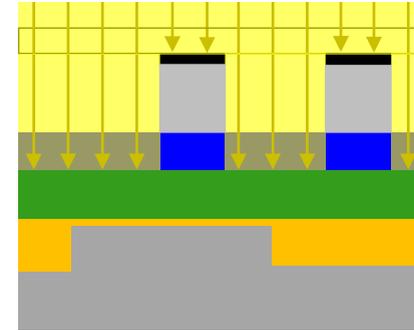




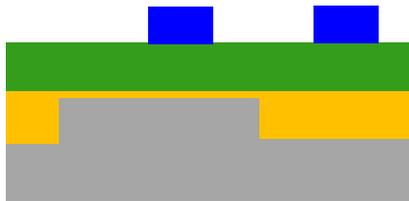
(a) Poly abscheiden



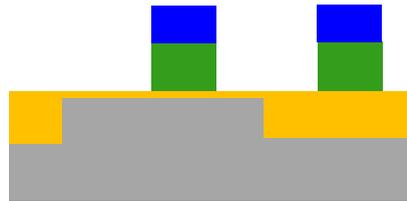
(b) Fotolack auftragen



(c) Belichten



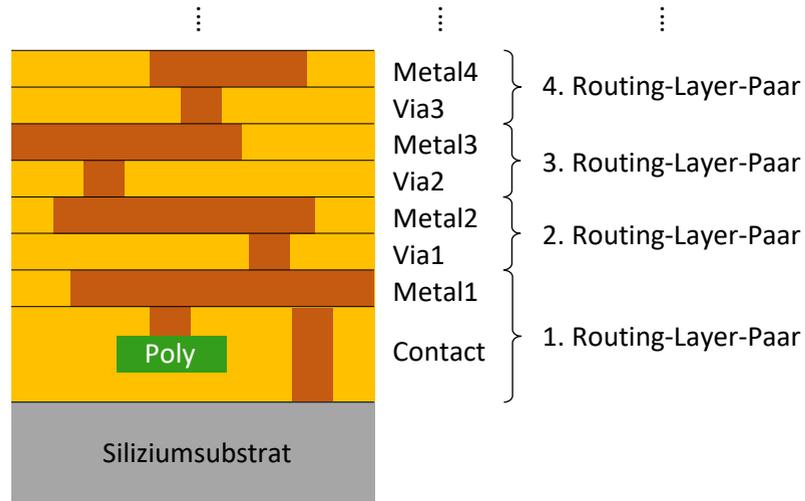
(d) Entwickeln

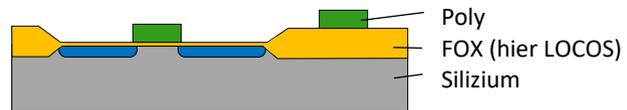


(e) Poly ätzen (RIE)

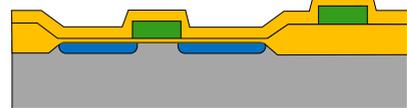


(f) Fotolack entfernen

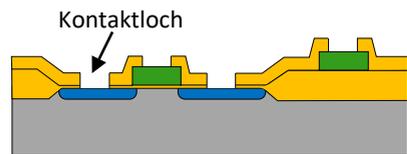




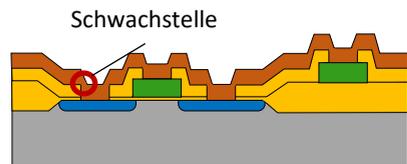
Anfangszustand nach FEOL



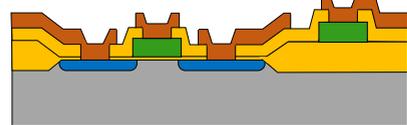
Schritt 1: 1. Zwischenoxid abscheiden



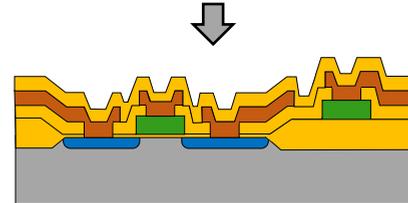
Schritt 2: Kontaktlöcher ätzen



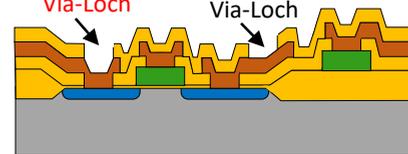
Schritt 3: Metall 1 abscheiden



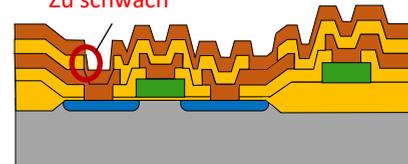
Schritt 4: Metall 1 ätzen



Schritt 5: 2. Zwischenoxid abscheiden



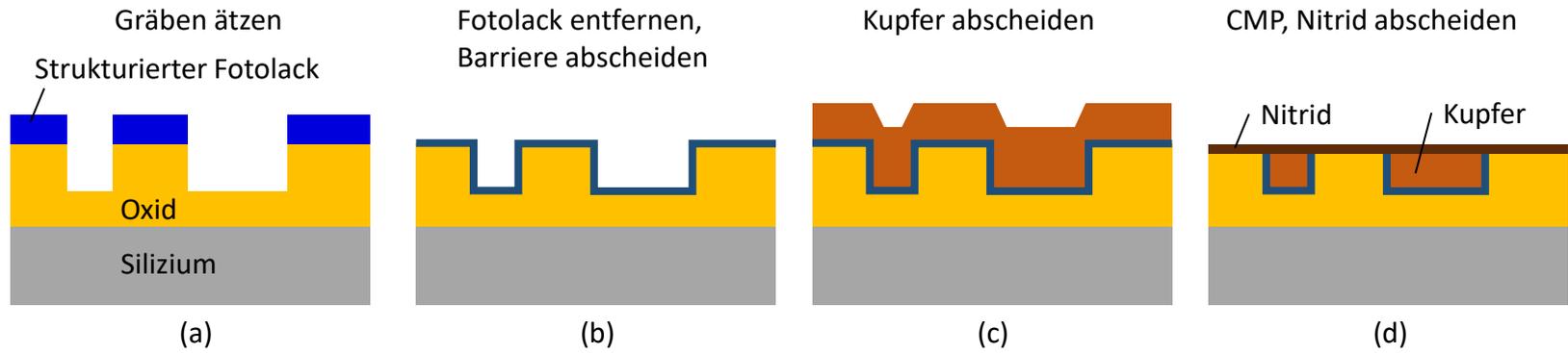
Schritt 6: Löcher für Via 1 ätzen

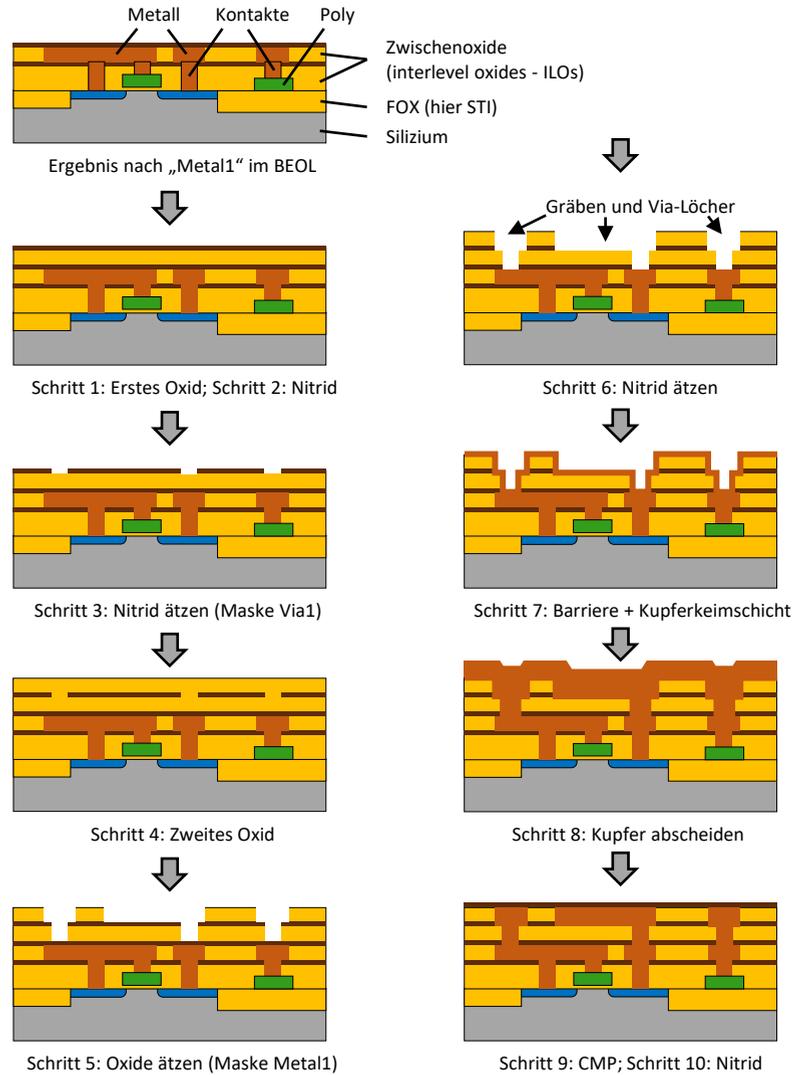


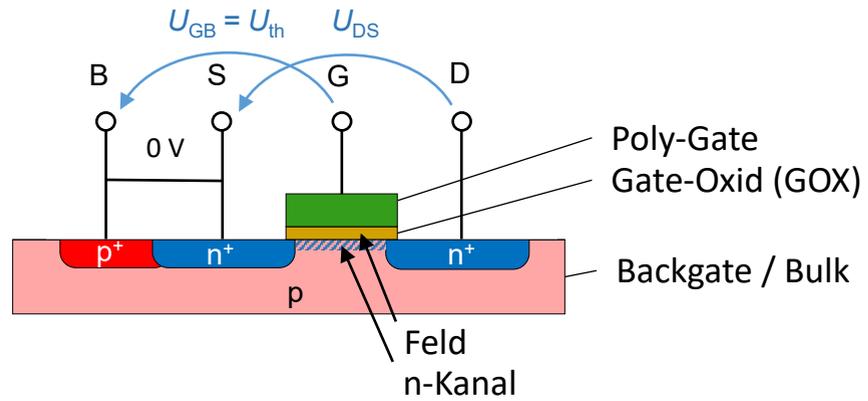
Schritt 7: Metall 2 abscheiden

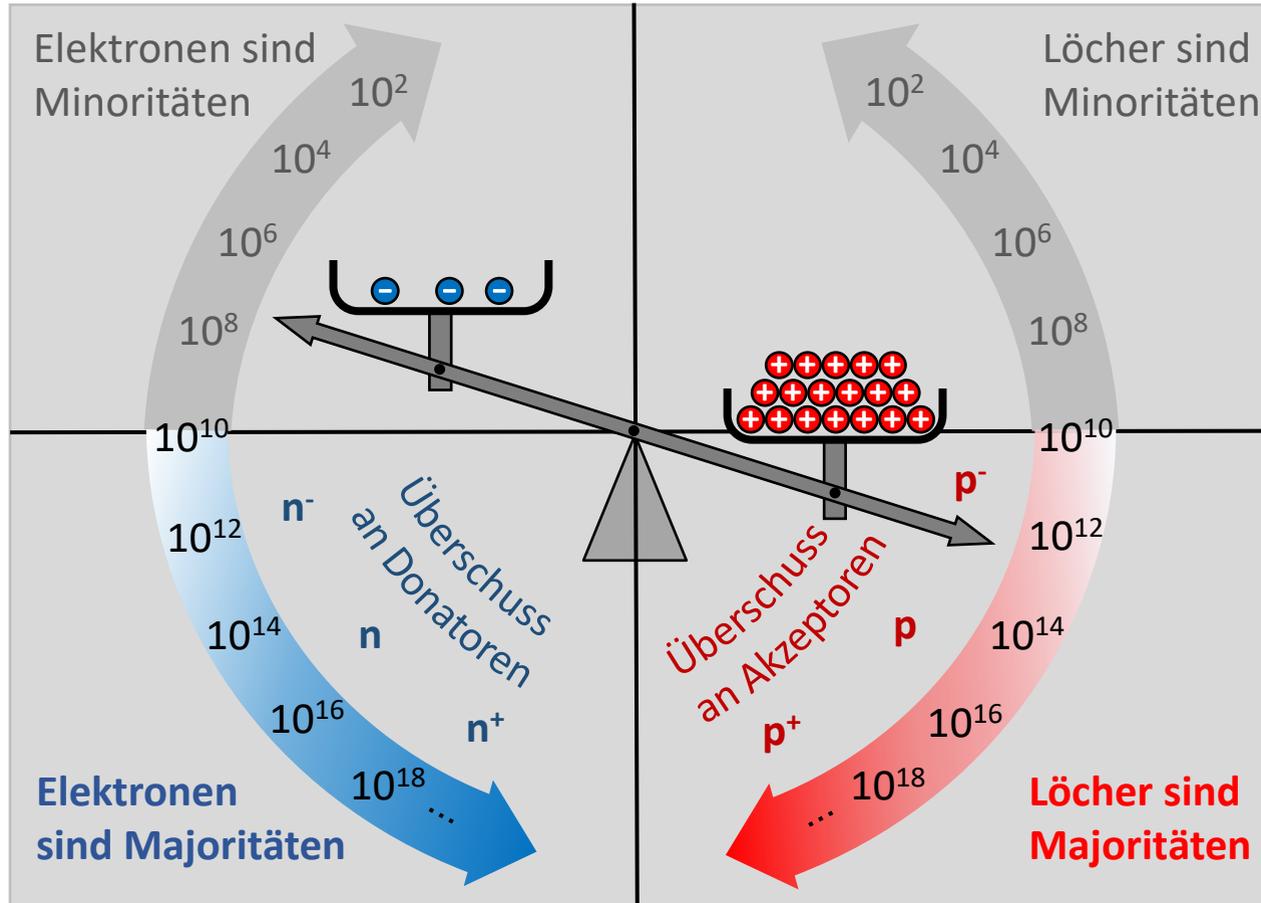


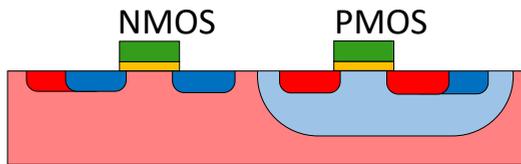
Schritt 8: Metall 2 ätzen



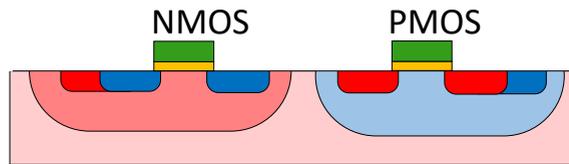




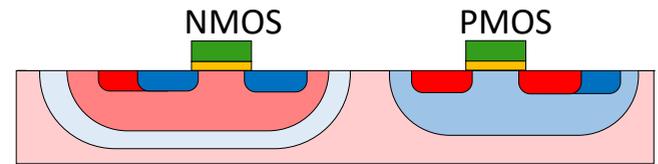




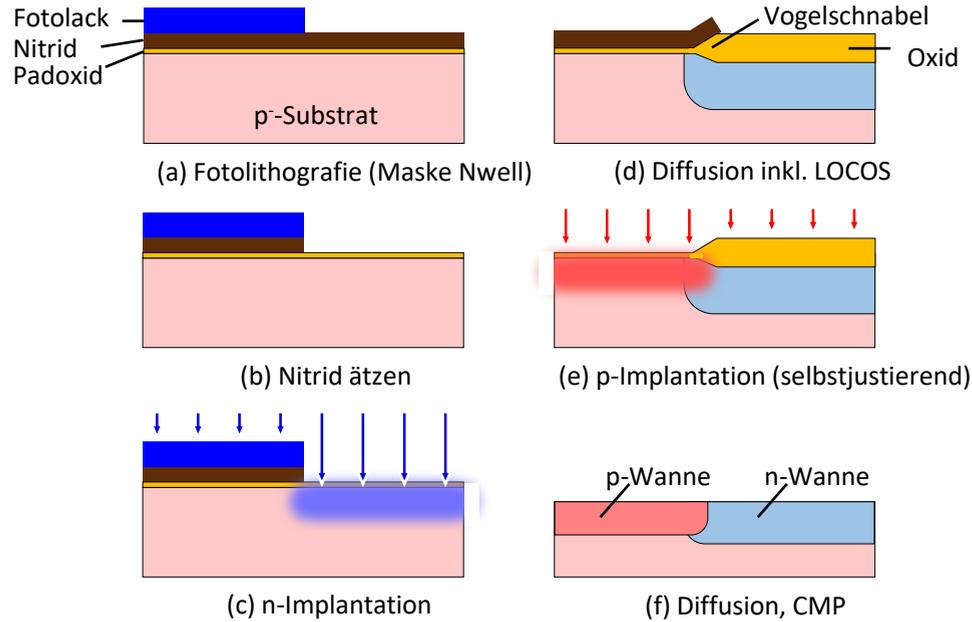
Single-Well-Prozess

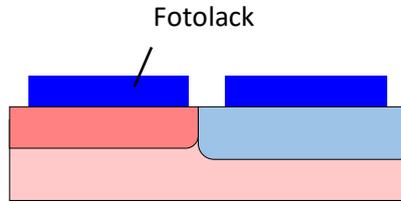


Twin-Well-Prozess

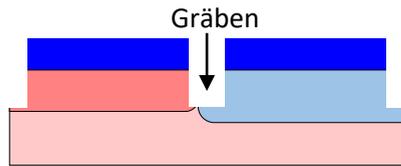


Triple-Well-Prozess

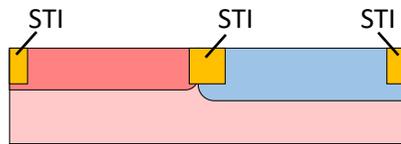




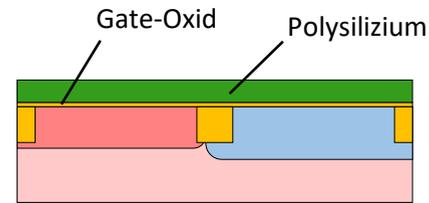
(a) Fotolithografie (Maske STI)



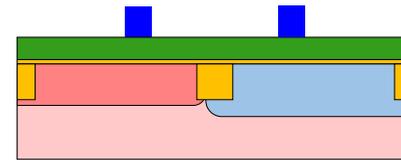
(b) Gräben für STI ätzen



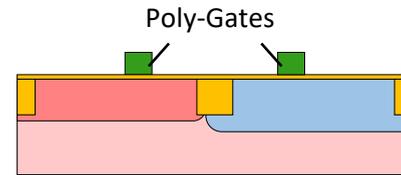
(c) Gräben für STI oxidieren, CMP



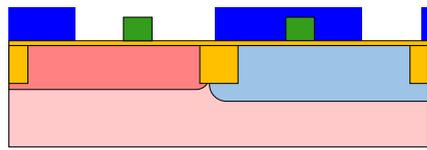
(d) Gate-Oxid und Poly abscheiden



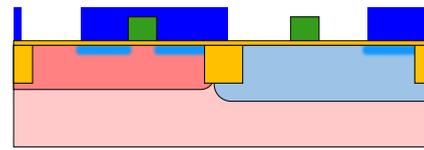
(e) Fotolithografie (Maske Poly)



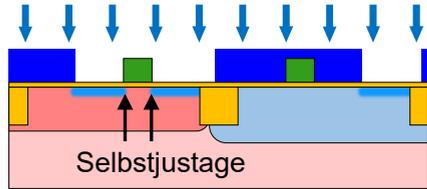
(f) Polysilizium ätzen



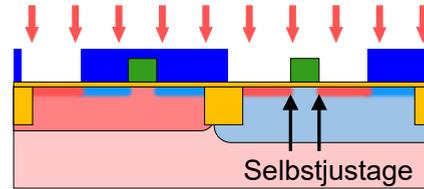
(a) Fotolithografie (Maske NSD)



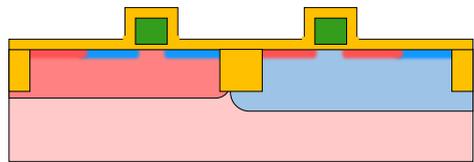
(c) Fotolithografie (Maske PSD)



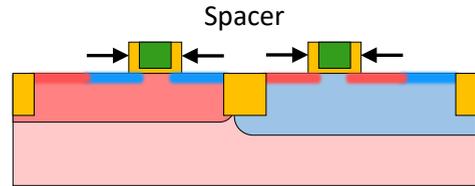
(b) n-Implantation (LDD)



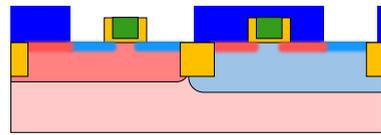
(d) p-Implantation (LDD)



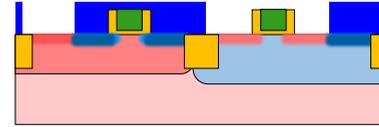
(a) Oxidation durch CVD



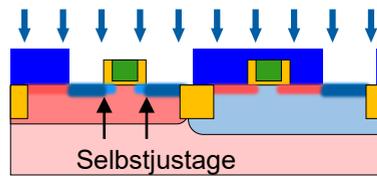
(b) Oxid ätzen



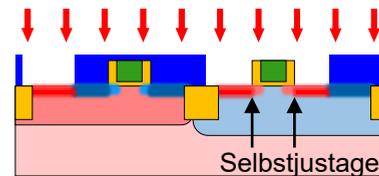
(a) Fotolithografie (Maske NSD)



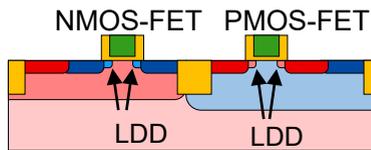
(c) Fotolithografie (Maske PSD)



(b) n⁺-Implantation



(d) p⁺-Implantation



(e) Diffusion