Chapter 7: Addressing Reliability in Physical Design

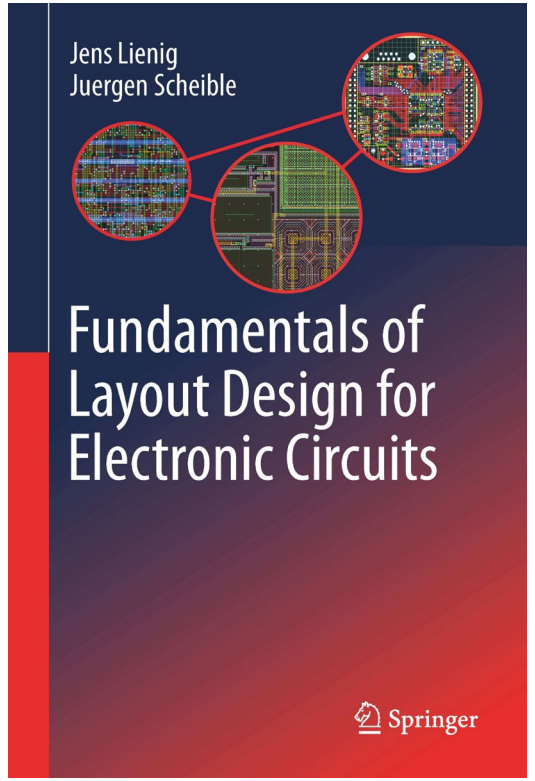
7.1 Parasitic Effects in Silicon

7.2 Surface Effects

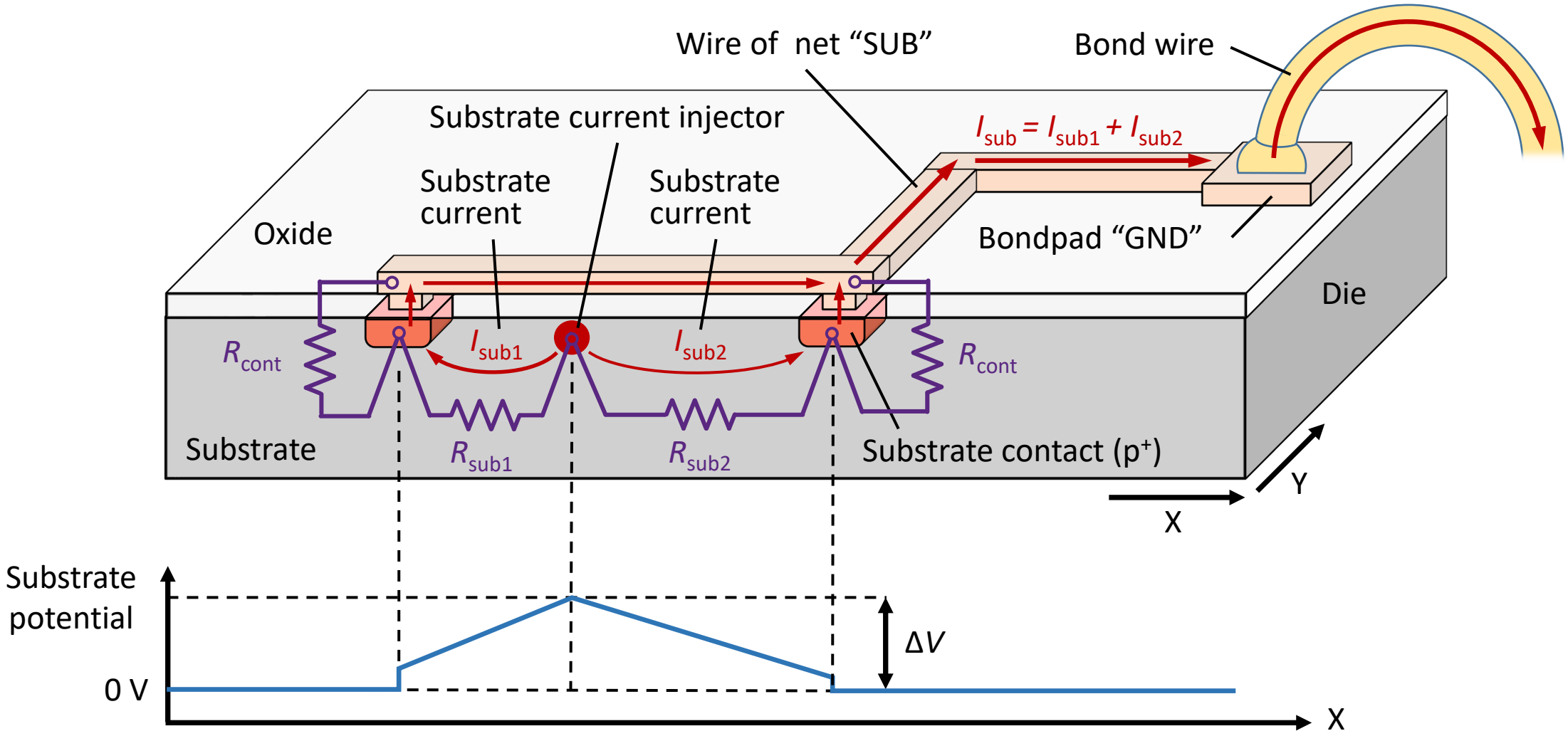
7.3 Interconnect Parasitics

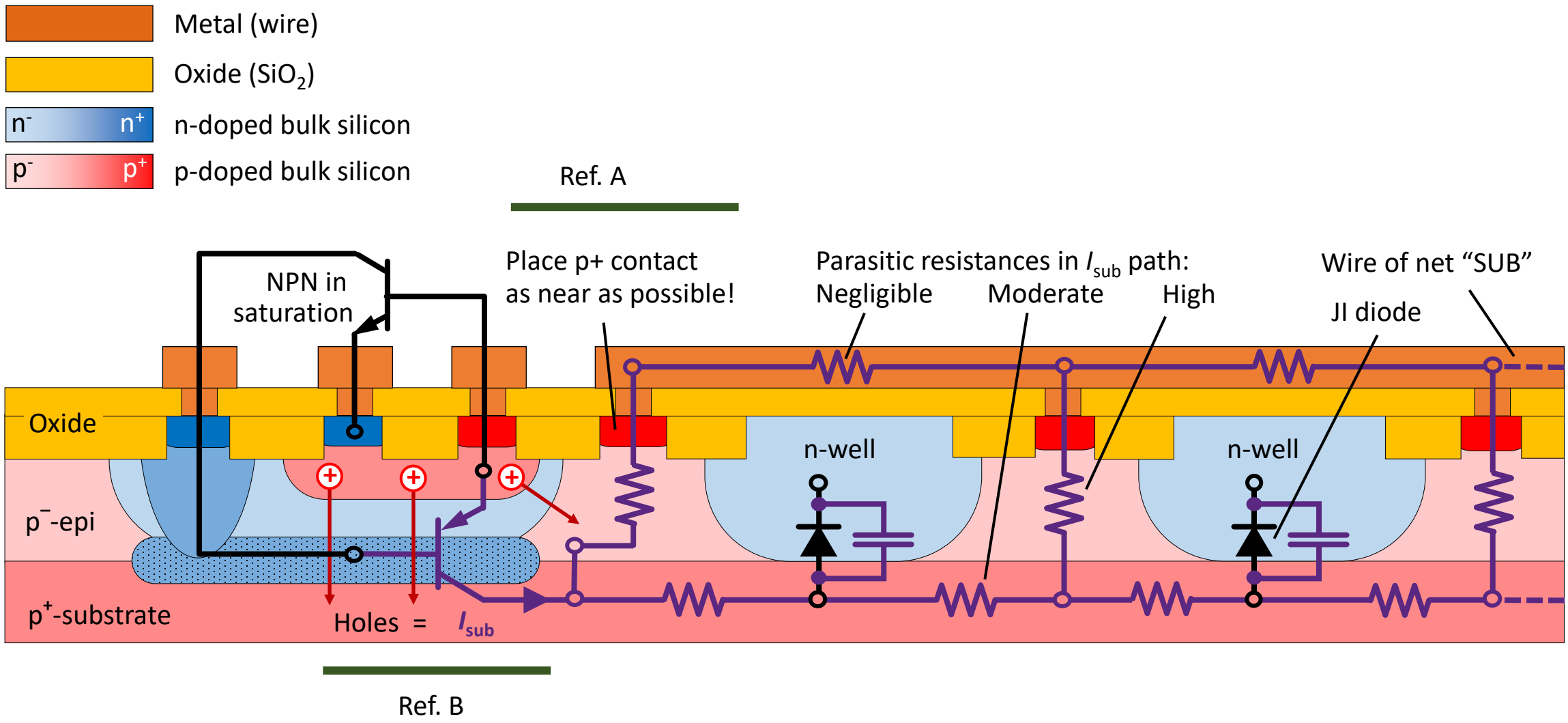
7.4 Overvoltage Protection

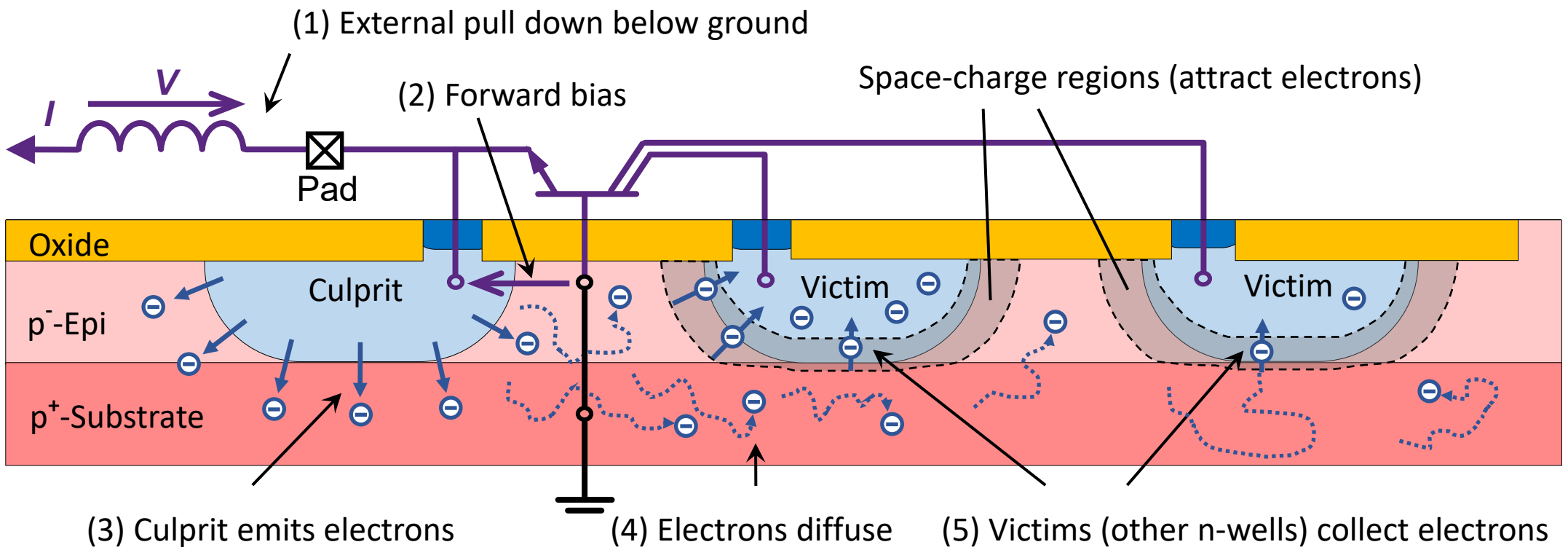
7.5 Migration Effects in Metal

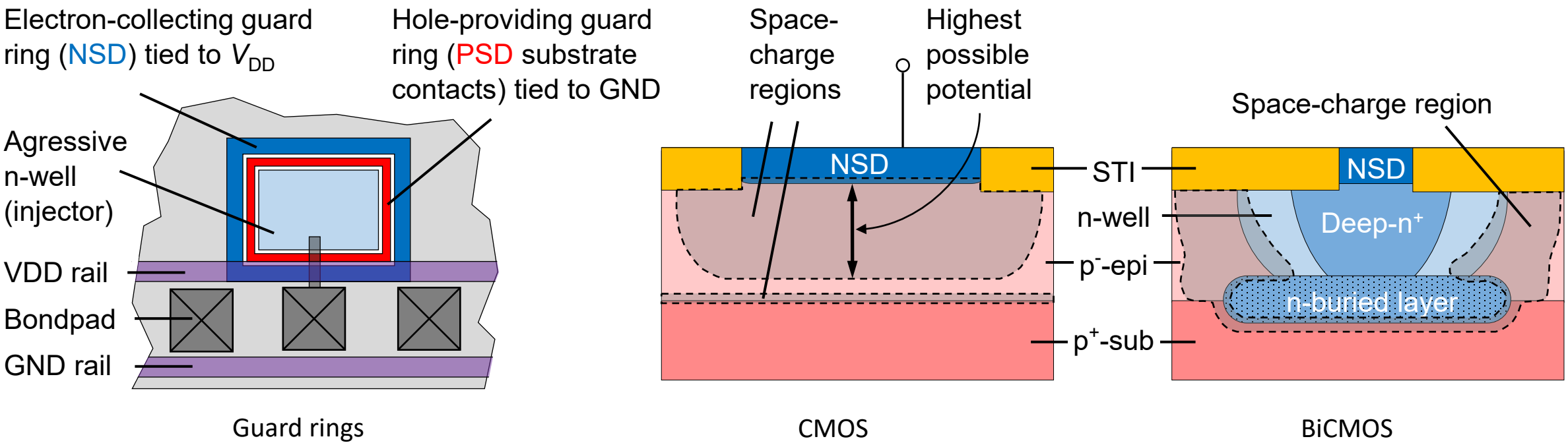


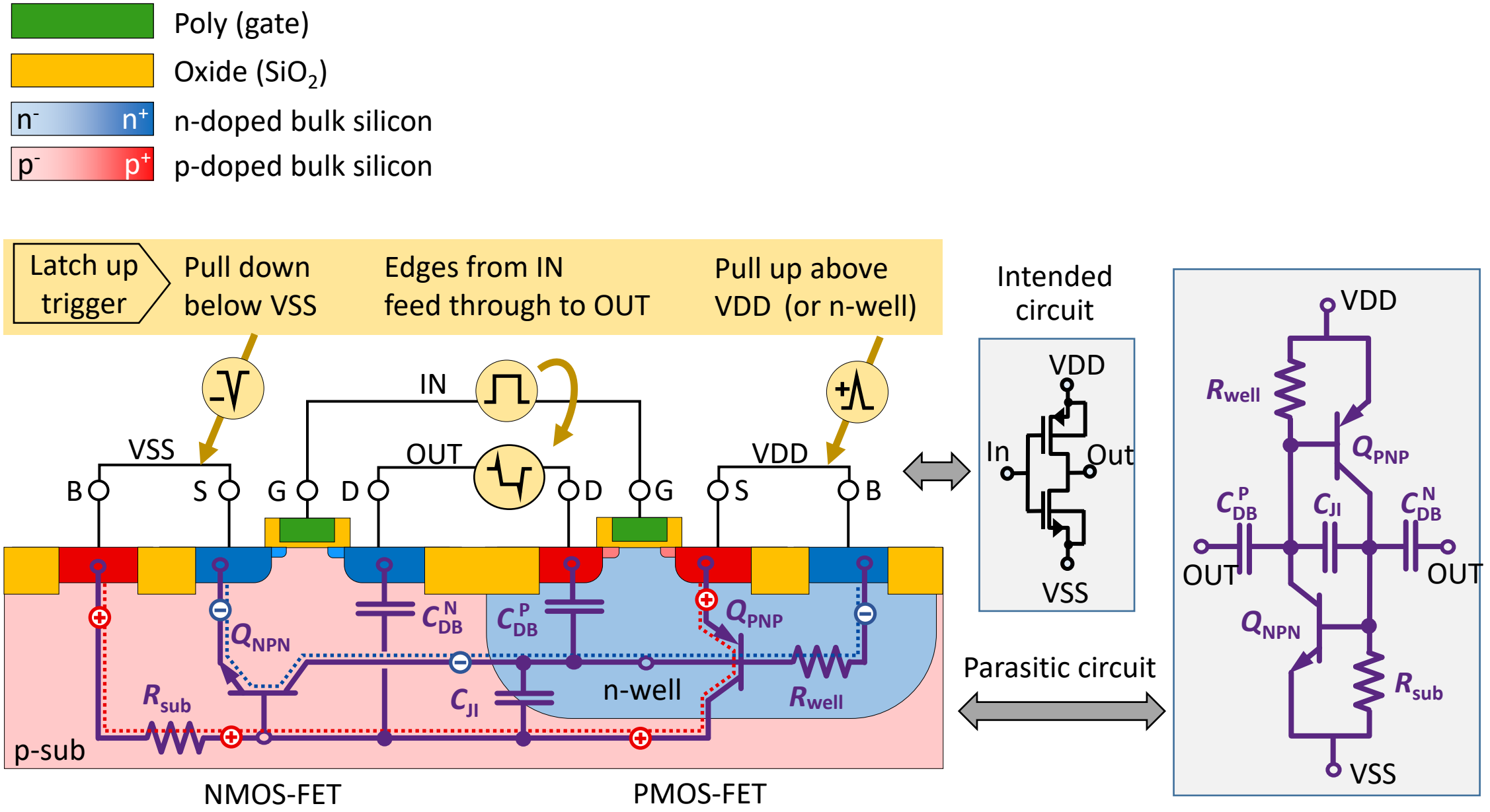
Chapter 7: Addressing Reliability in Physical Design

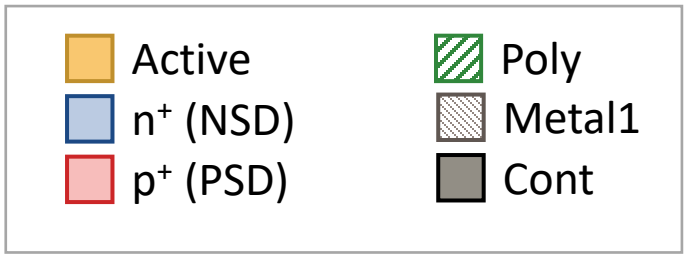


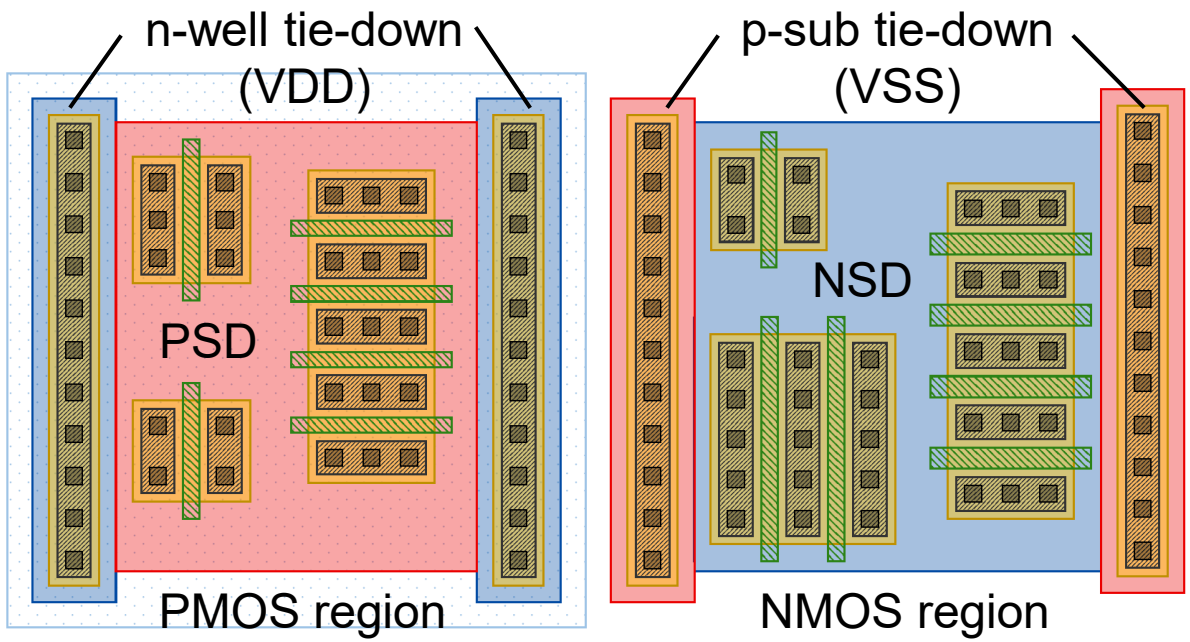




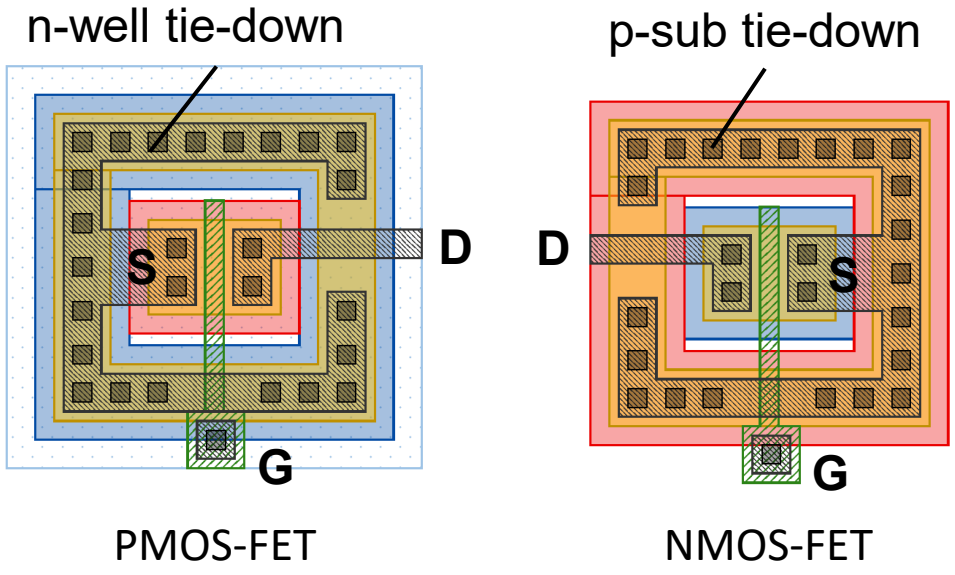




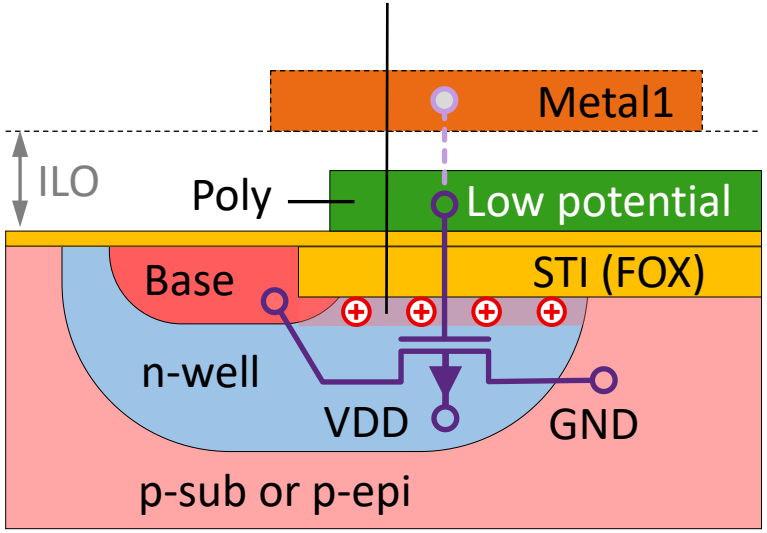




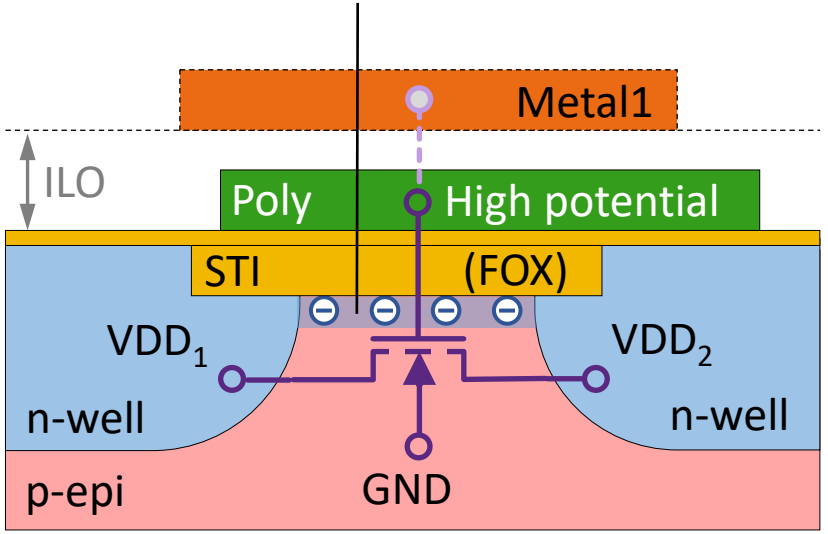
Backgate contacts laid out as guard rings

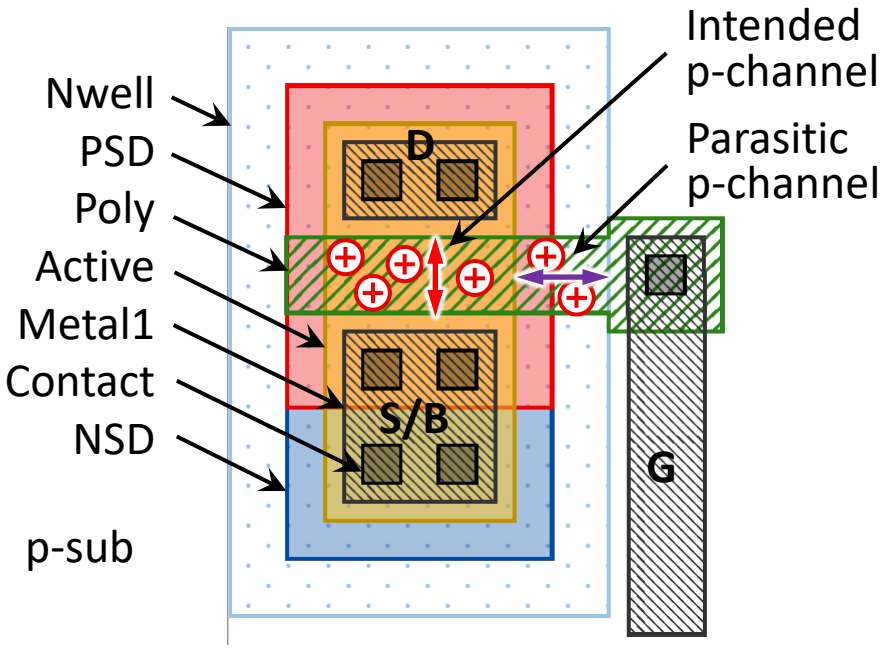


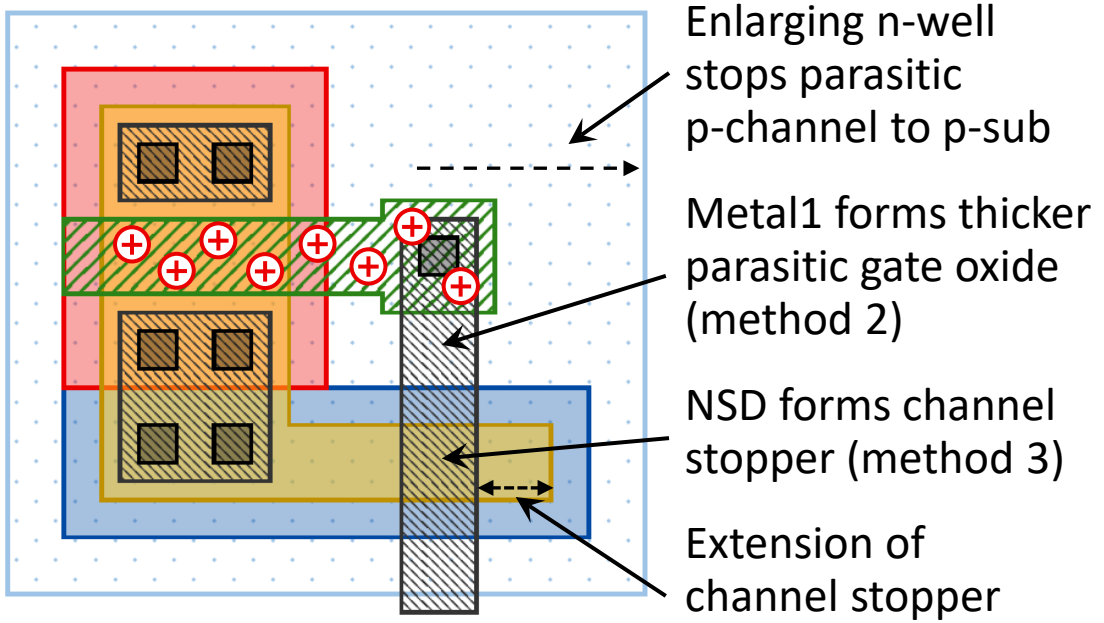
Parasitic PMOS channel

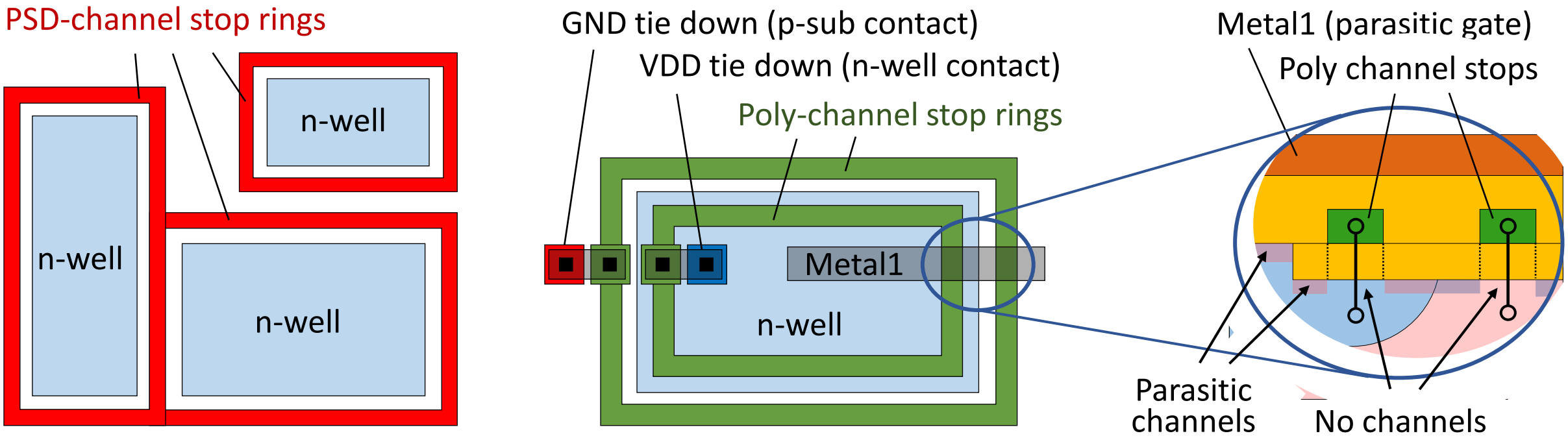


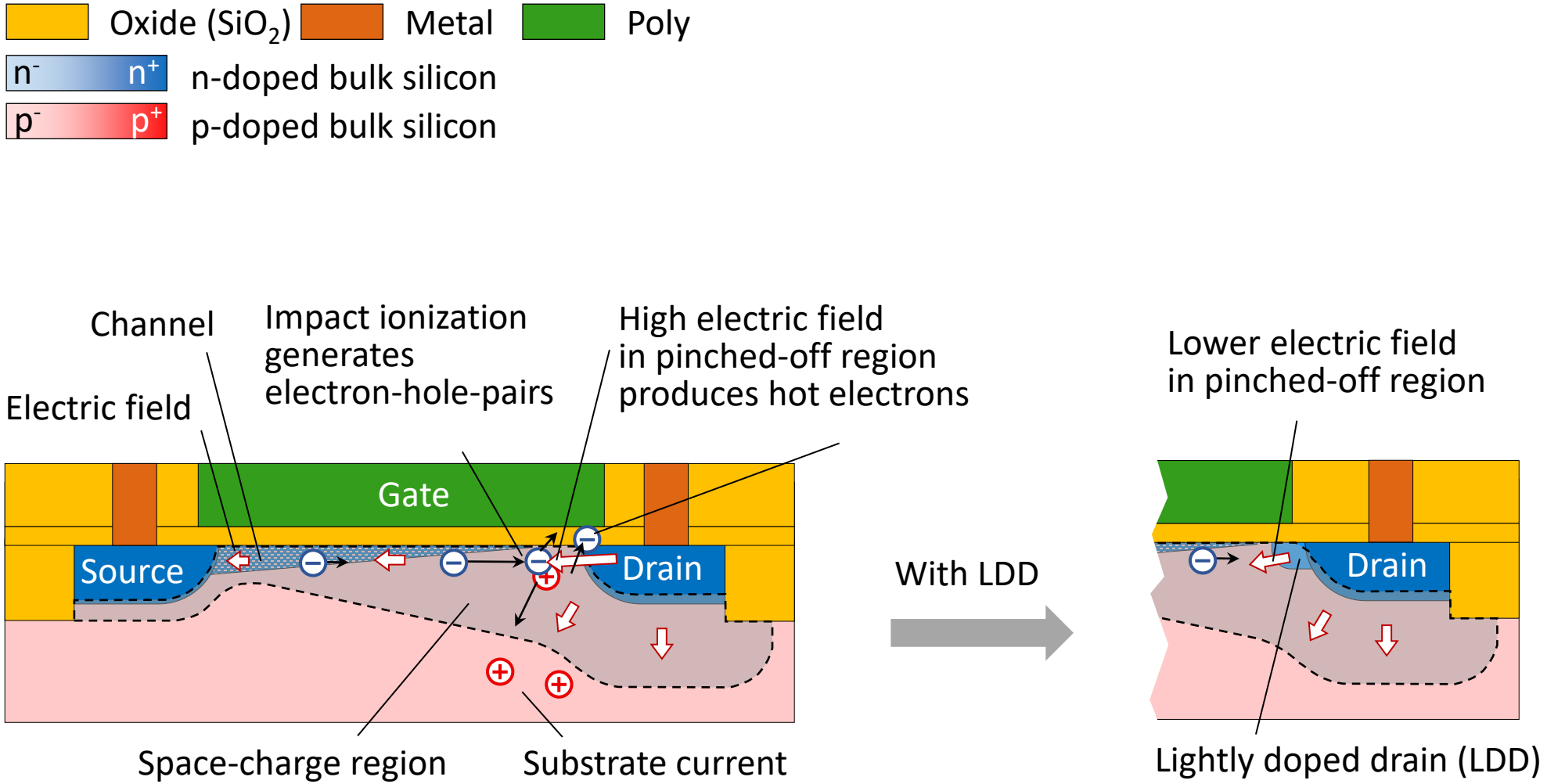
Parasitic NMOS channel

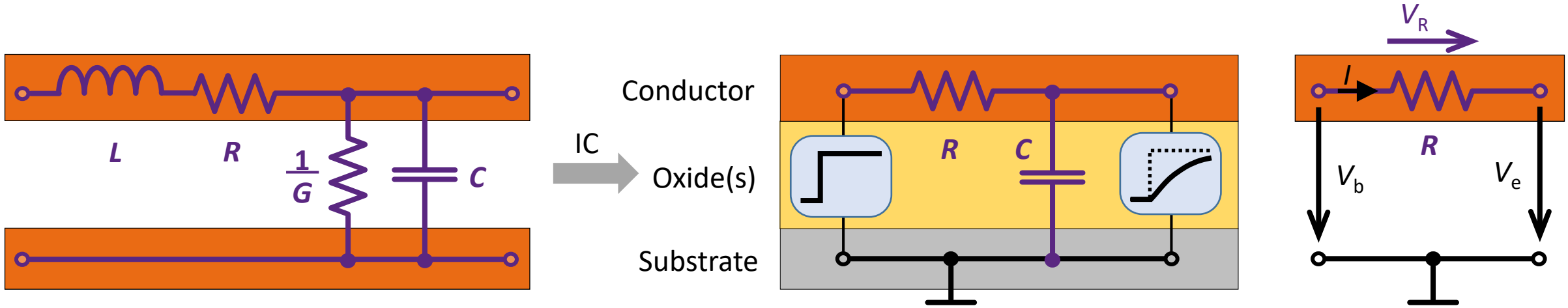


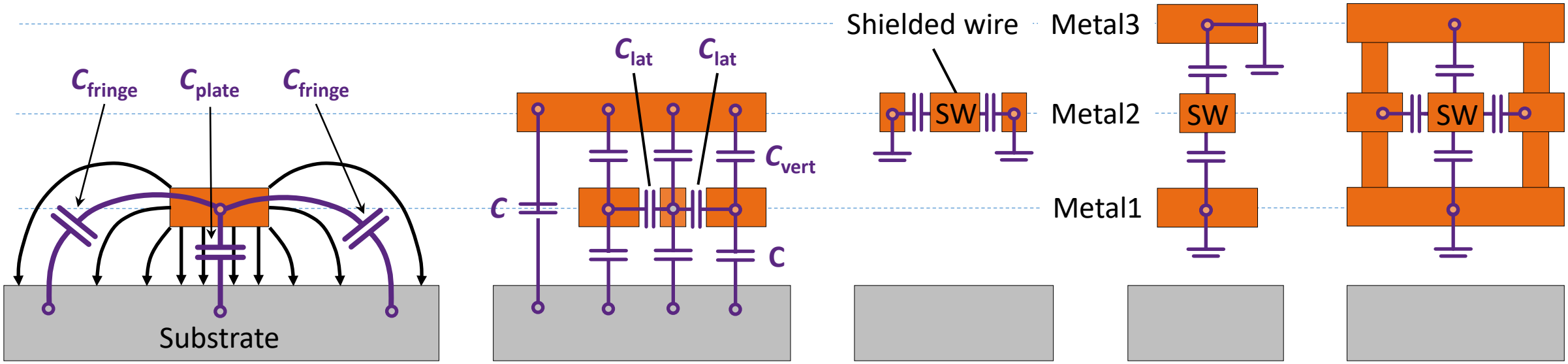


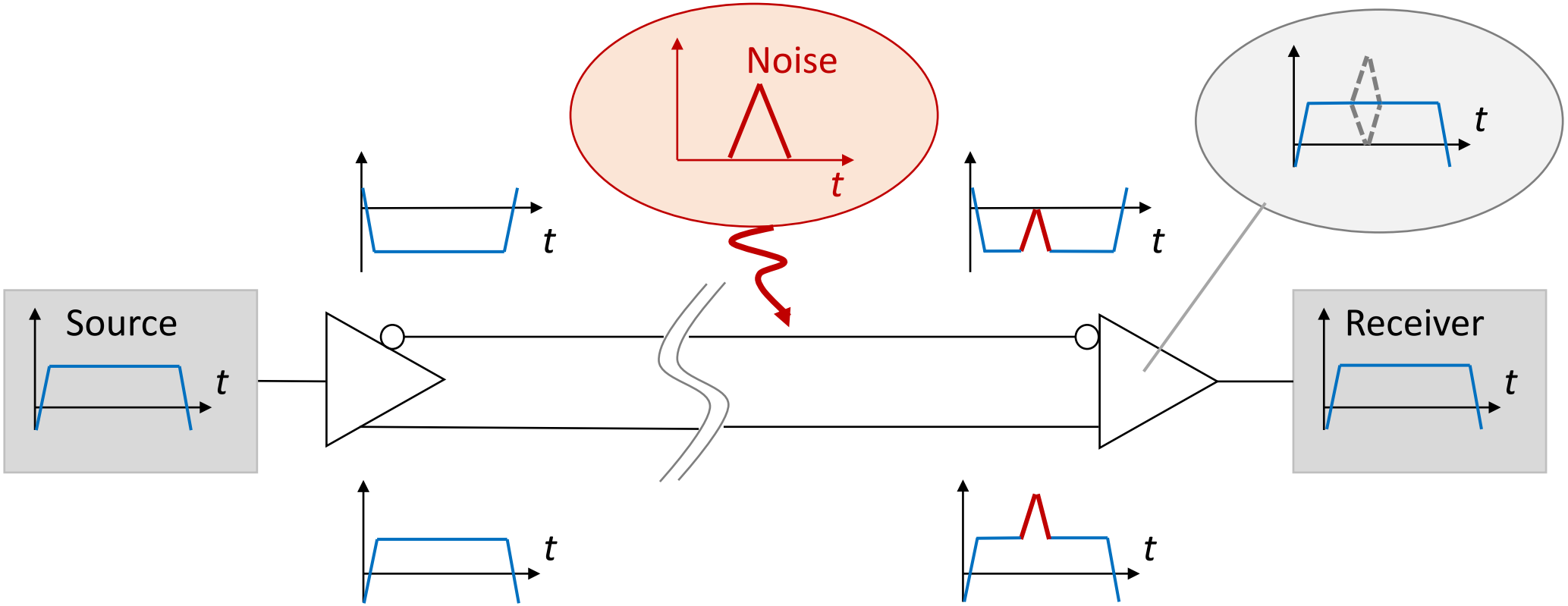


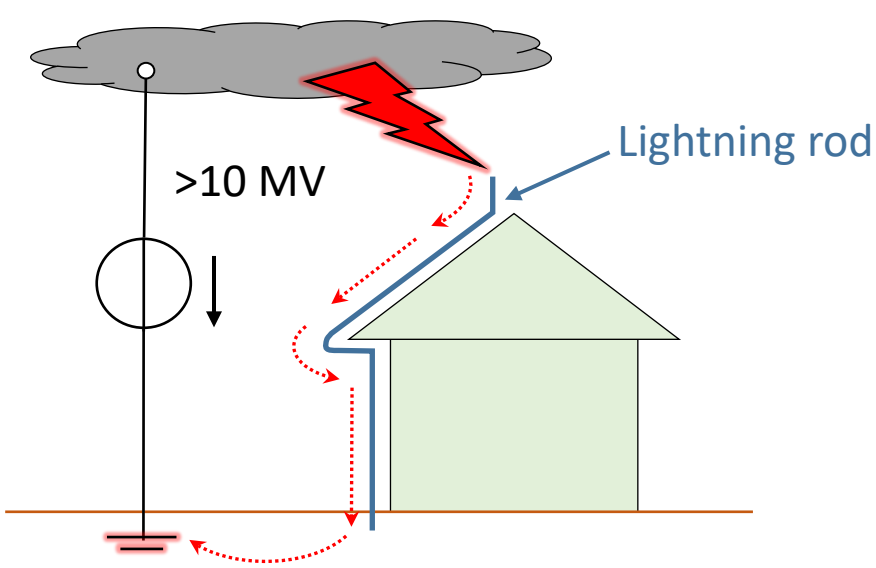


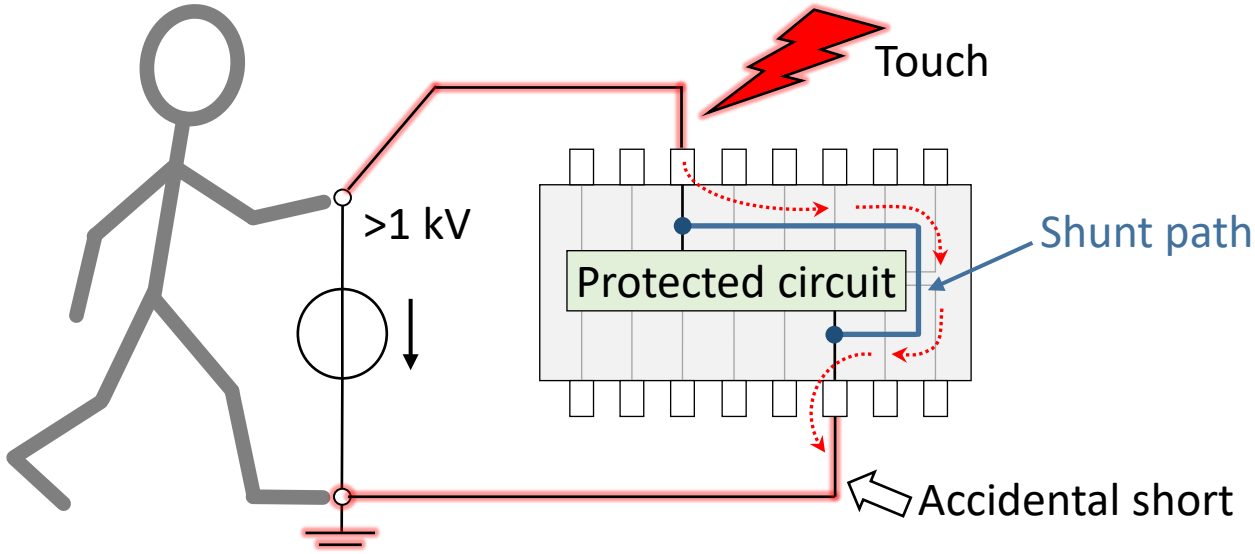


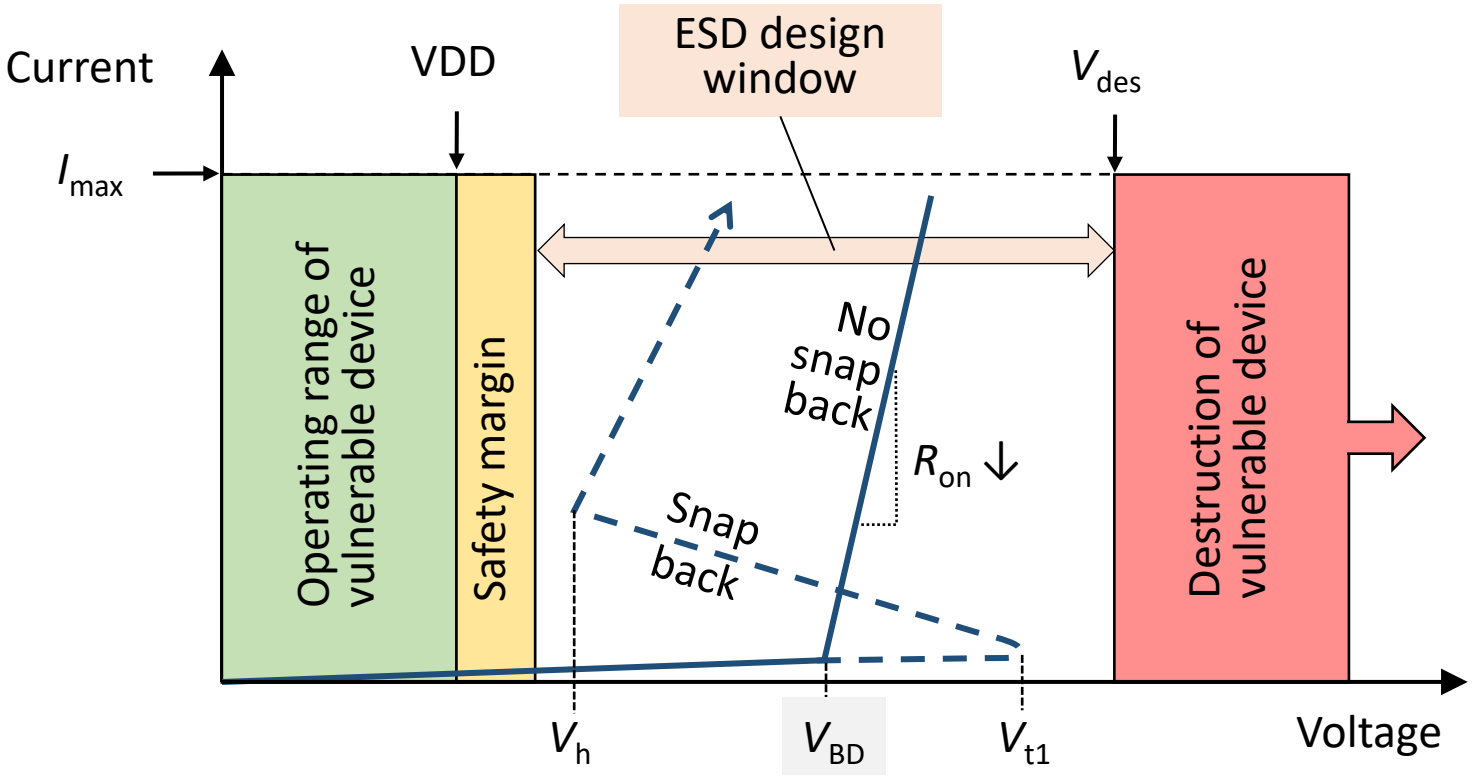




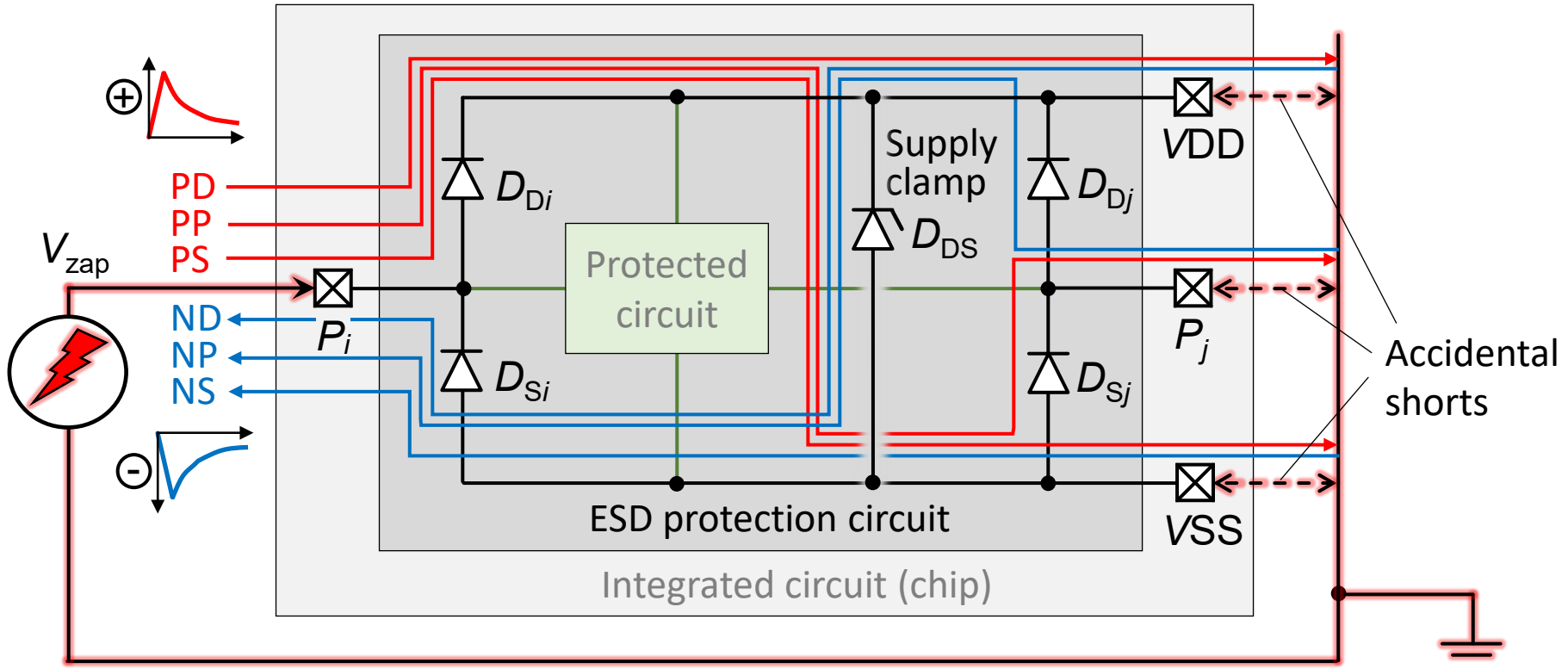


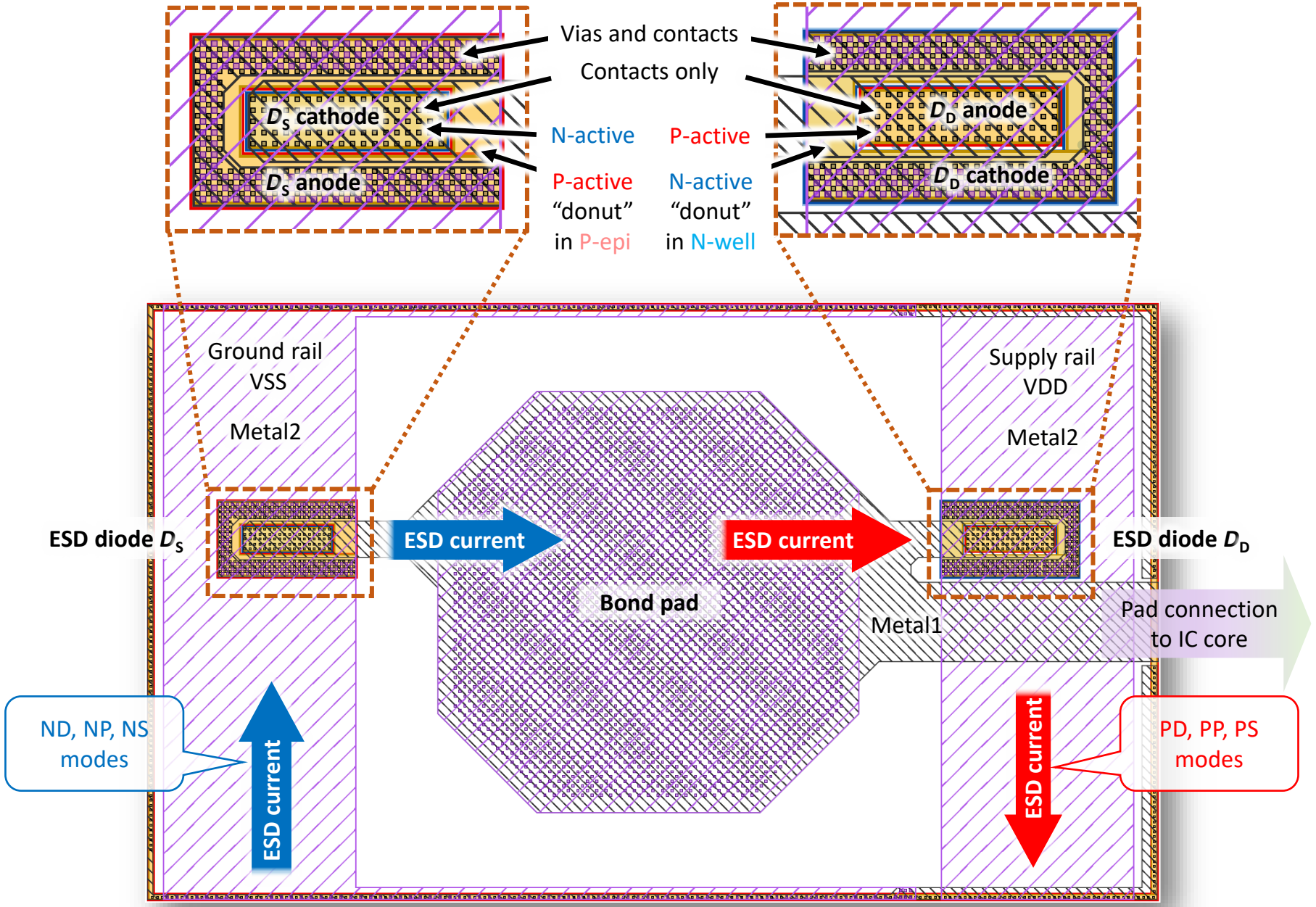


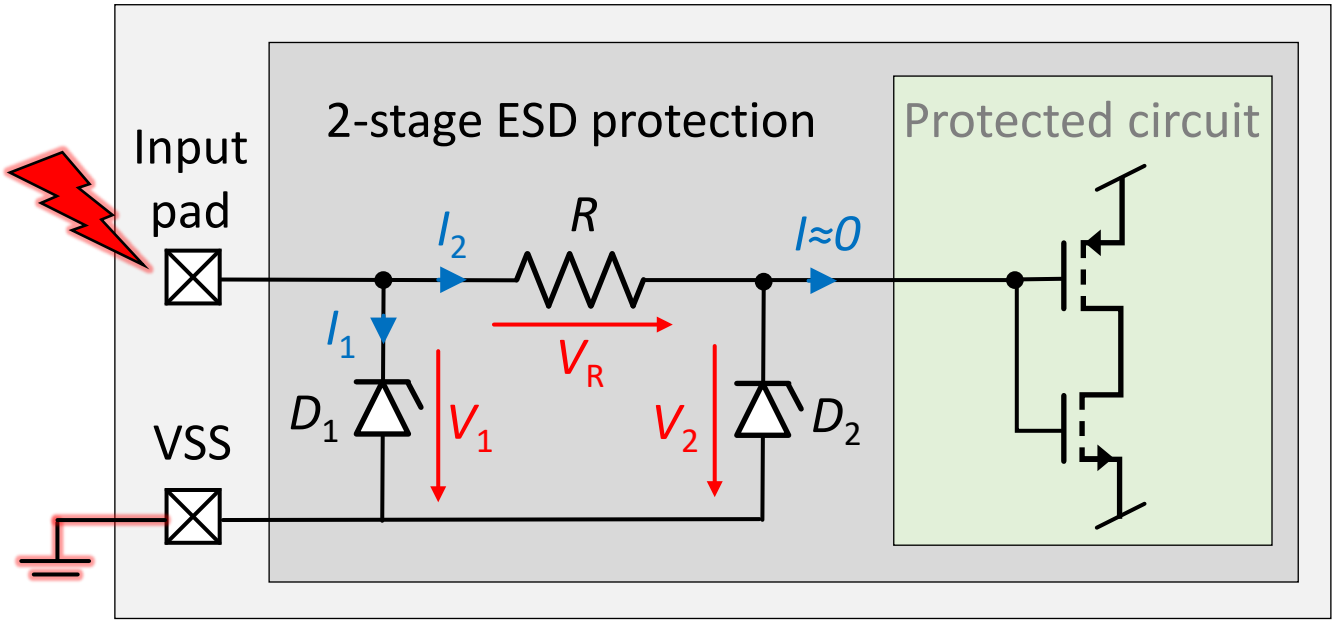




V_h Holding voltage
V_{BD} Breakdown voltage
V_{t1} Trigger voltage
V_{des} Destruction voltage



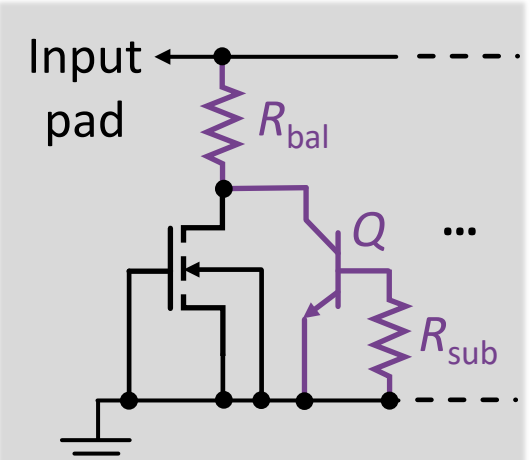


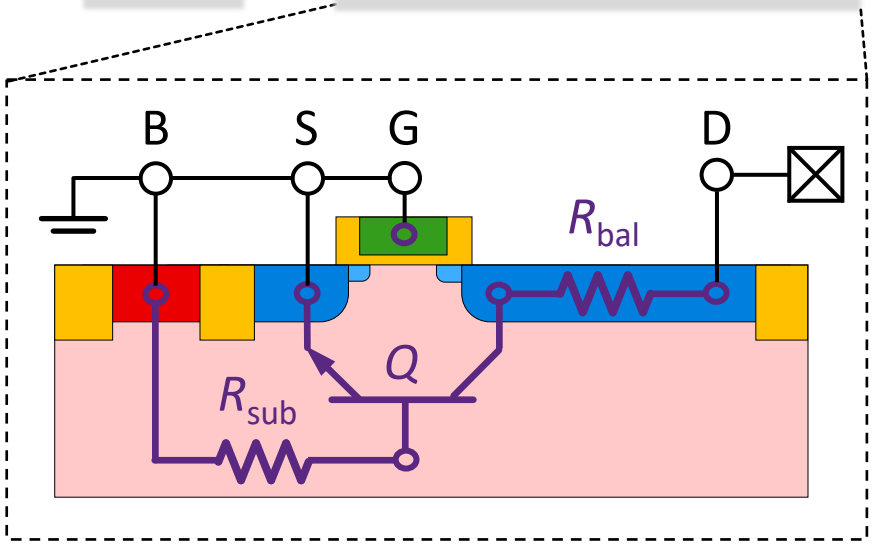


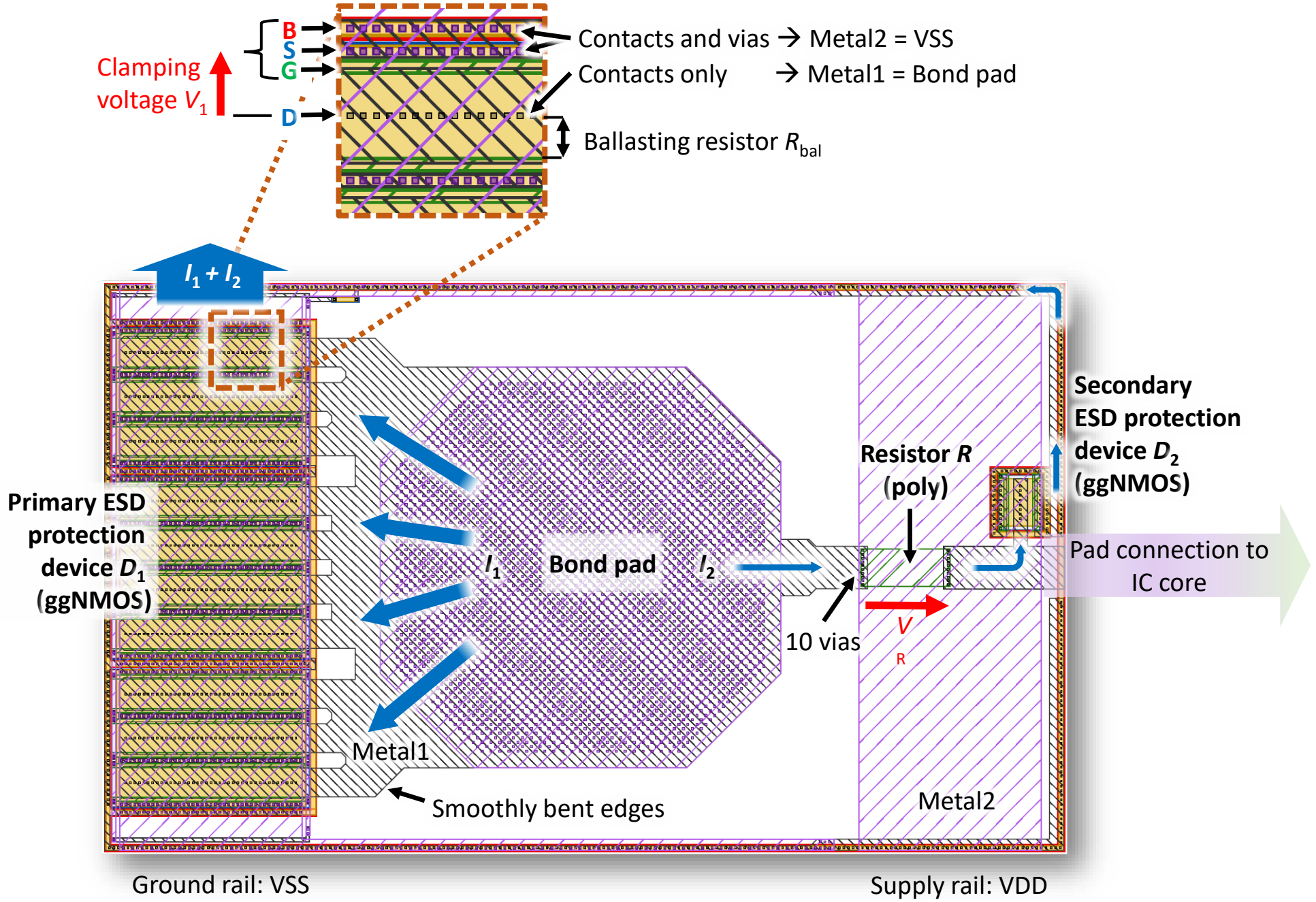
Examples of ESD devices D_1, D_2:

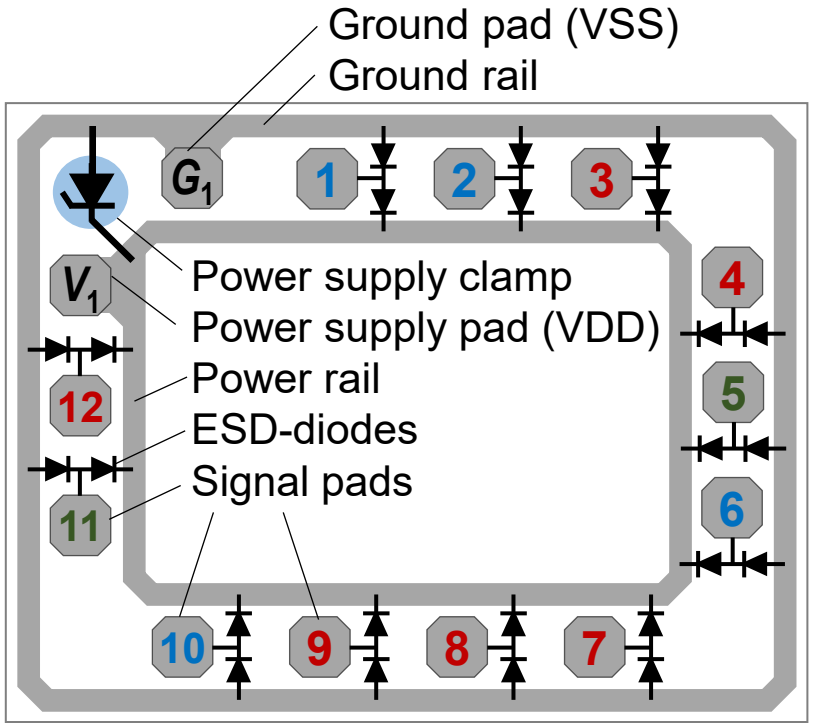
Zener diode

ggNMOS

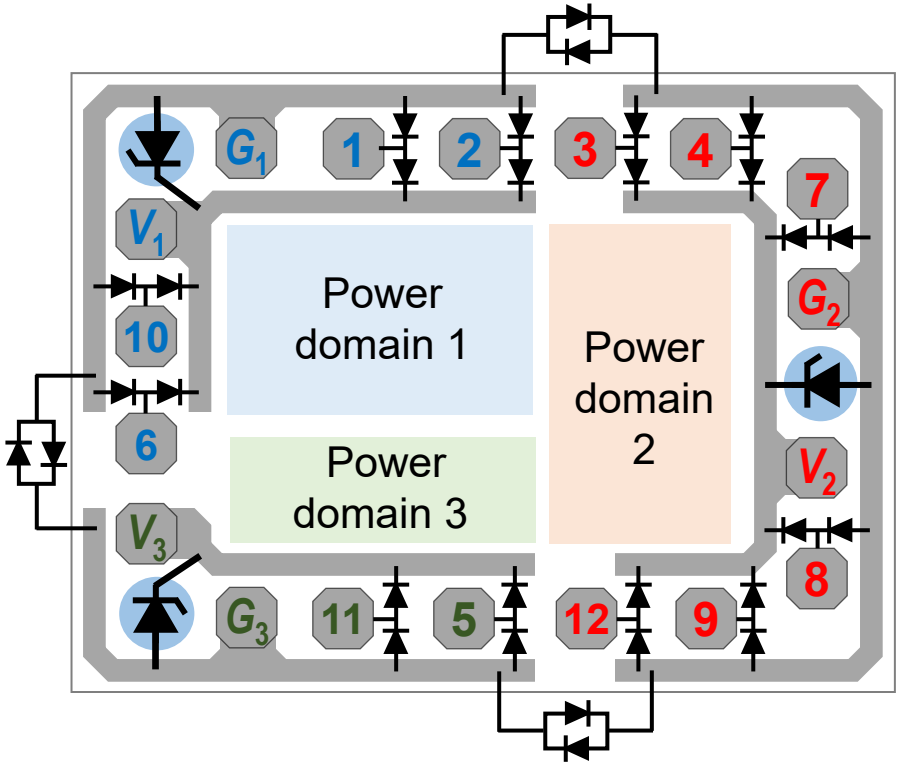




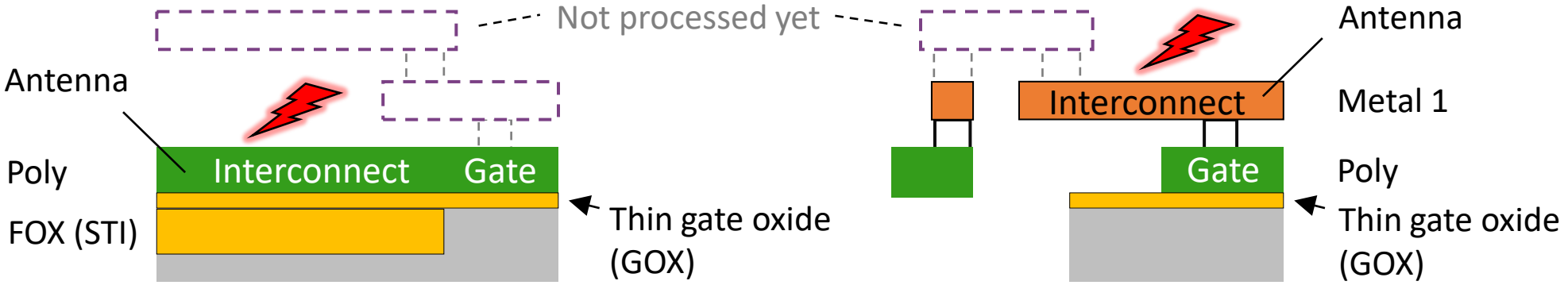


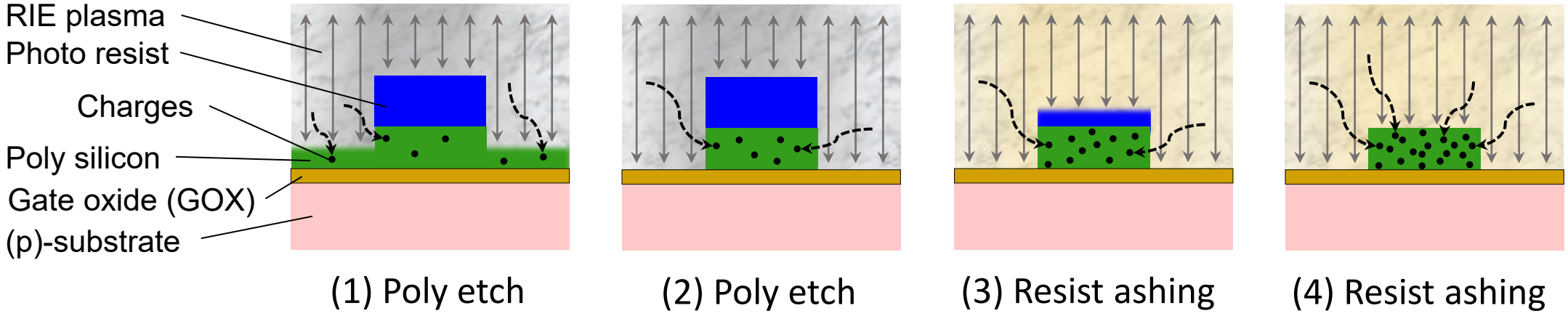


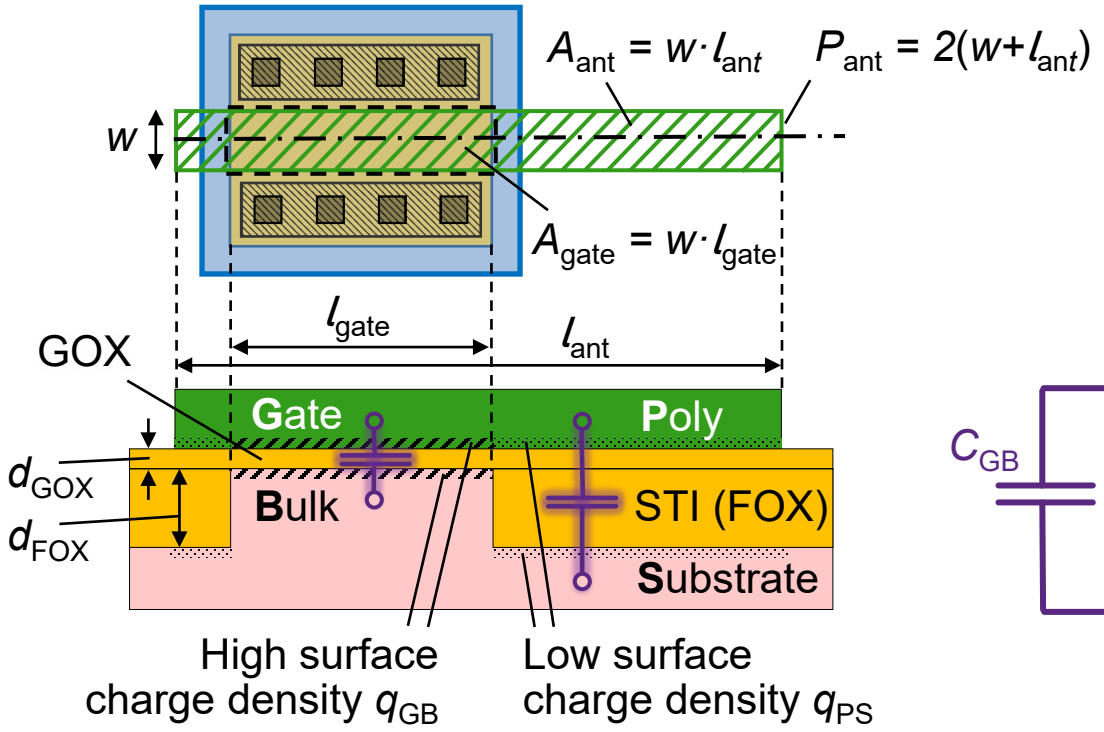
Single power domain

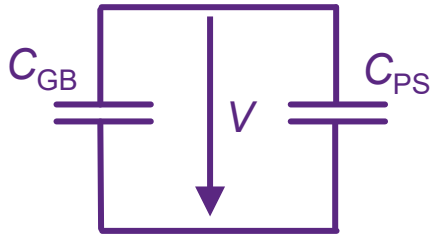


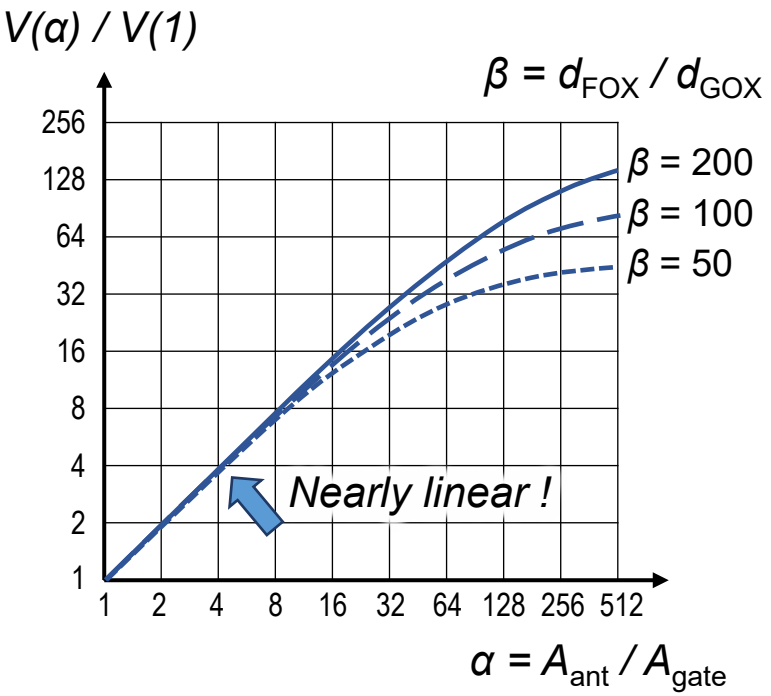
Multiple power domains

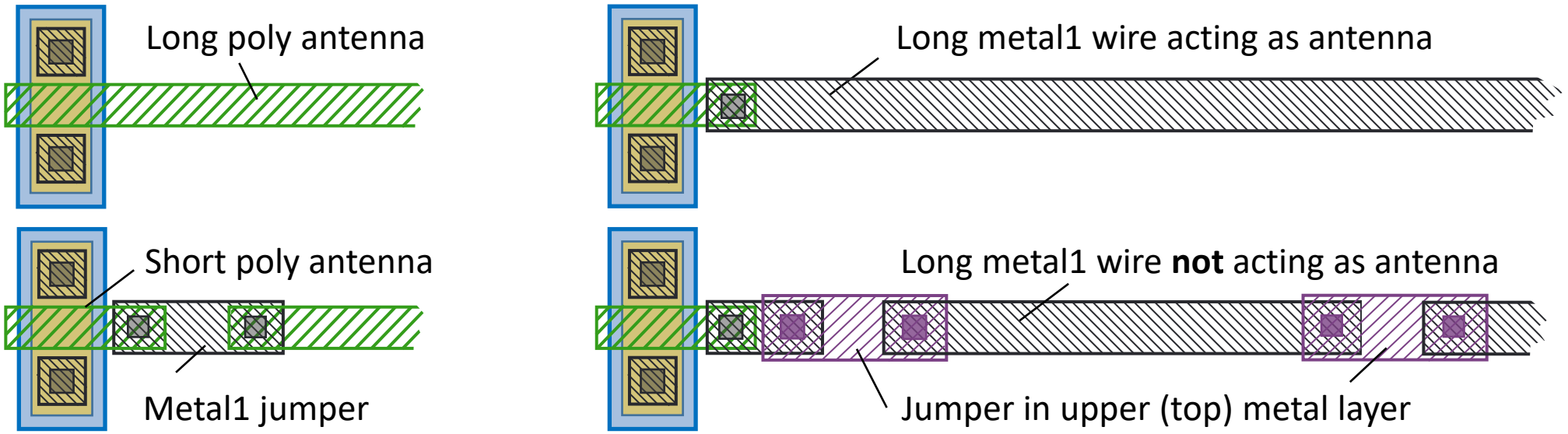


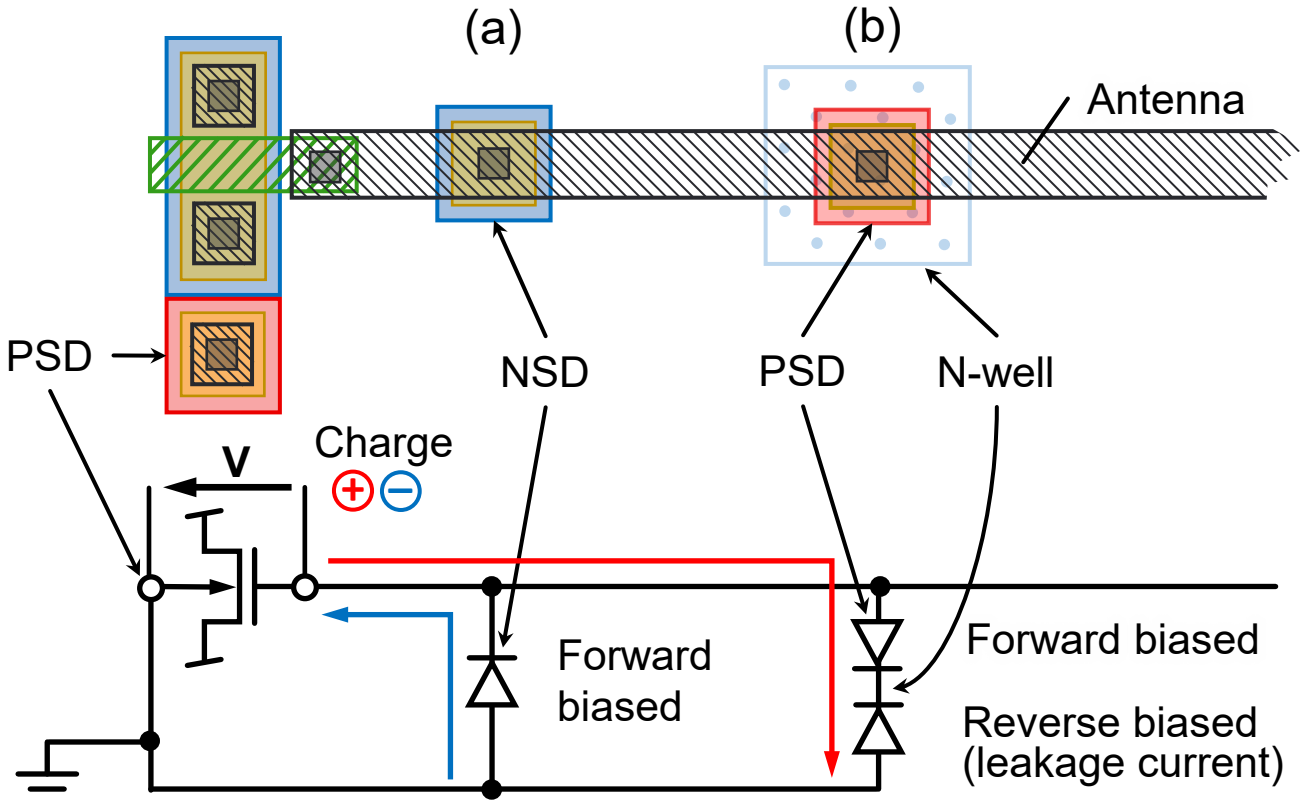


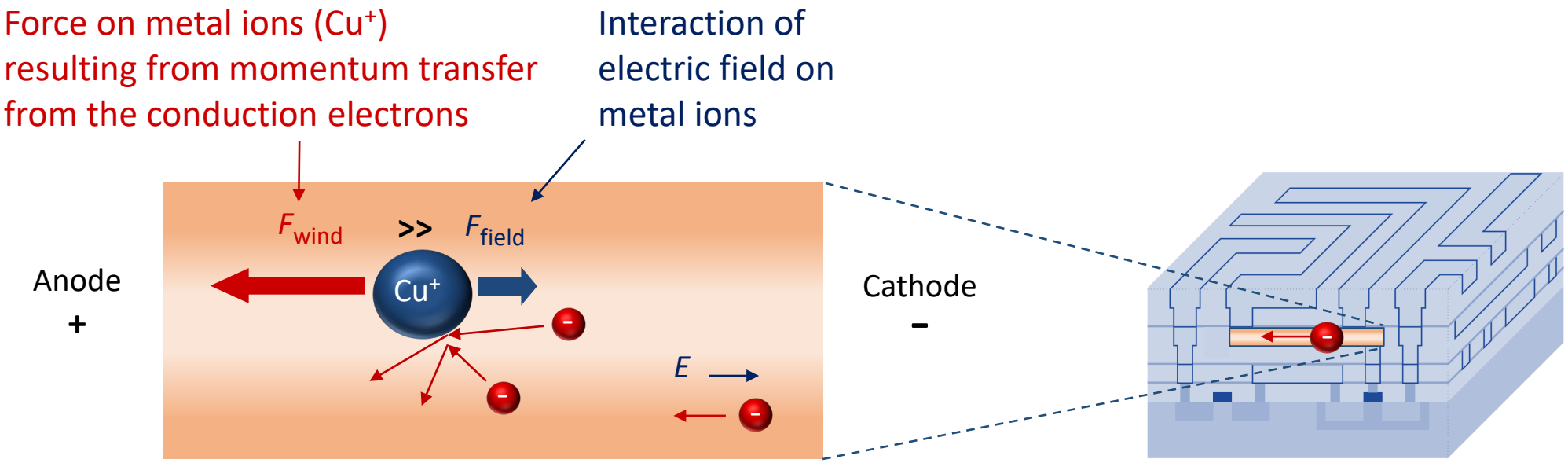




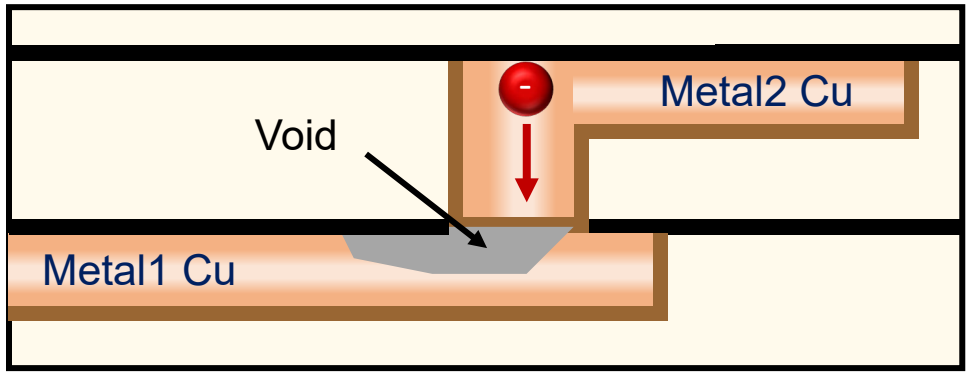




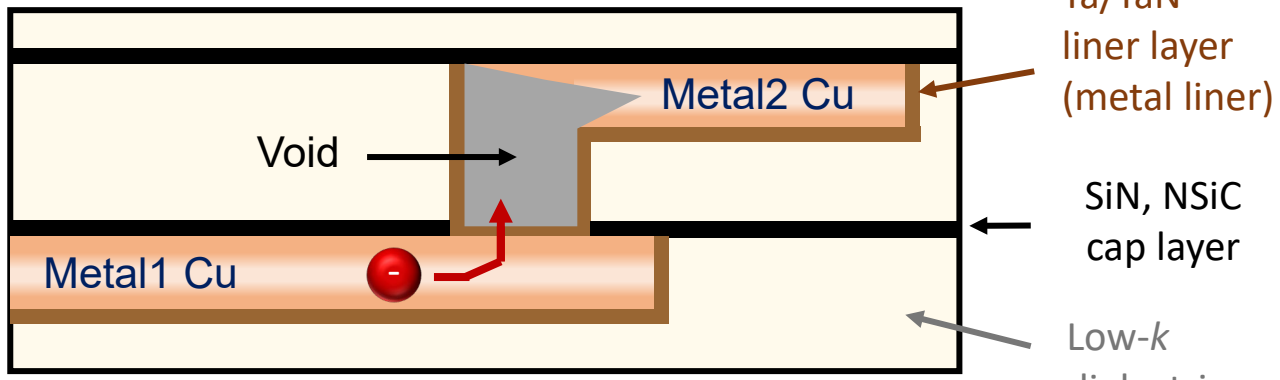


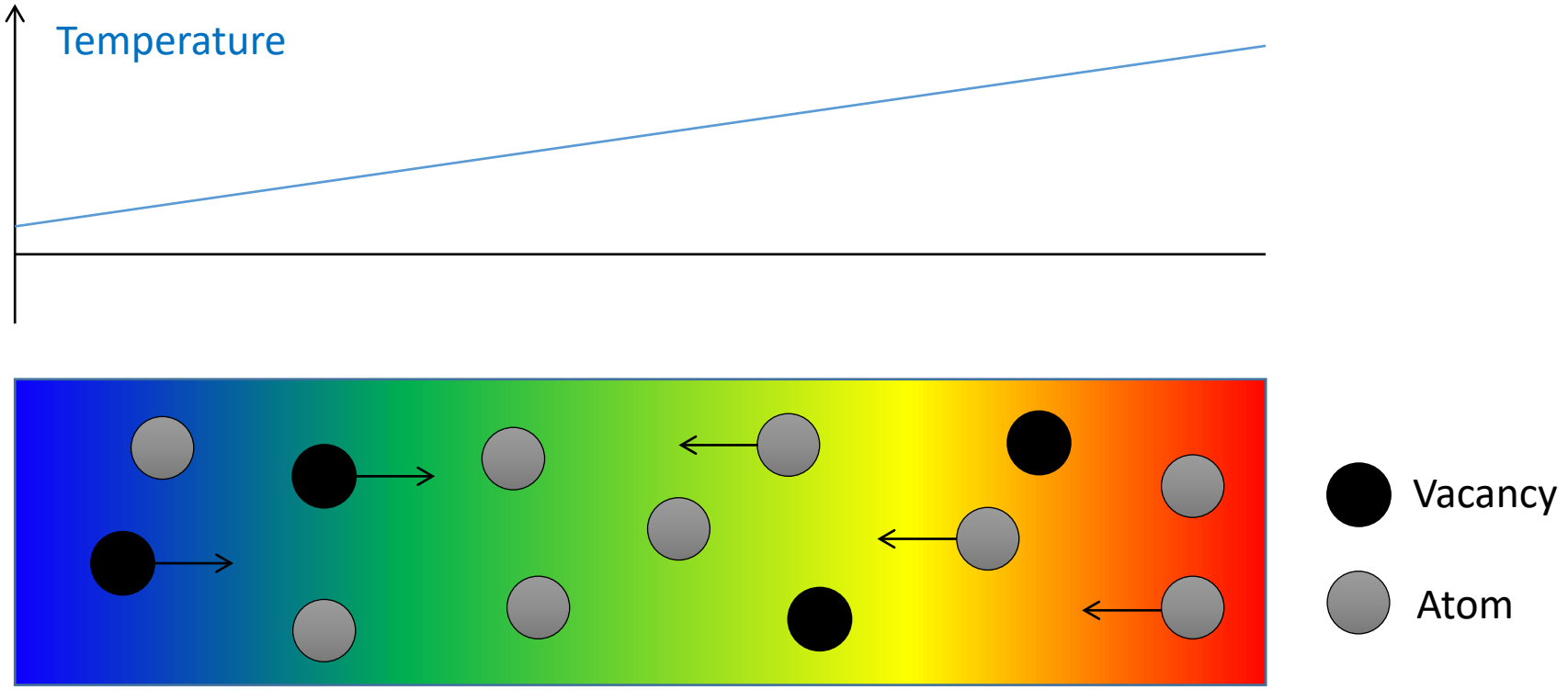


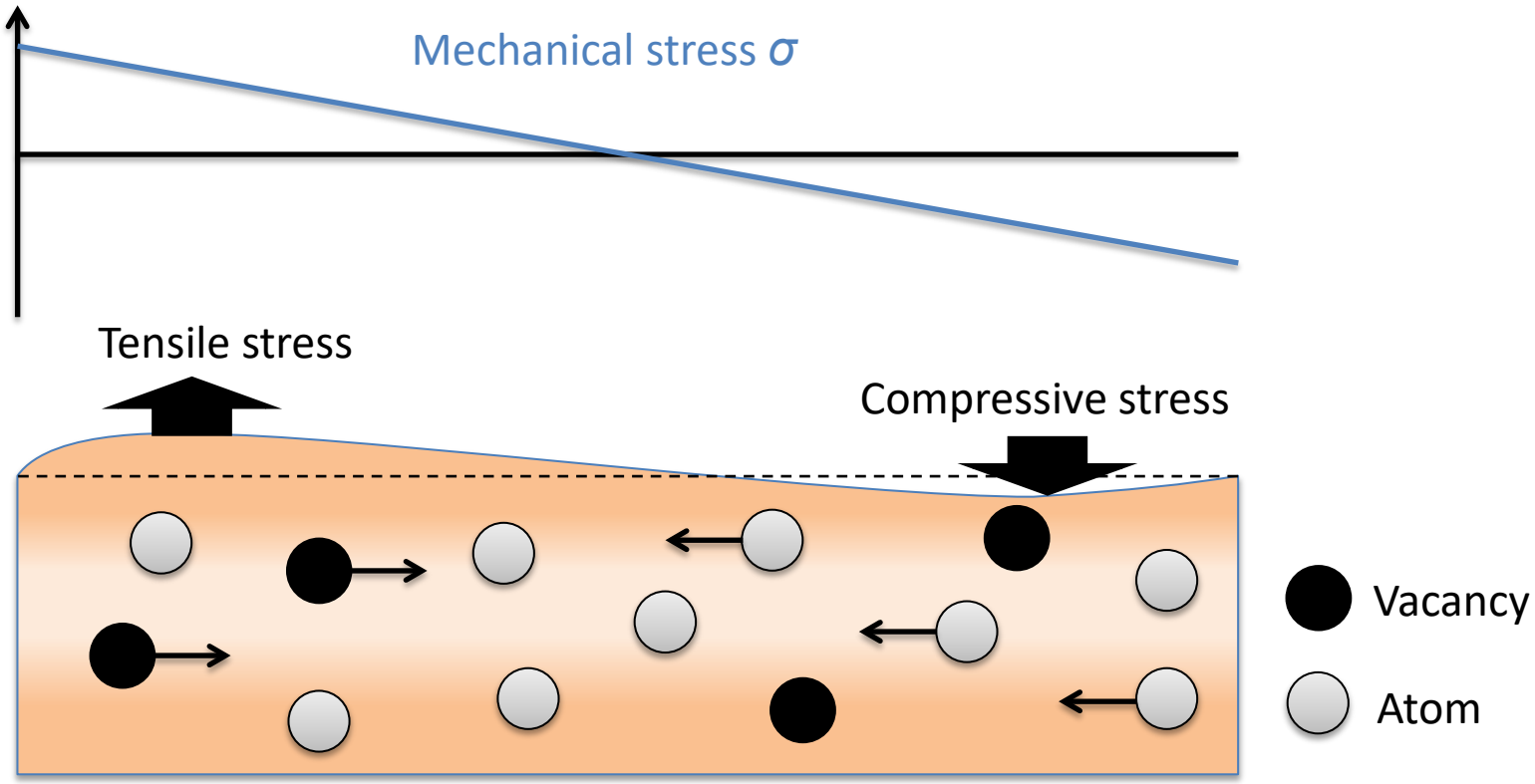
Line Depletion

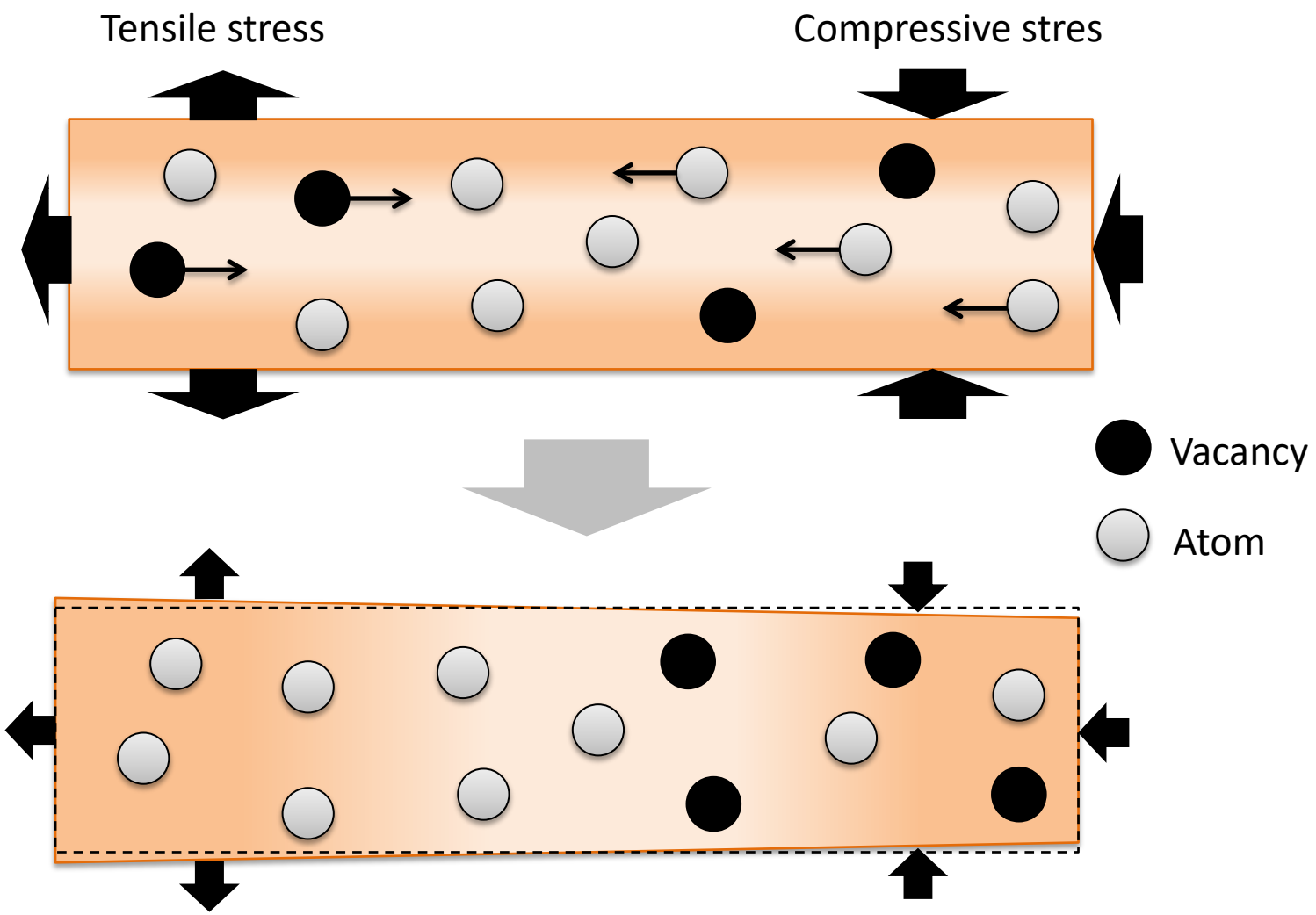


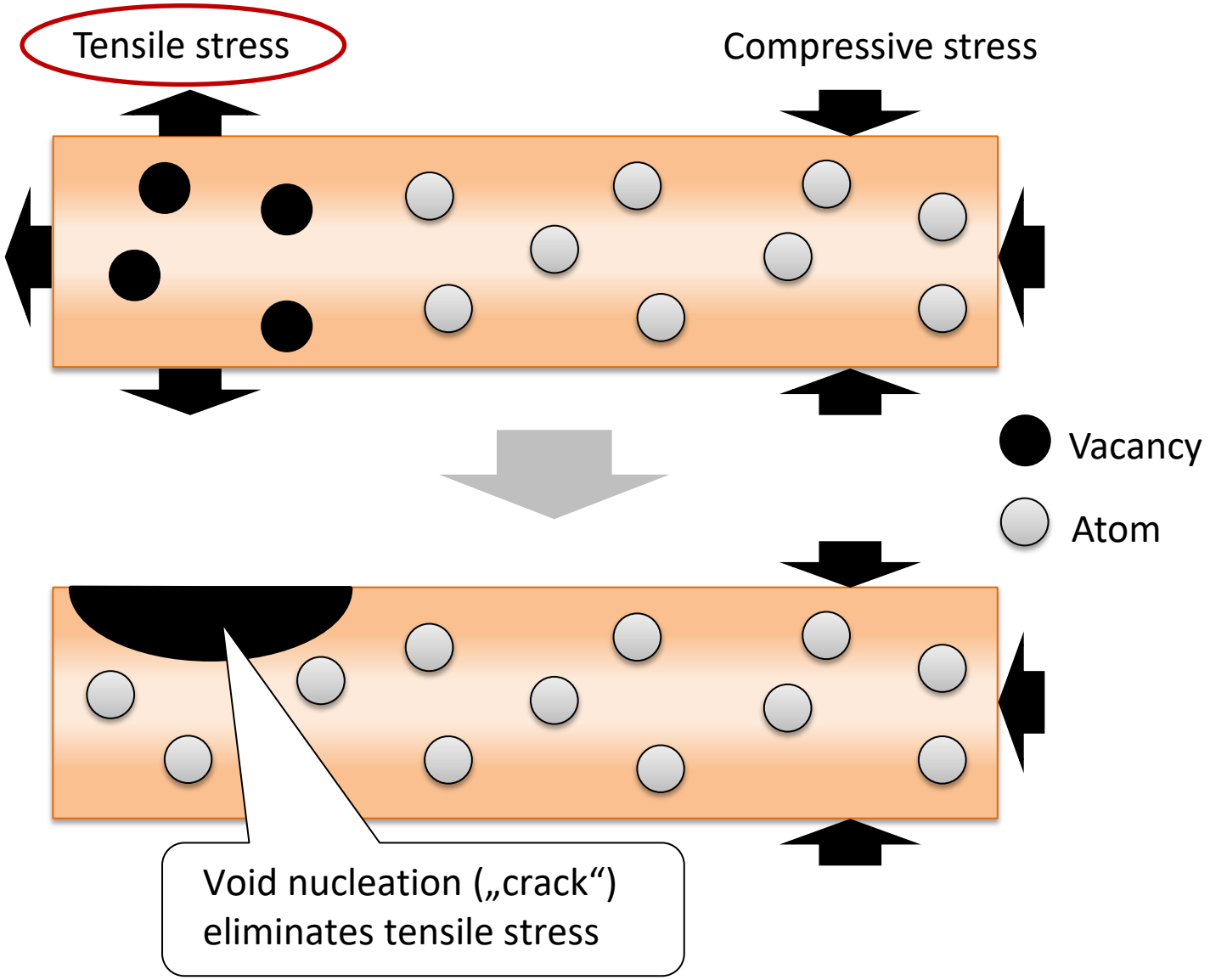
Via Depletion

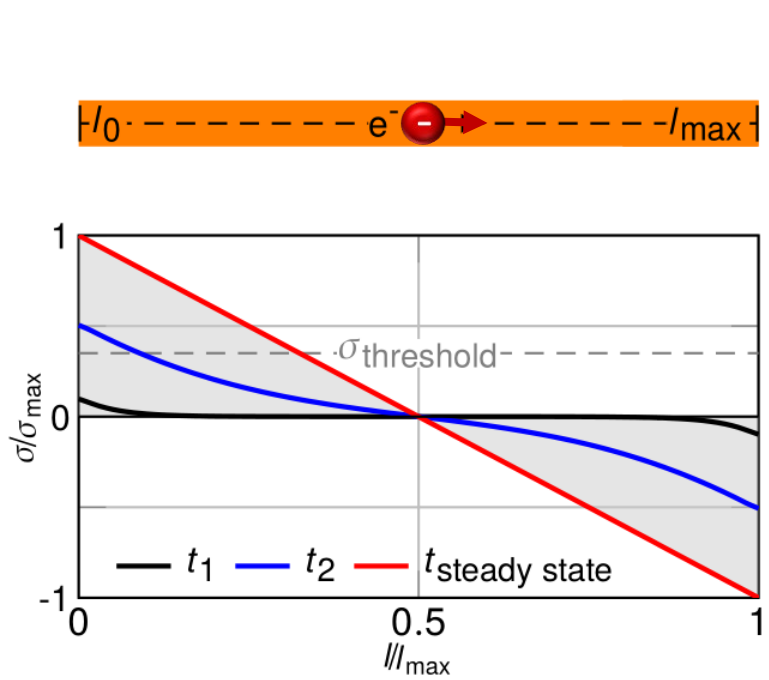


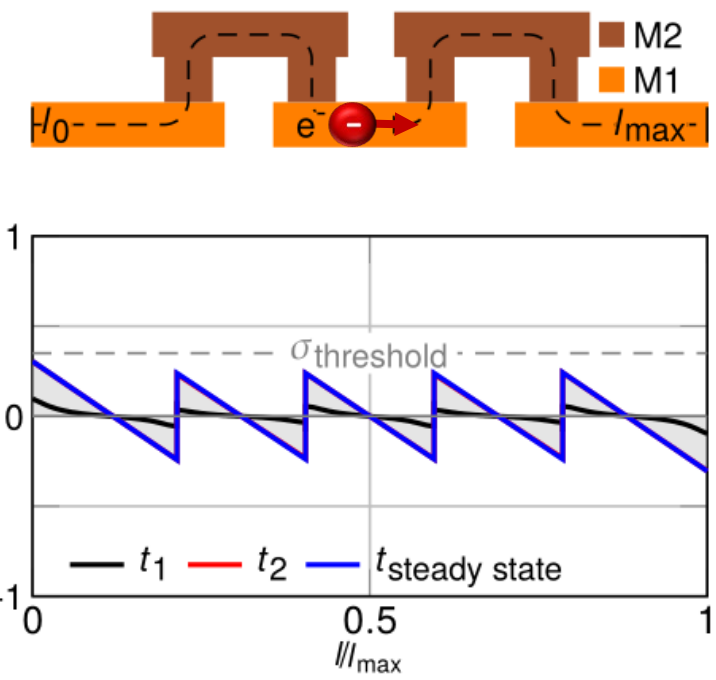


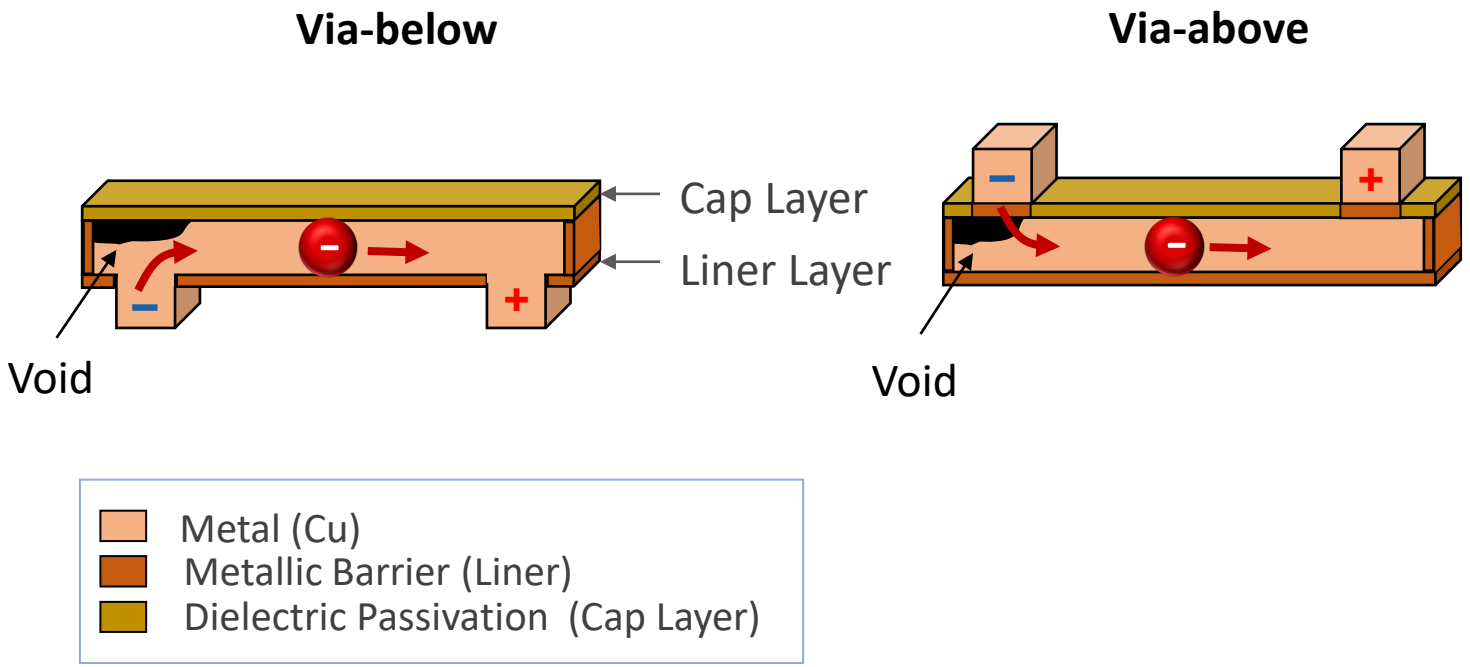


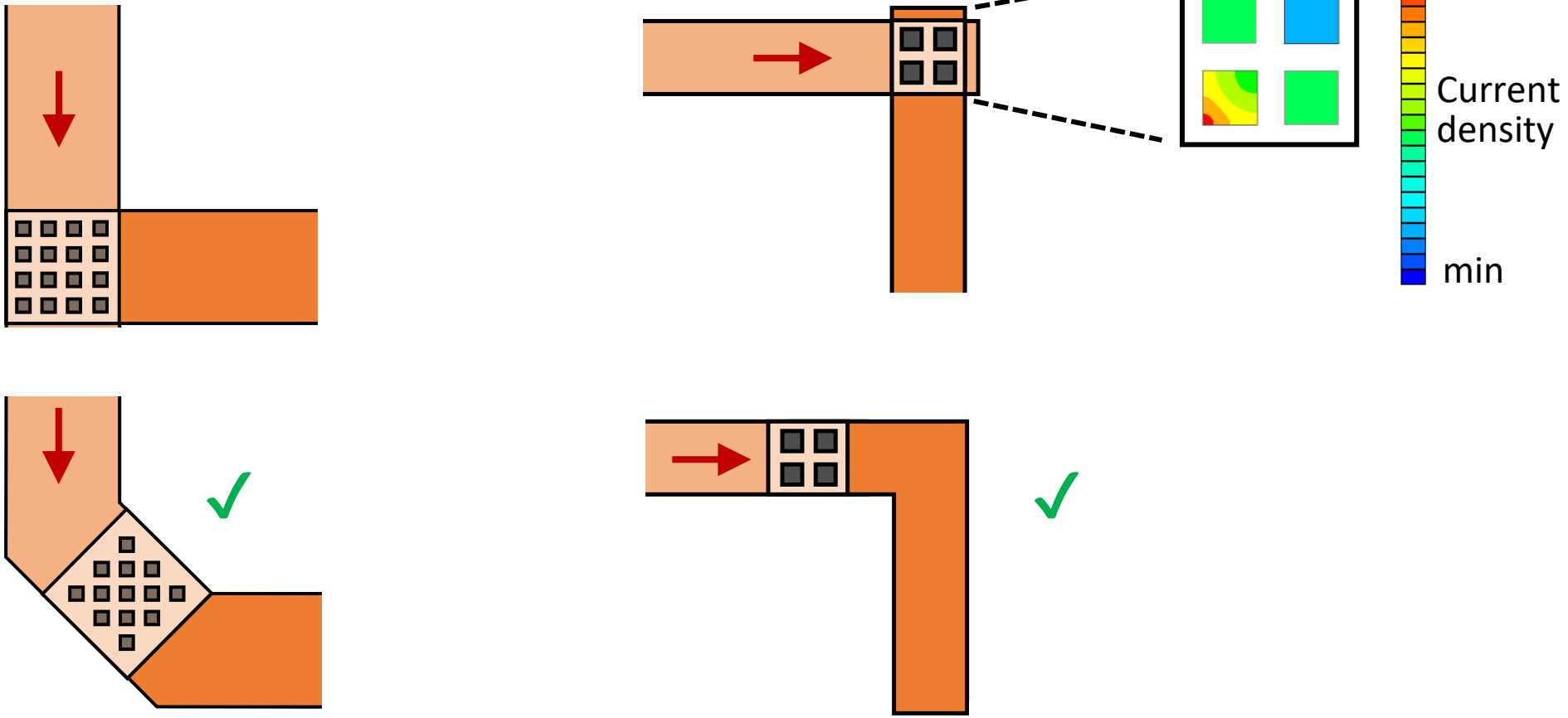


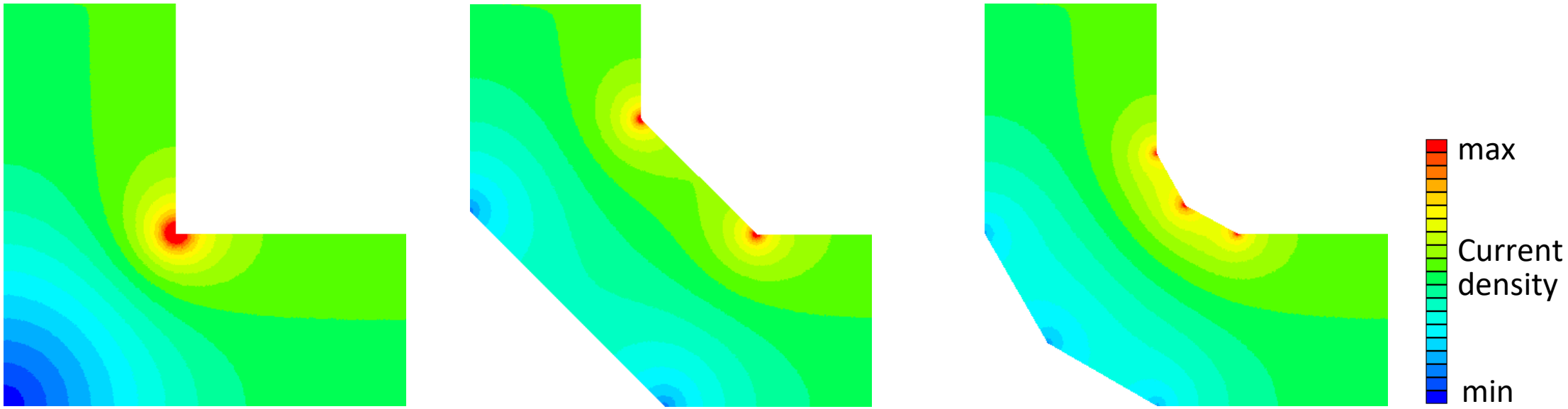


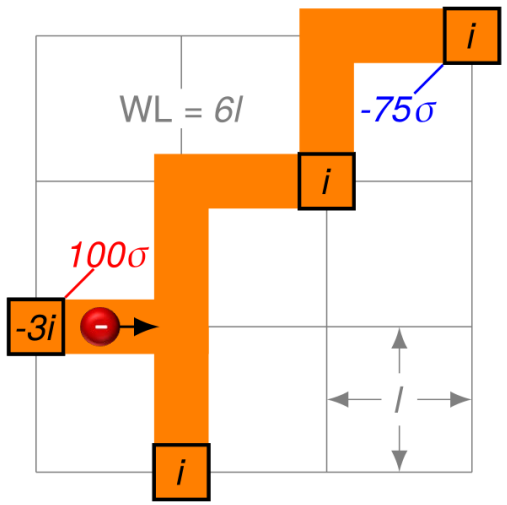




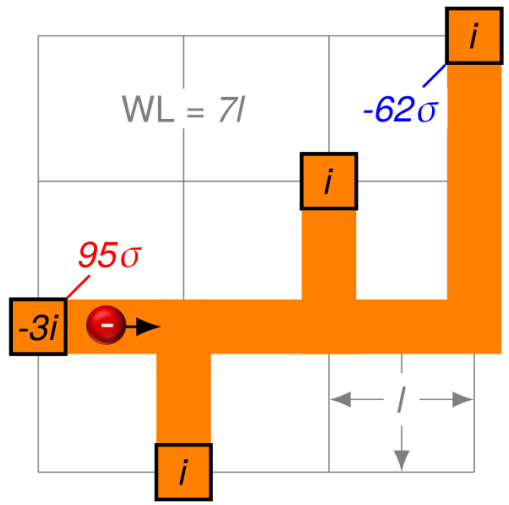




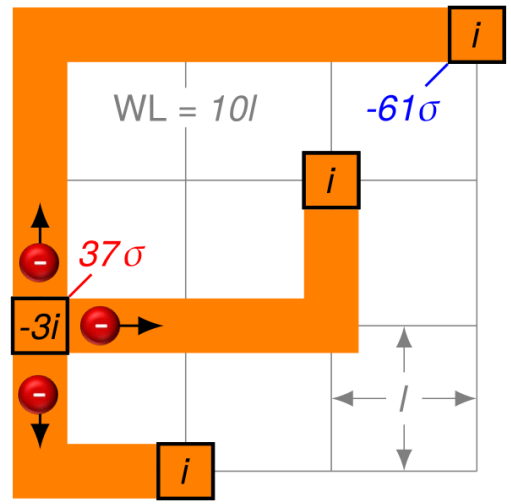




RMST net topology



Trunk net topology



Current-optimized net topology