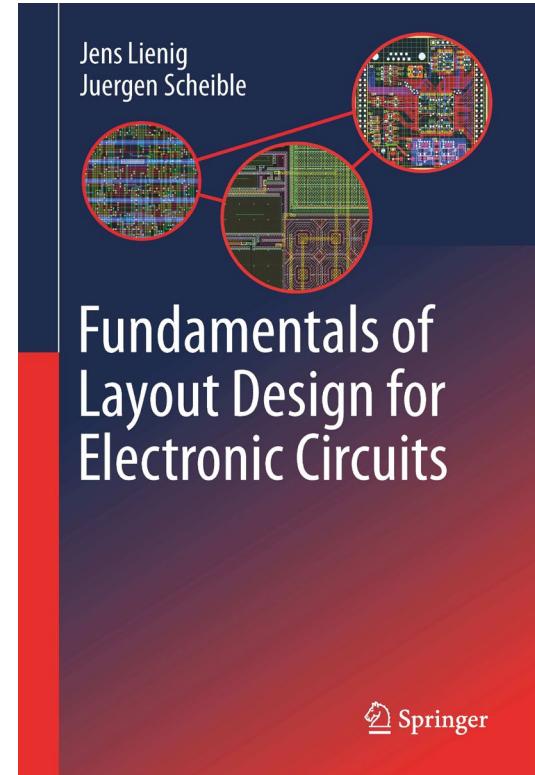


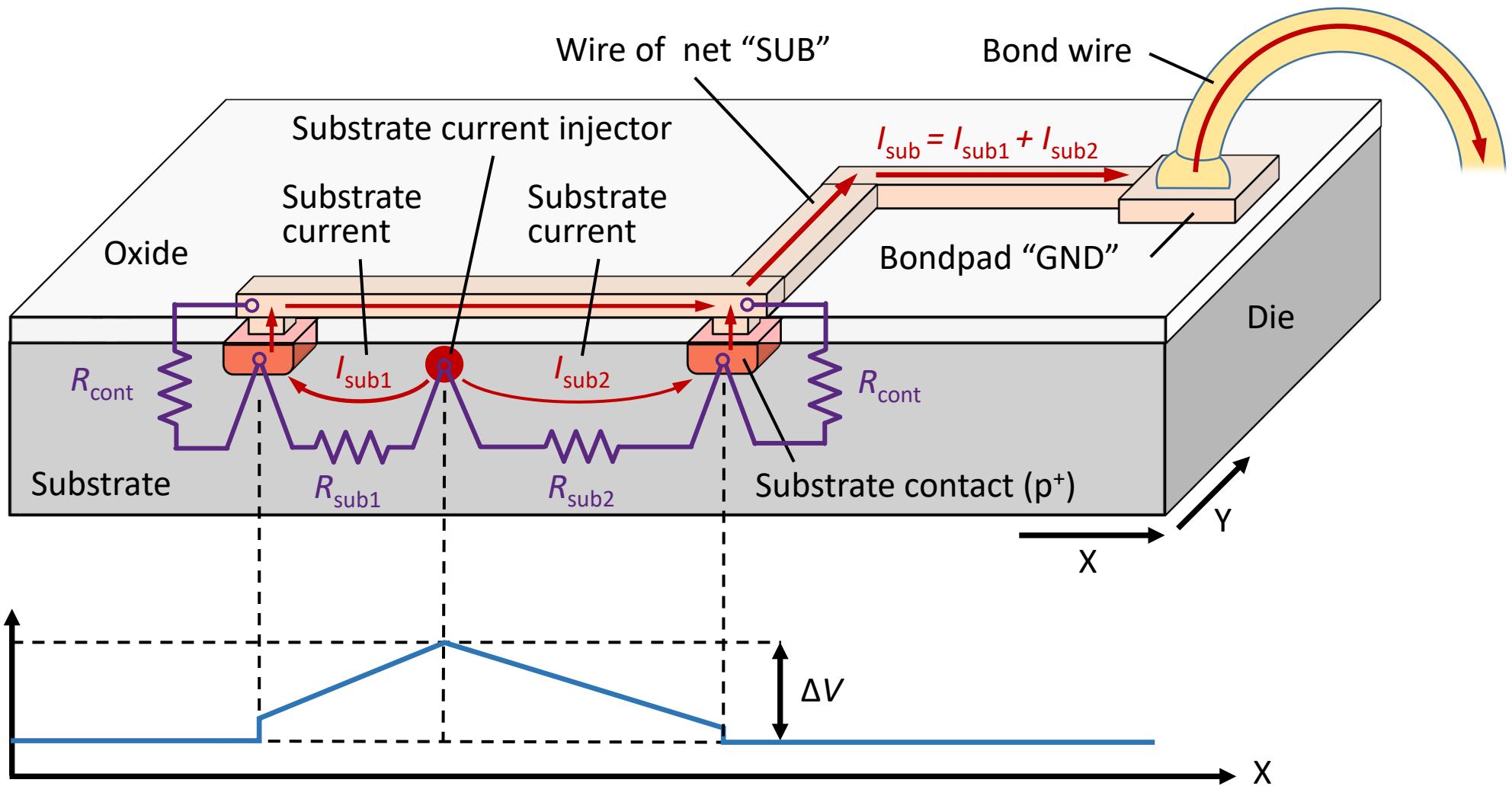
Chapter 7: Addressing Reliability in Physical Design

- 7.1 Parasitic Effects in Silicon
- 7.2 Surface Effects
- 7.3 Interconnect Parasitics
- 7.4 Overvoltage Protection
- 7.5 Migration Effects in Metal



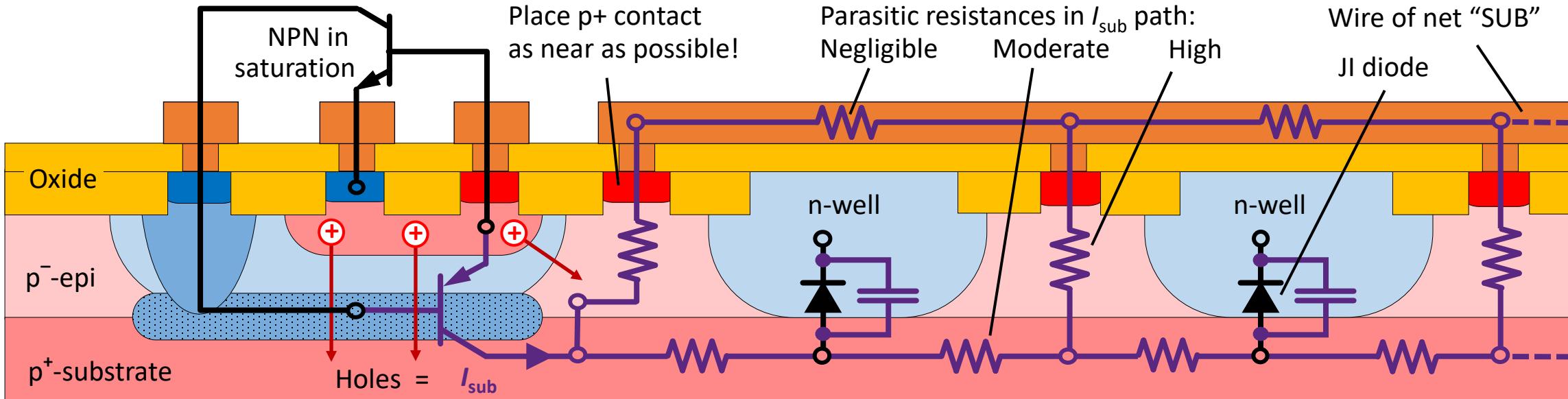
Chapter 7: Addressing Reliability in Physical Design

- 7.1 Parasitic Effects in Silicon**
 - 7.1.1 Substrate Debiasing
 - 7.1.2 Injection of Minority Carriers
 - 7.1.3 Latchup
 - 7.1.4 Breakdown Voltage aka Blocking Capability of p-n Junctions
- 7.2 Surface Effects**
 - 7.2.1 Parasitic Channel Effects
 - 7.2.2 Hot Carrier Injection
- 7.3 Interconnect Parasitics**
 - 7.3.1 Line Losses
 - 7.3.2 Signal Distortions
 - 7.3.3 Crosstalk
- 7.4 Overvoltage Protection**
 - 7.4.1 Electrostatic Discharge (ESD)
 - 7.4.2 Antenna Effect
- 7.5 Migration Effects in Metal**
 - 7.5.1 Electromigration
 - 7.5.2 Thermal Migration
 - 7.5.3 Stress Migration
 - 7.5.4 Mitigating Electromigration
 - 7.5.5 Mitigating Thermal and Stress Migration

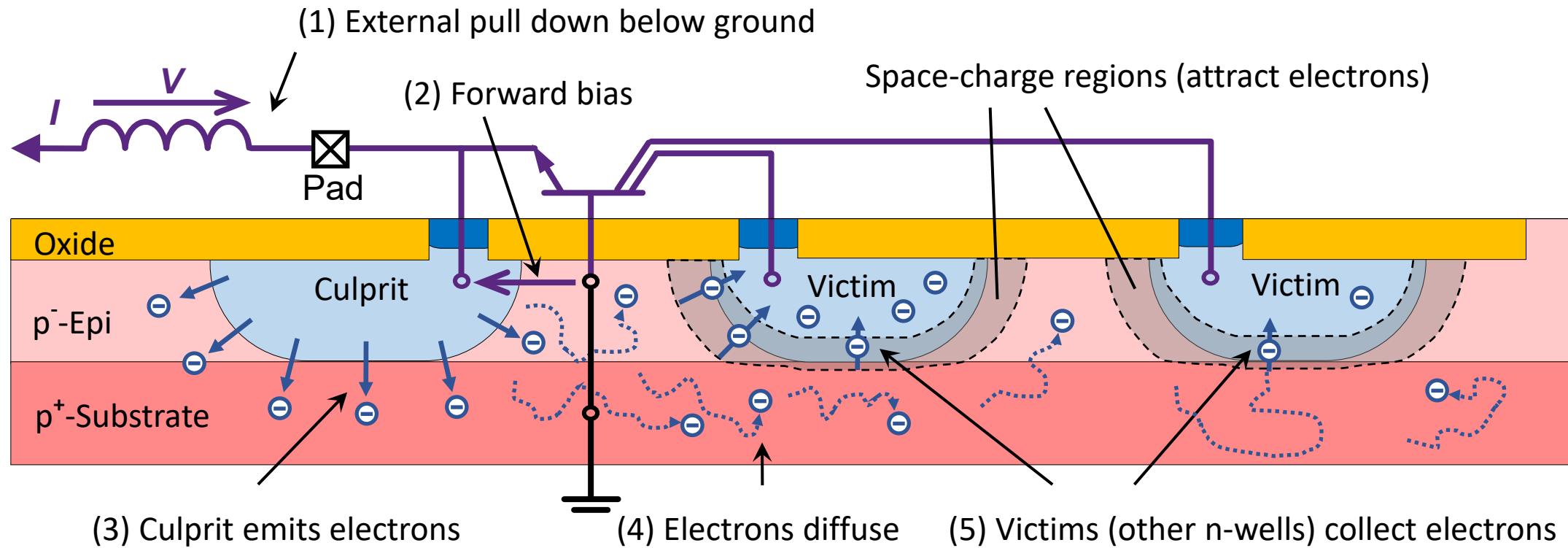


Metal (wire)
Oxide (SiO_2)
n^- n^+ n-doped bulk silicon
p^- p^+ p-doped bulk silicon

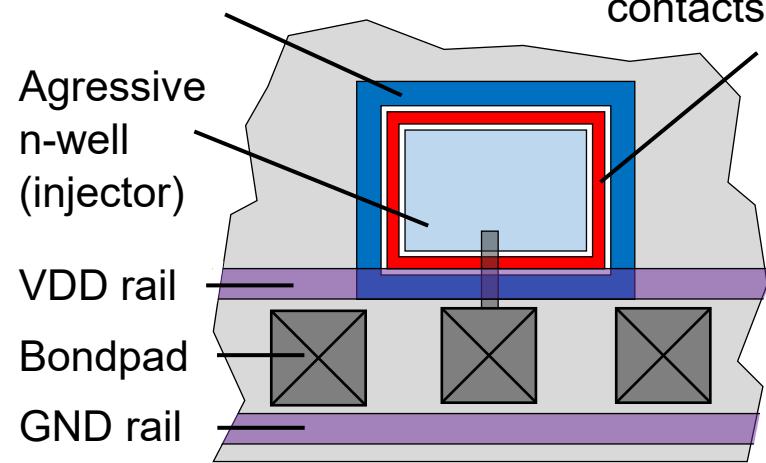
Ref. A



Ref. B

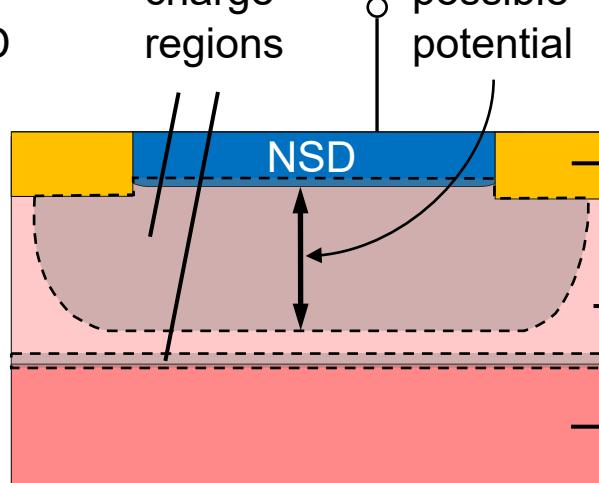


Electron-collecting guard ring (**NSD**) tied to V_{DD}

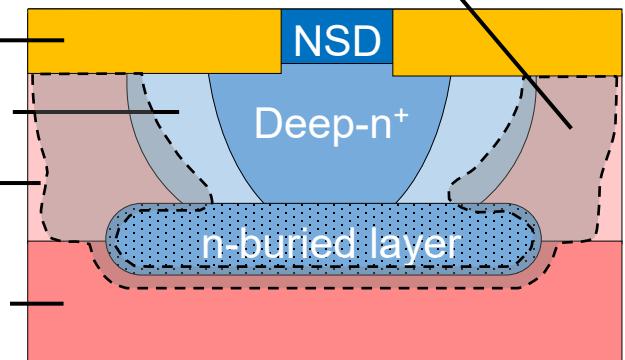


Hole-providing guard ring (**PSD** substrate contacts) tied to GND

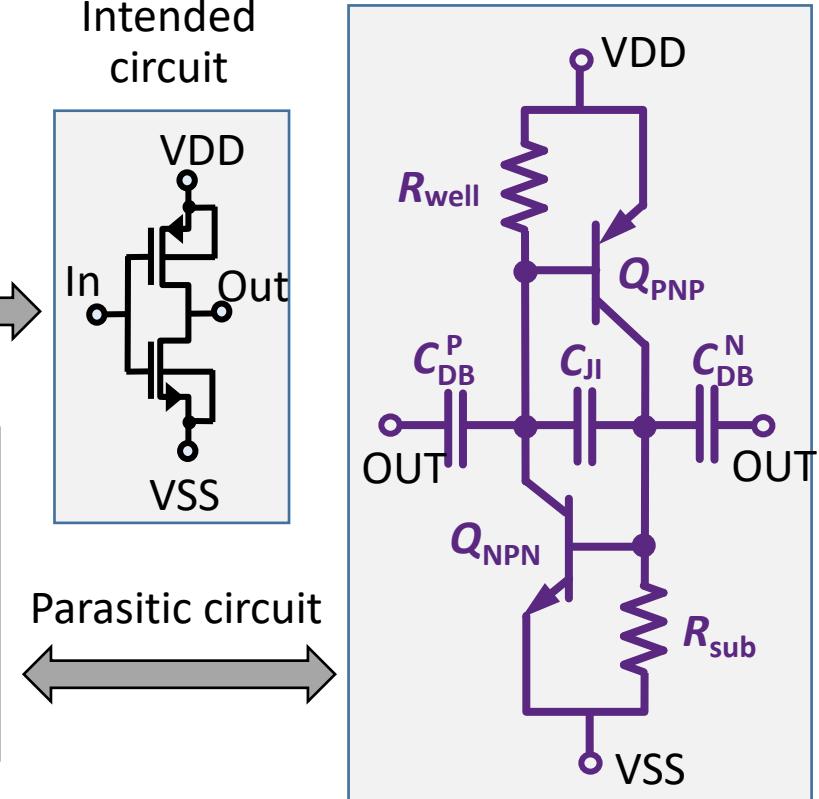
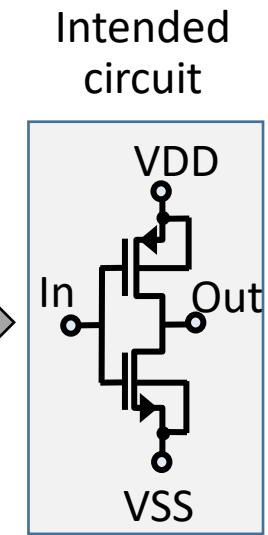
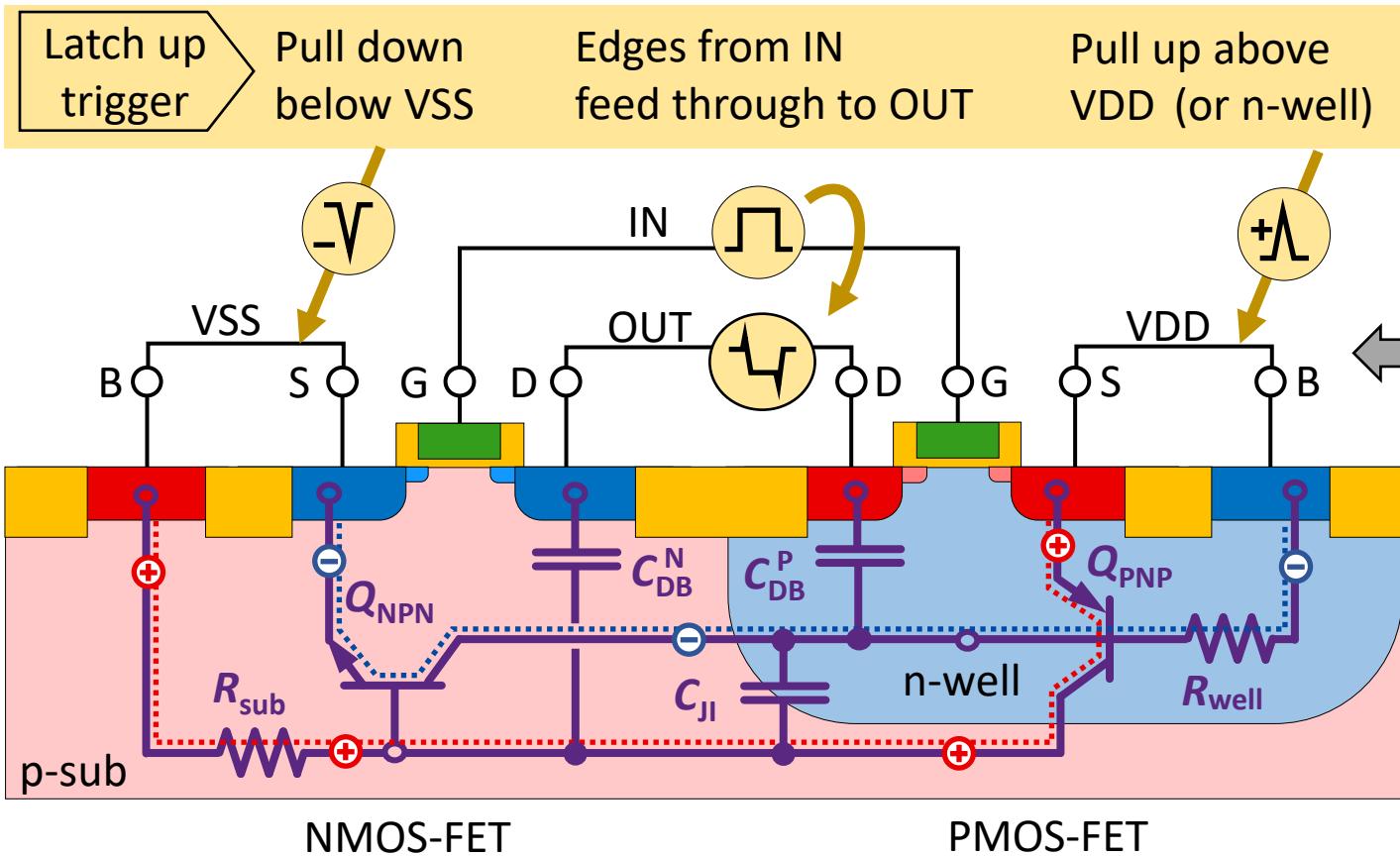
Space-charge regions
Highest possible potential

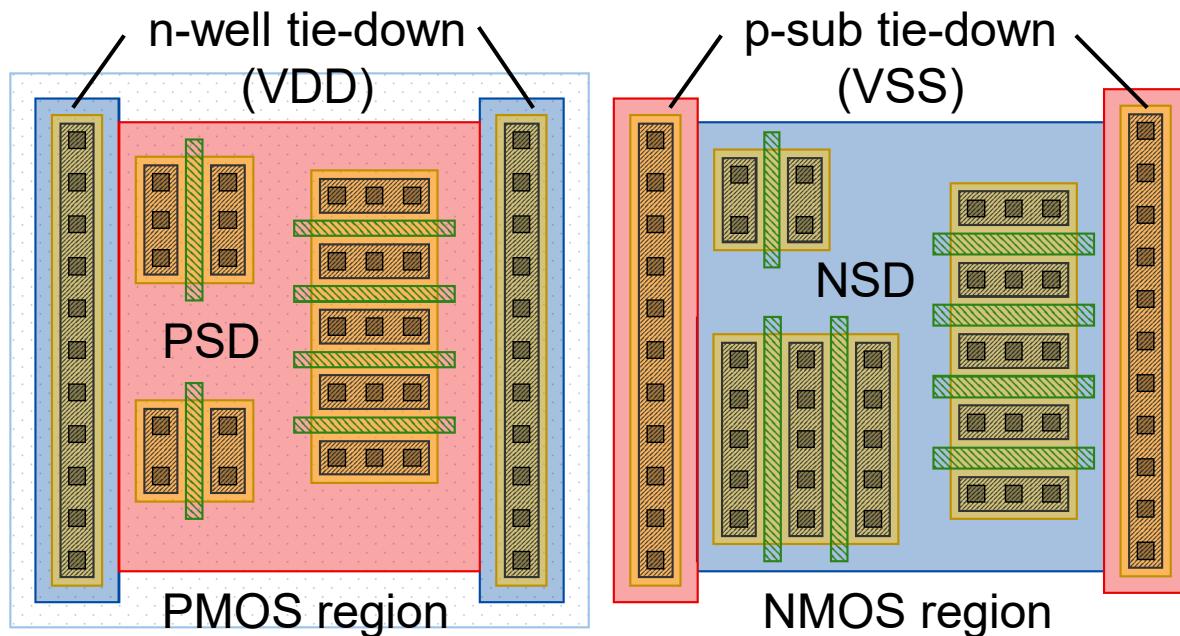
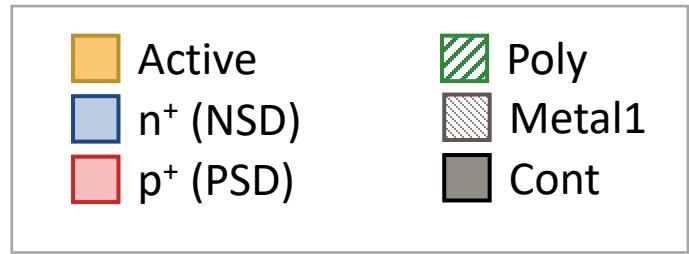


Space-charge region

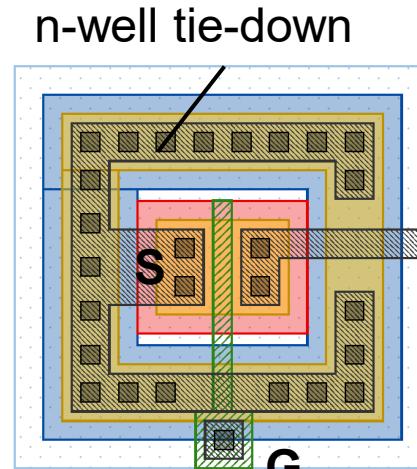


The diagram illustrates a cross-section of a p-n junction diode. It consists of several distinct layers: a green layer at the top labeled "Poly (gate)", followed by a yellow layer labeled "Oxide (SiO_2)". Below these is a blue layer labeled "n⁻" which is identified as "n-doped bulk silicon". At the bottom is a red layer labeled "p⁻" which is identified as "p-doped bulk silicon".

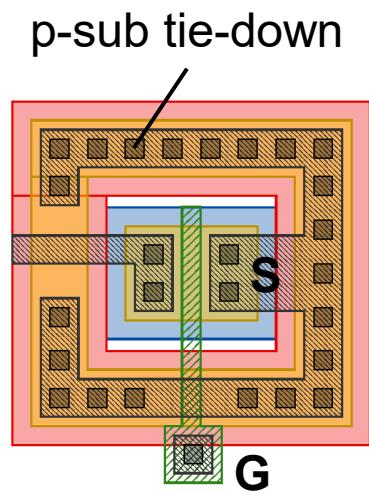




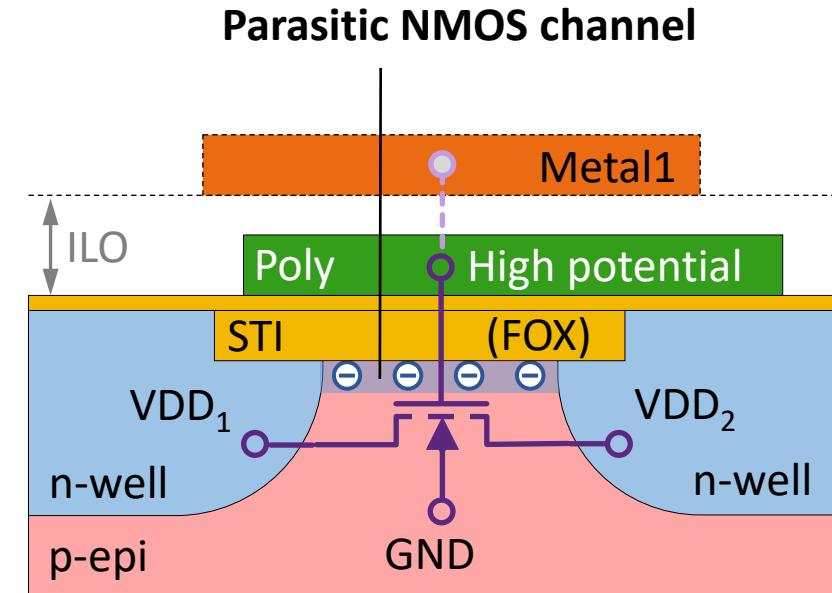
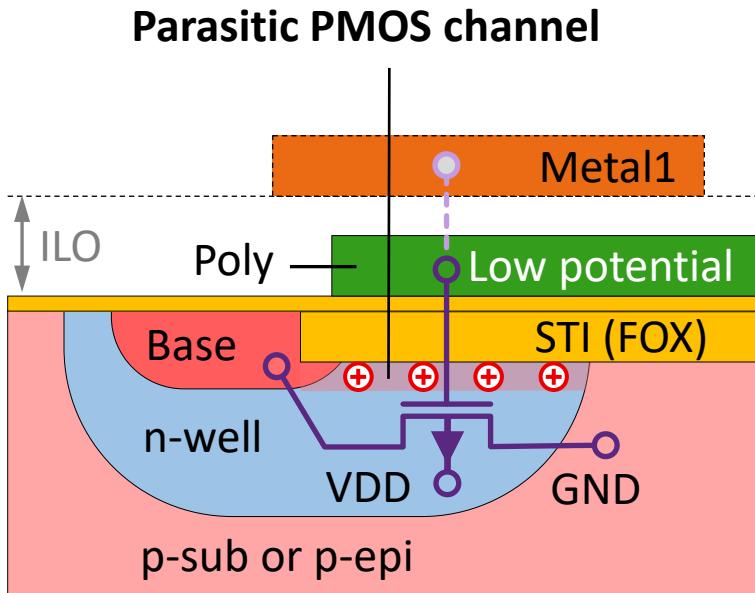
Backgate contacts laid out as guard rings

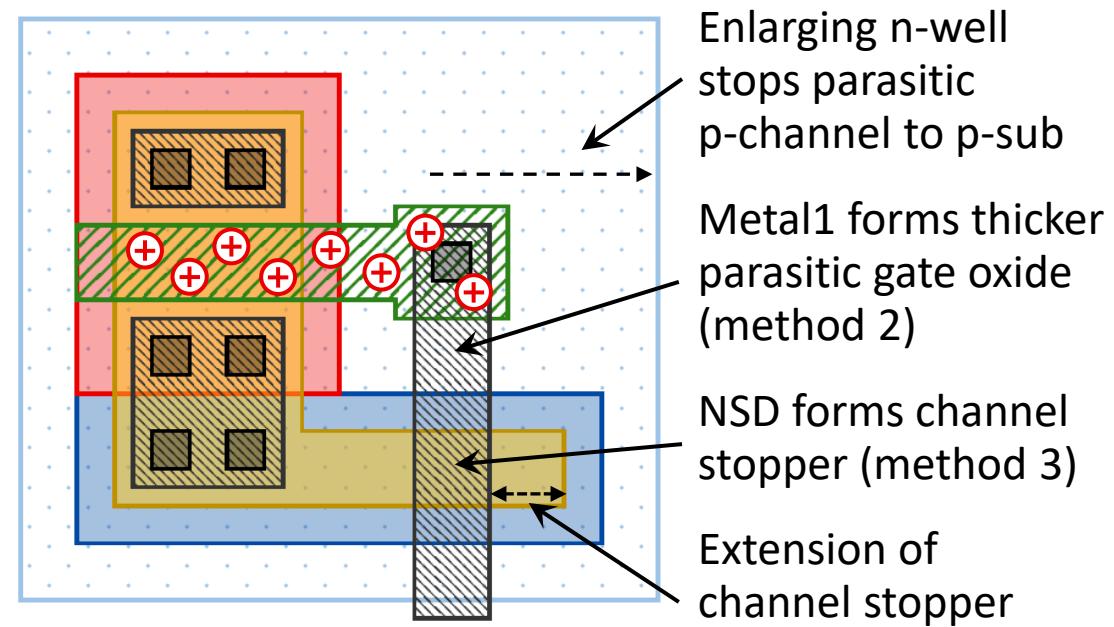
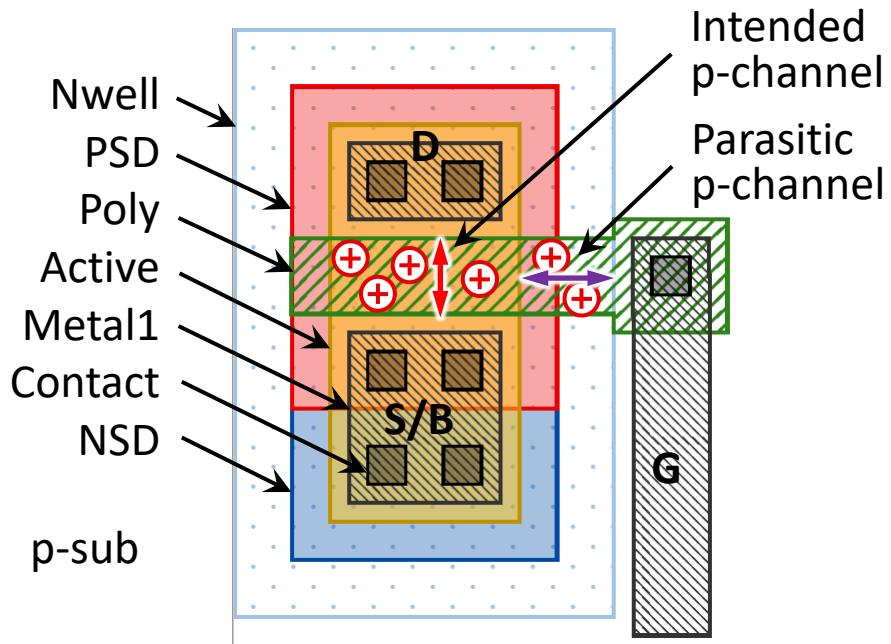


PMOS-FET

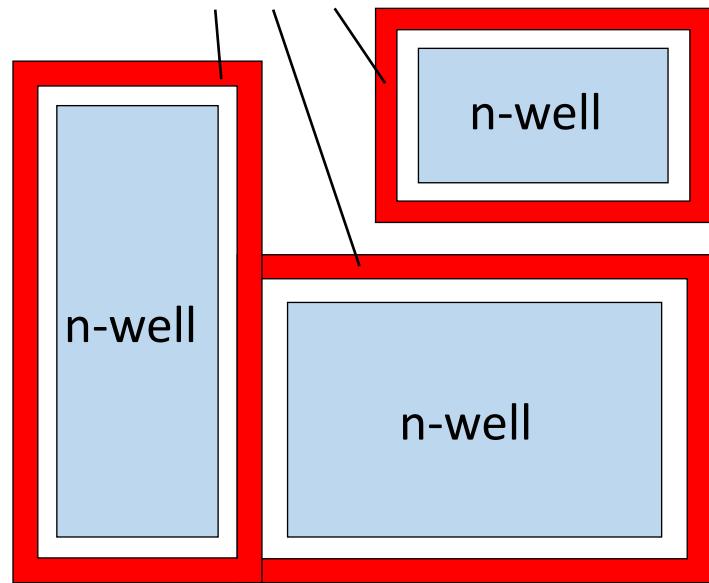


NMOS-FET

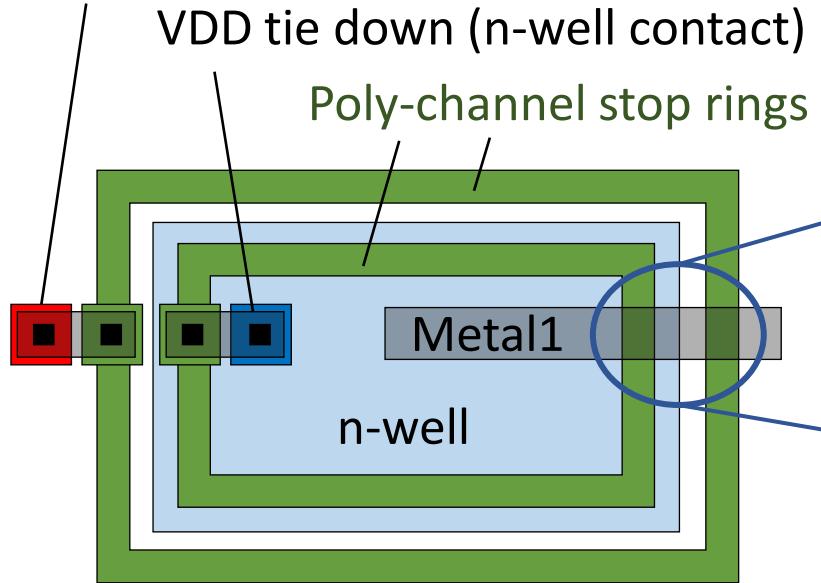




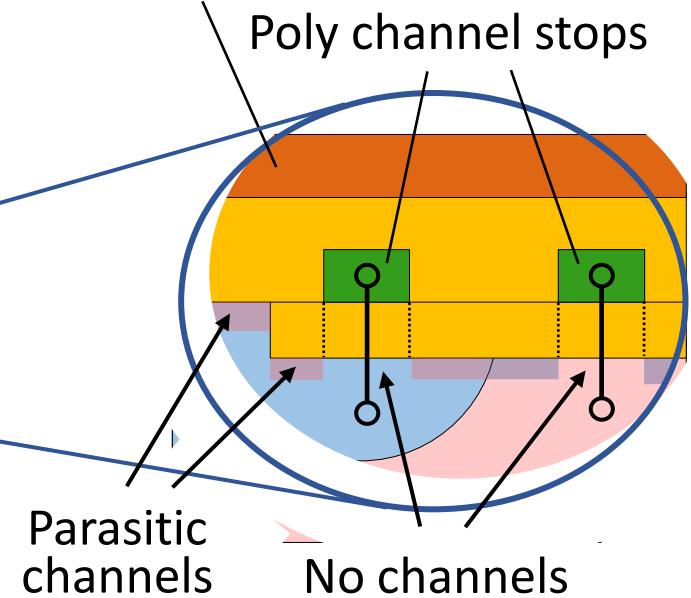
PSD-channel stop rings



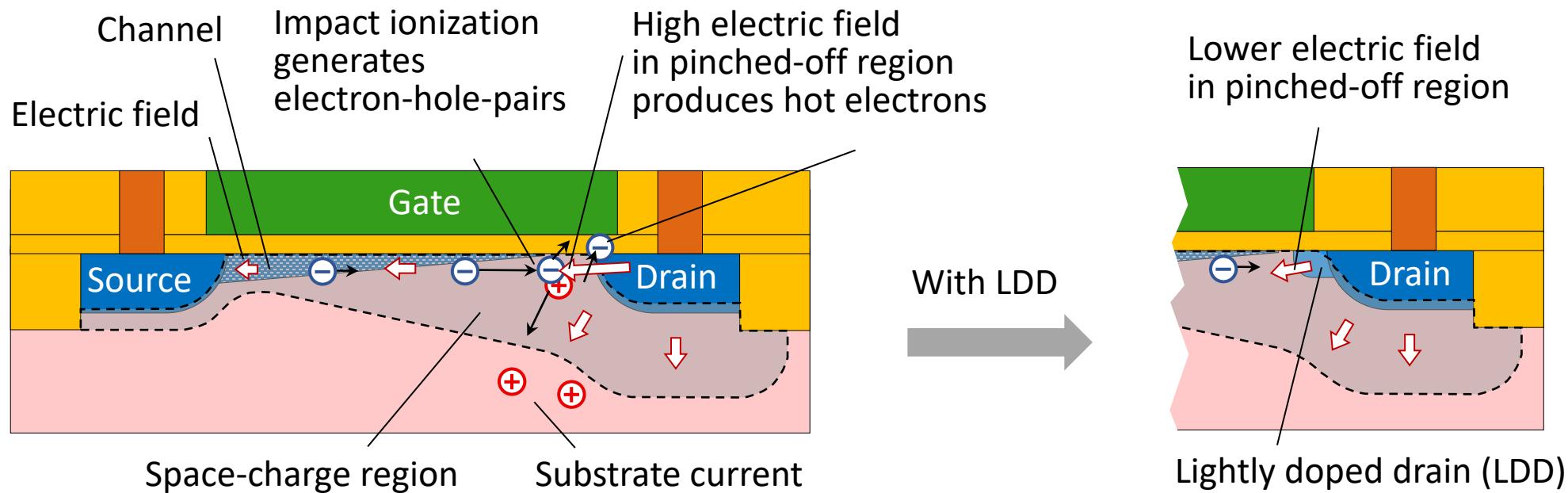
GND tie down (p-sub contact)

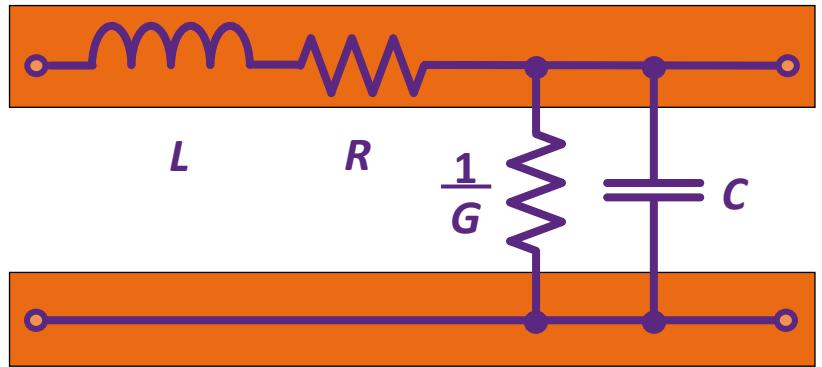


Metal1 (parasitic gate)
Poly channel stops



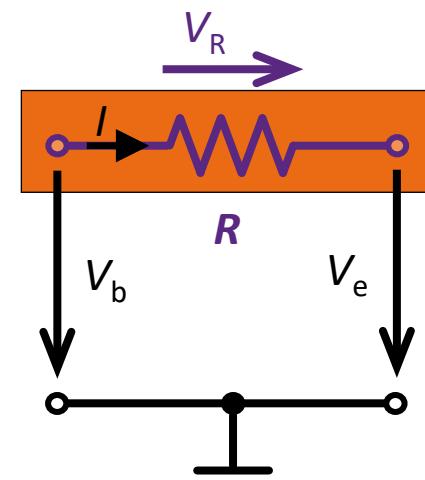
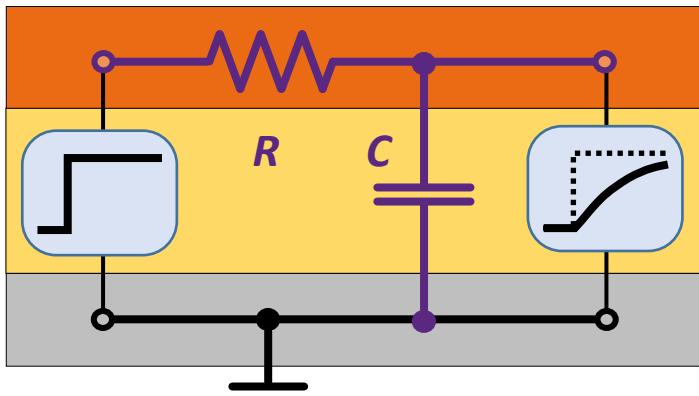
	Oxide (SiO_2)		Metal		Poly
n^-	n^+	n^- n^+	n-doped bulk silicon		
p^-	p^+	p^- p^+	p-doped bulk silicon		

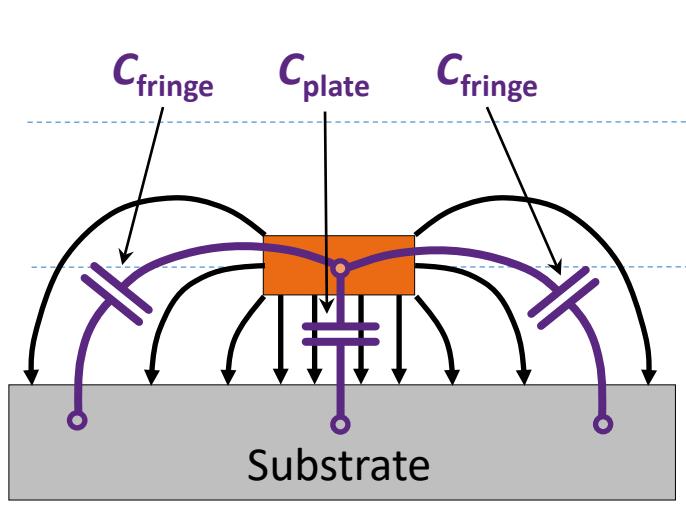




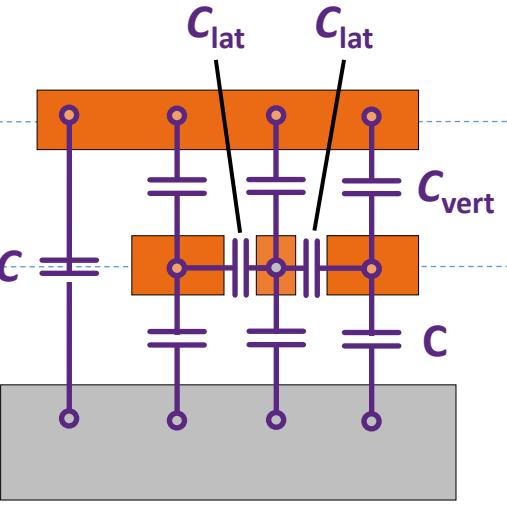
IC

Conductor
Oxide(s)
Substrate

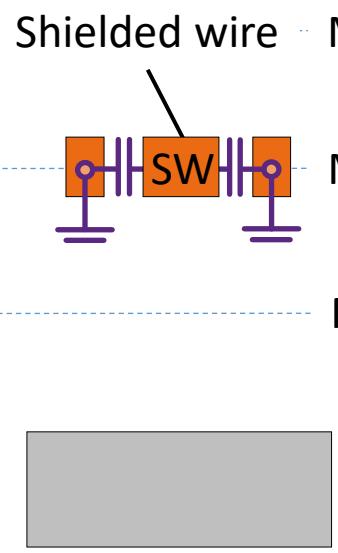




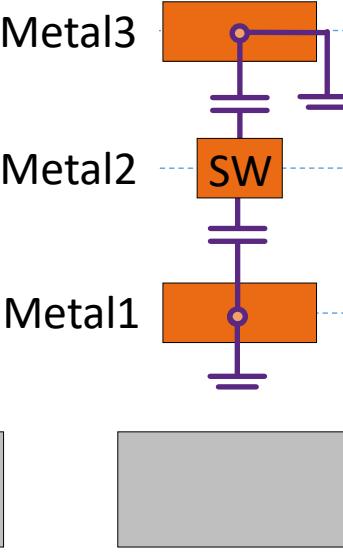
(a)



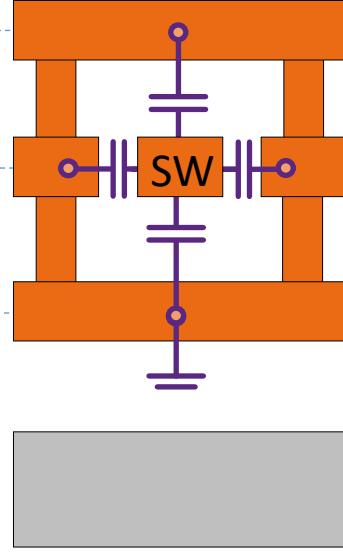
(b)



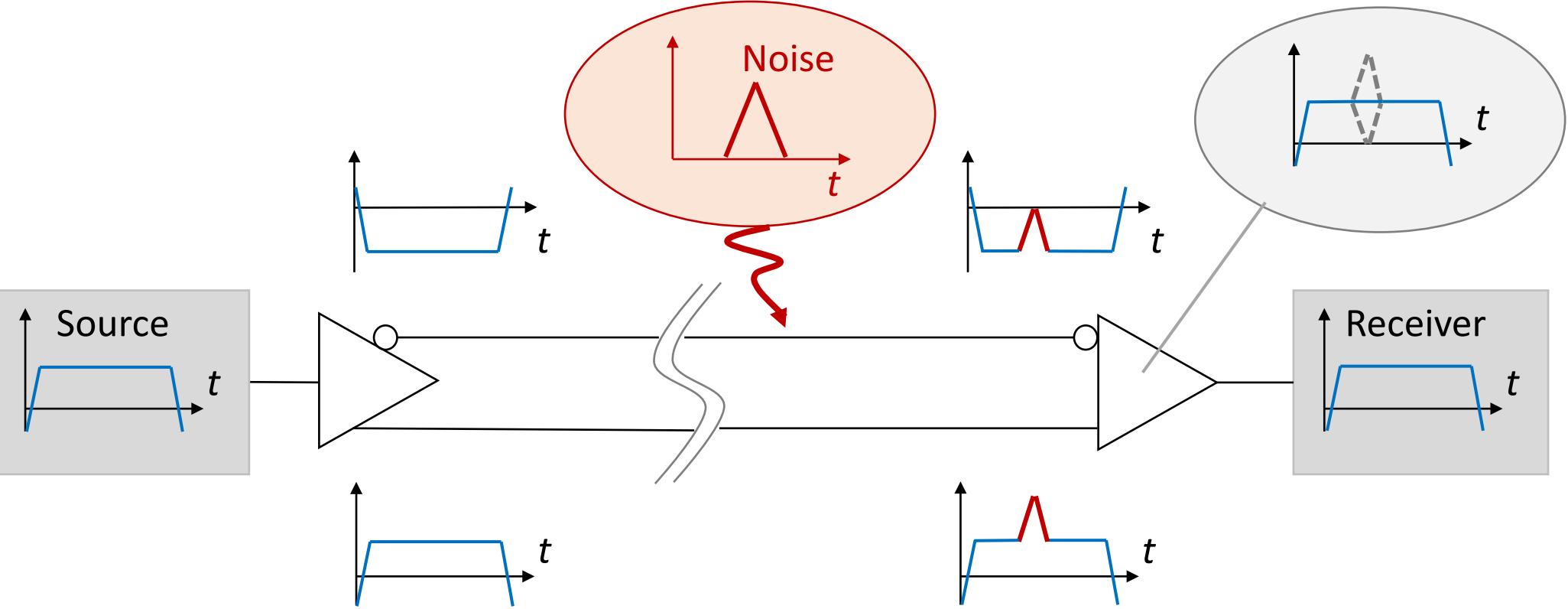
(c)

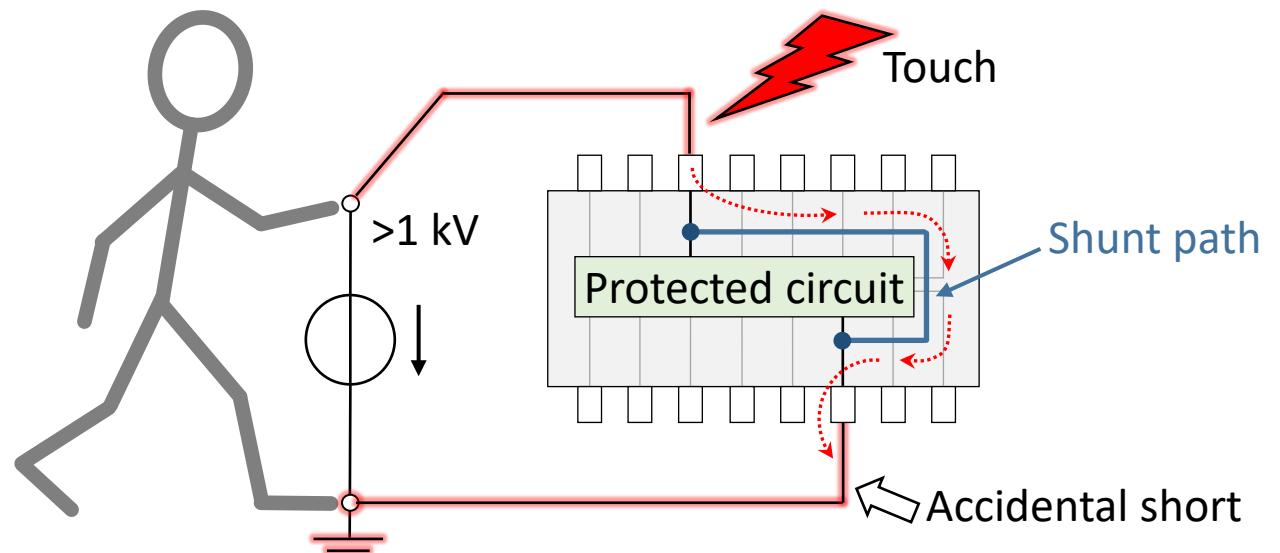
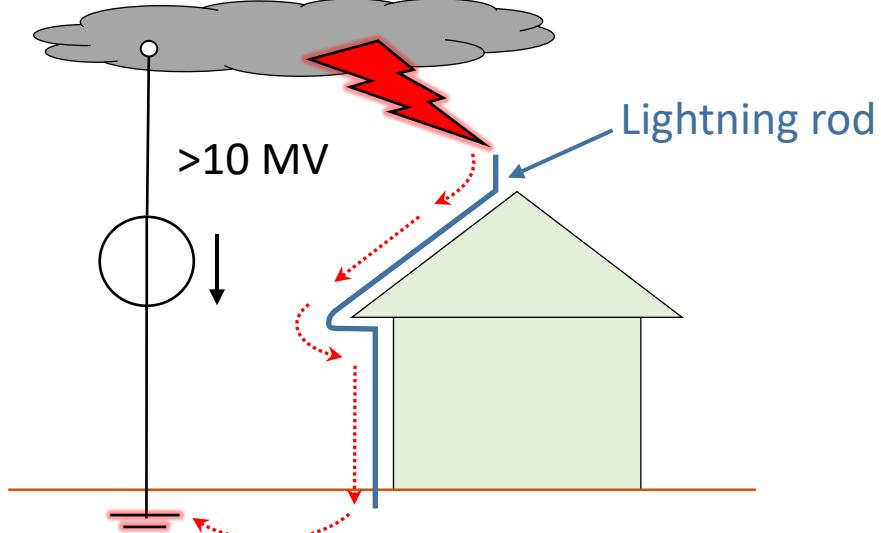


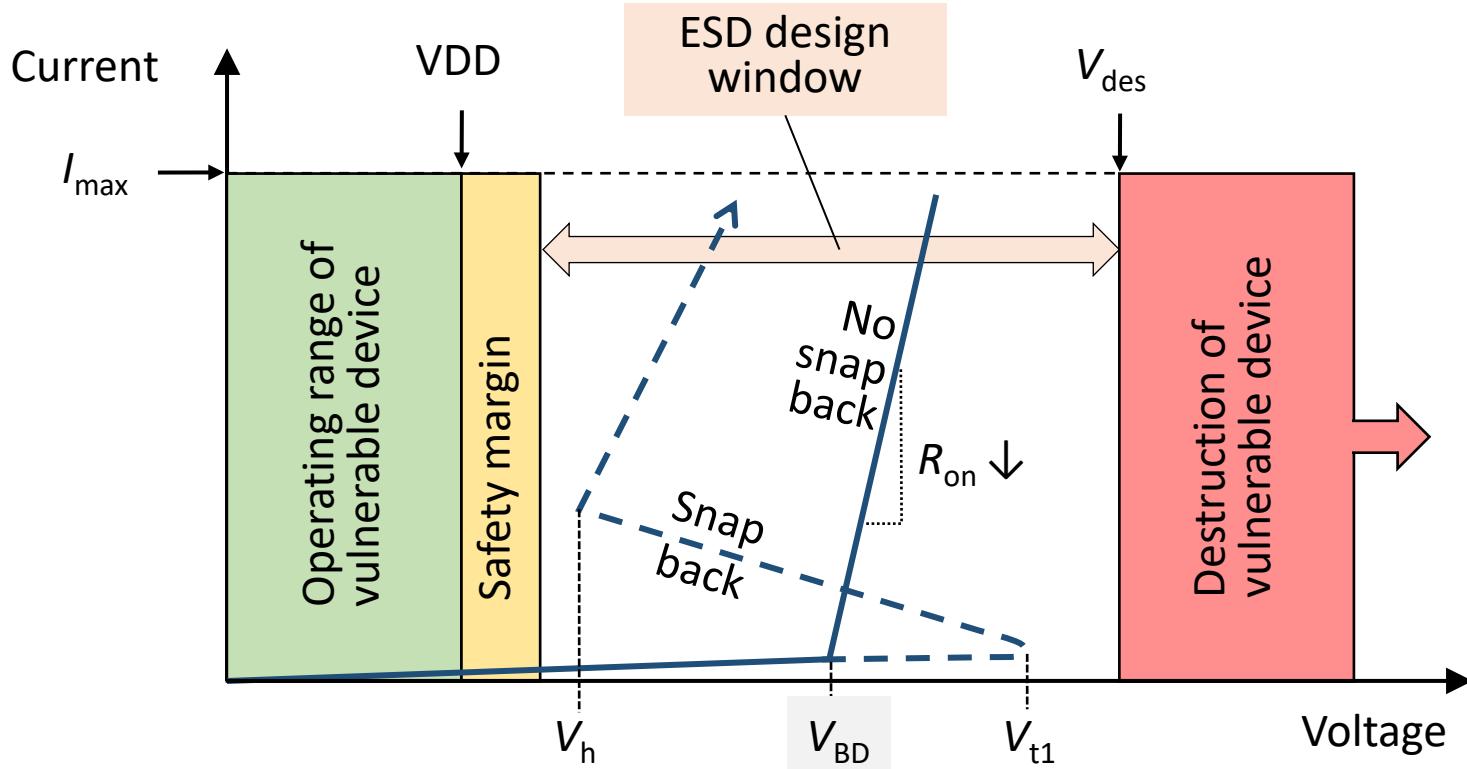
(d)



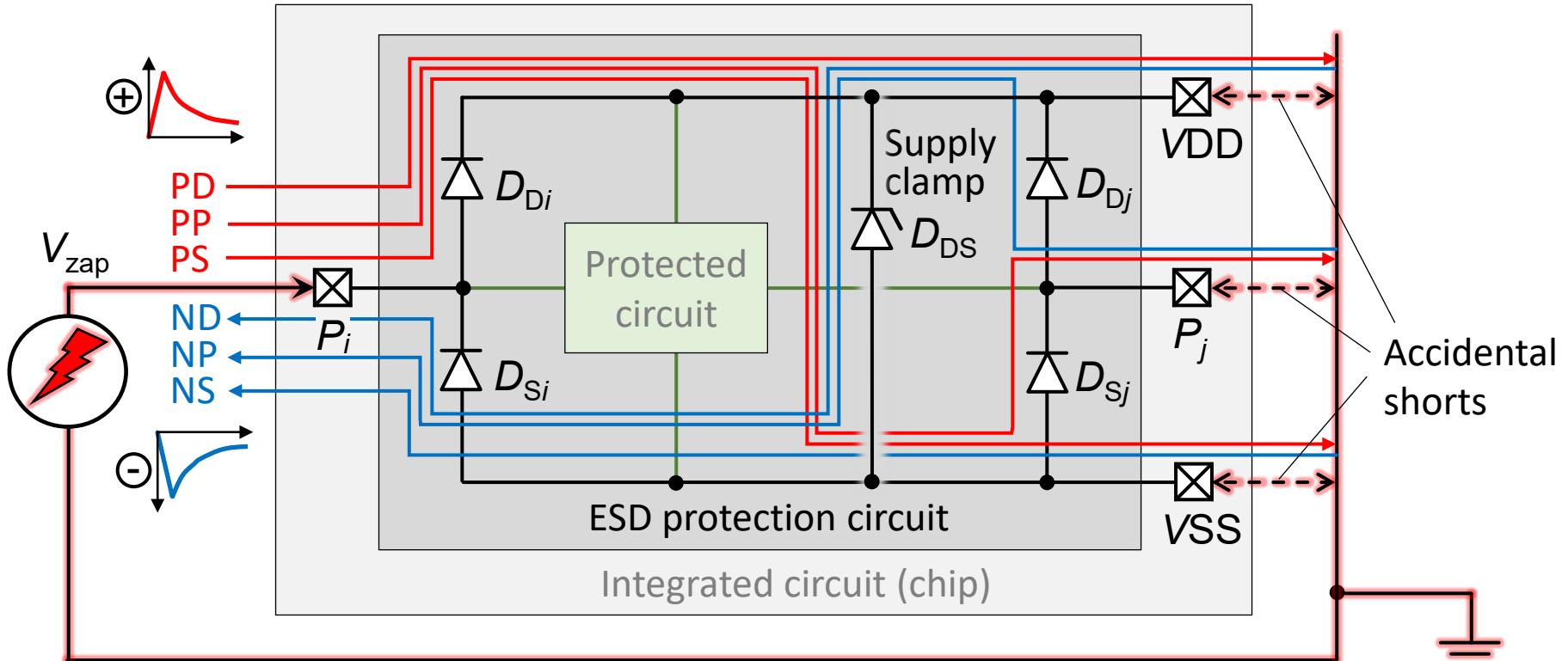
(e)

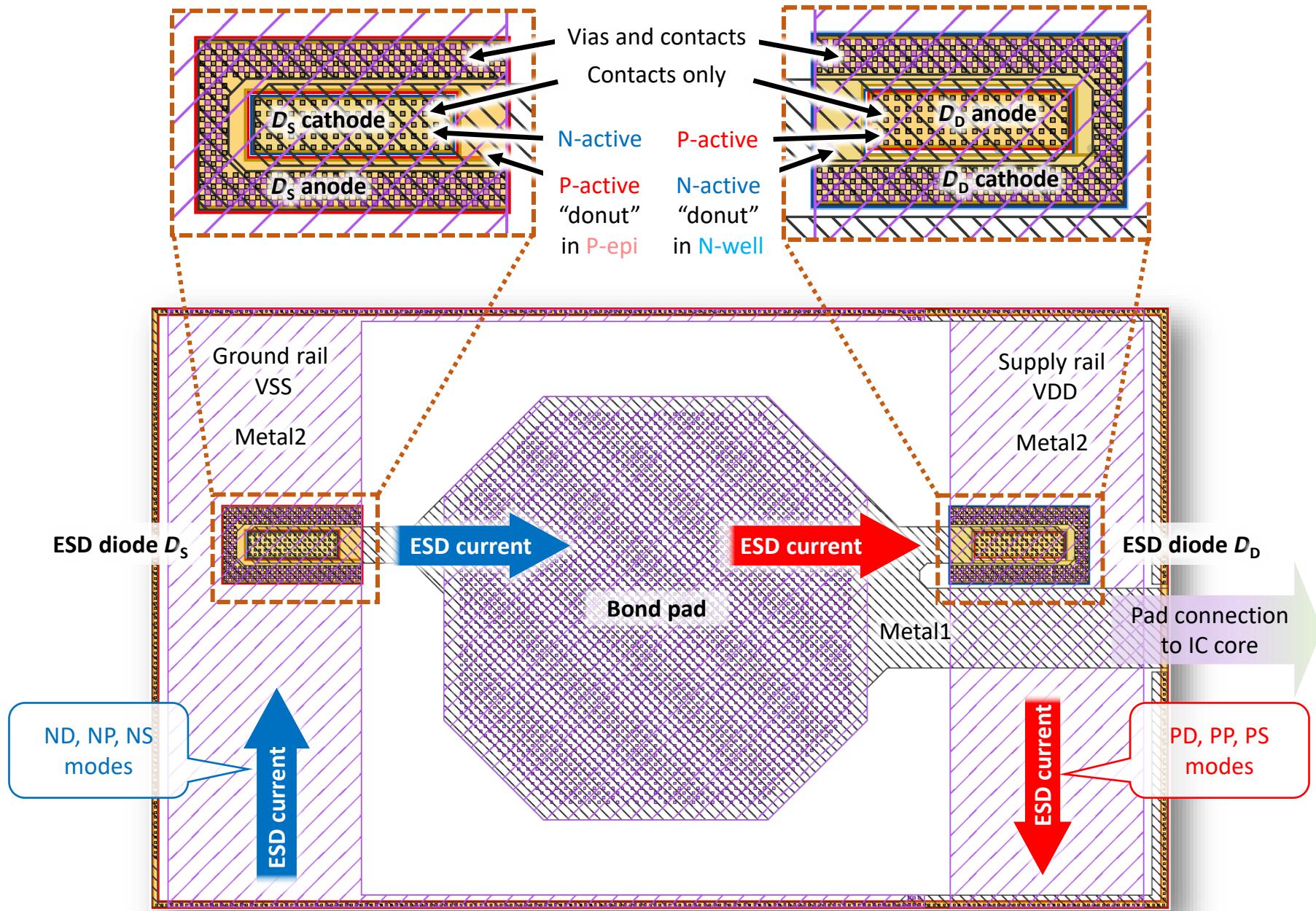






V_h	Holding voltage
V_{BD}	Breakdown voltage
V_{t1}	Trigger voltage
V_{des}	Destruction voltage

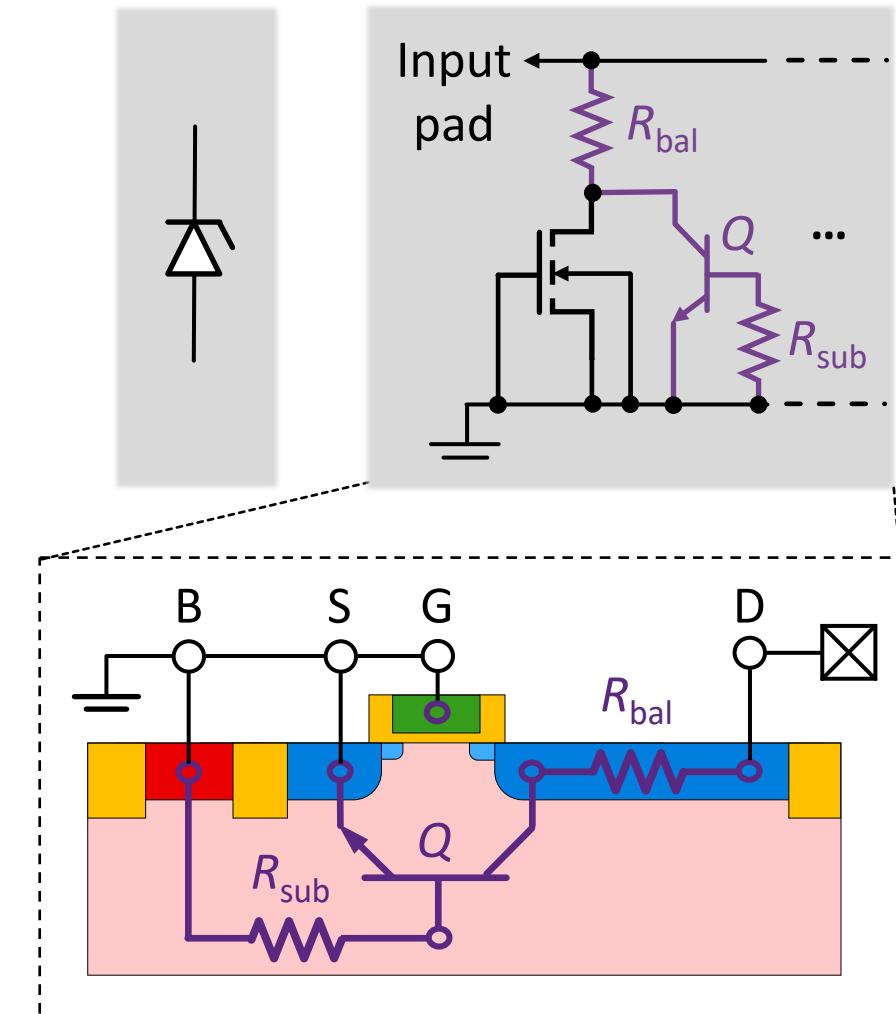
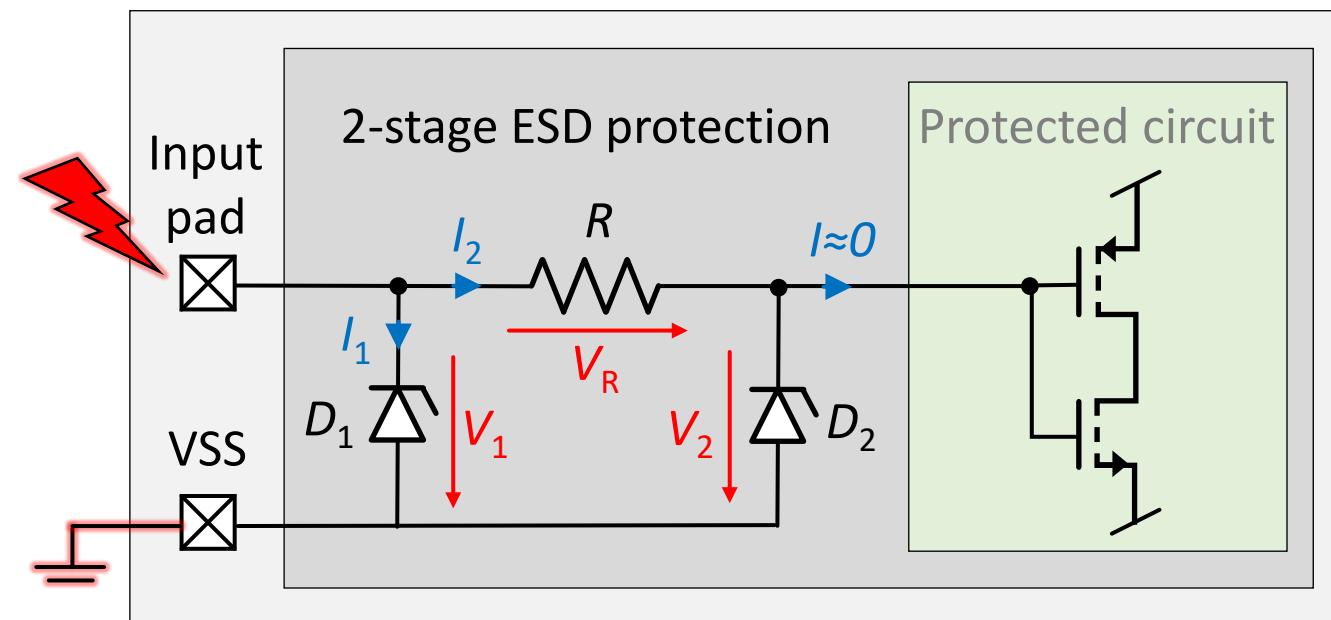


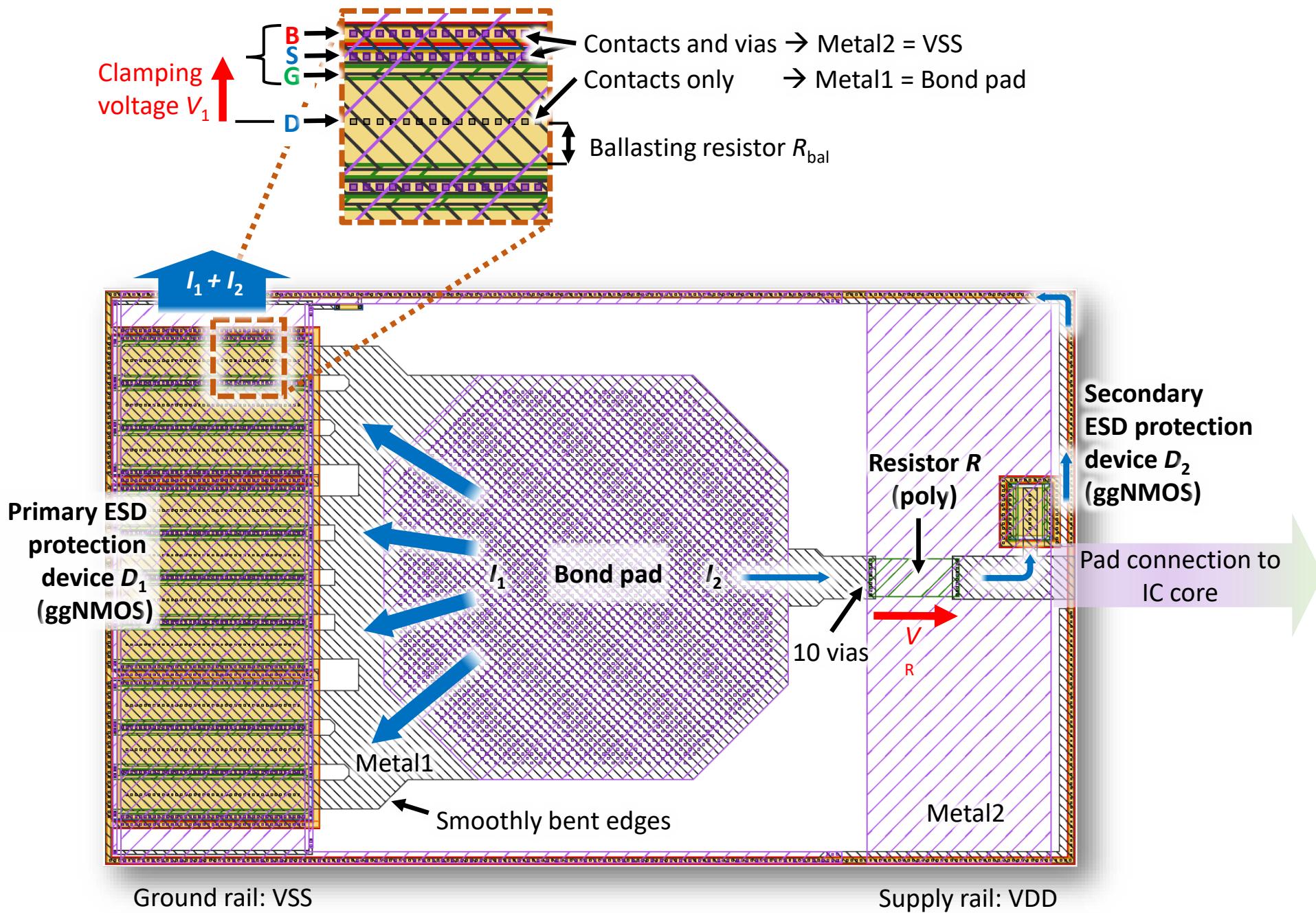


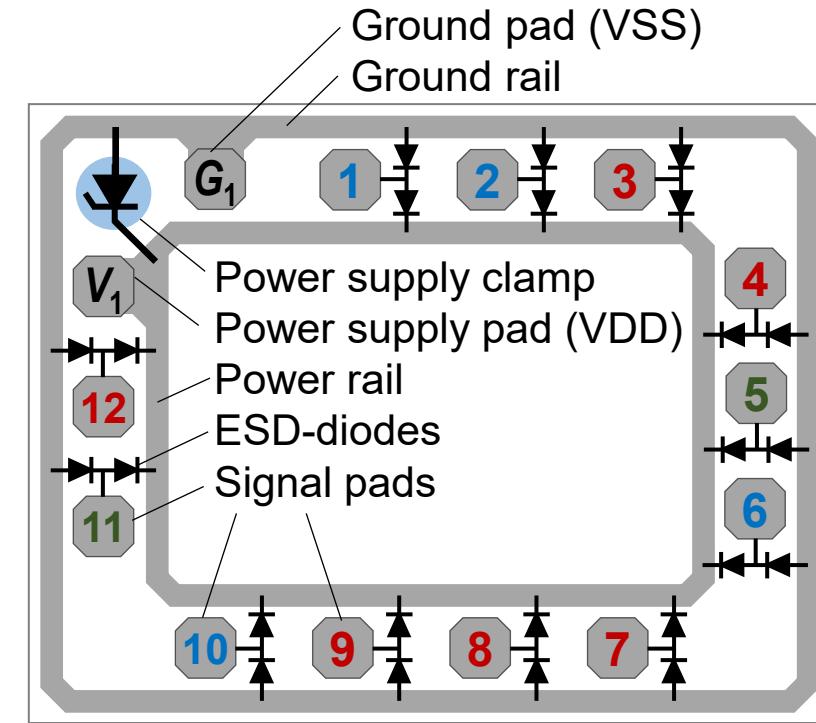
Examples of ESD devices D_1, D_2 :

Zener diode

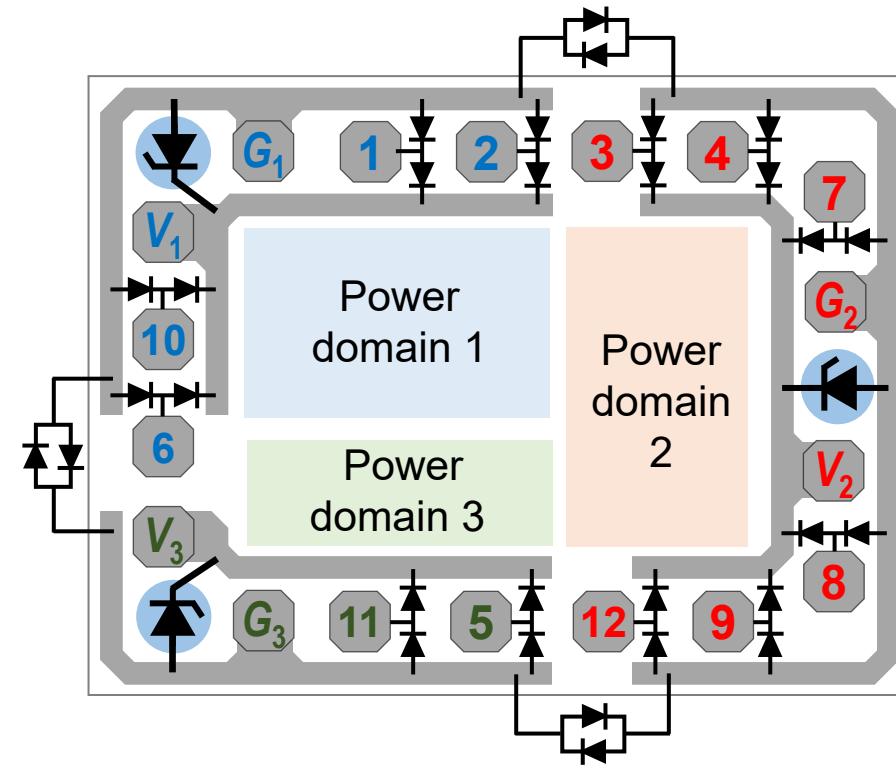
ggNMOS



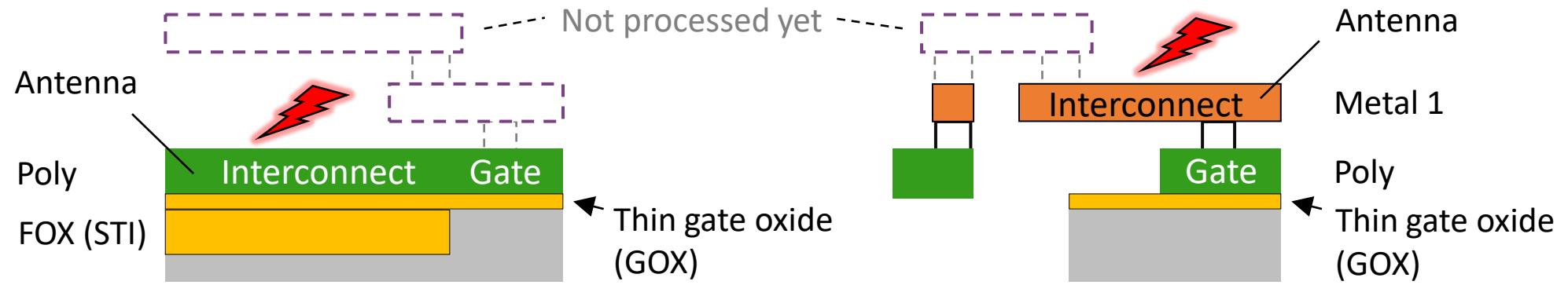


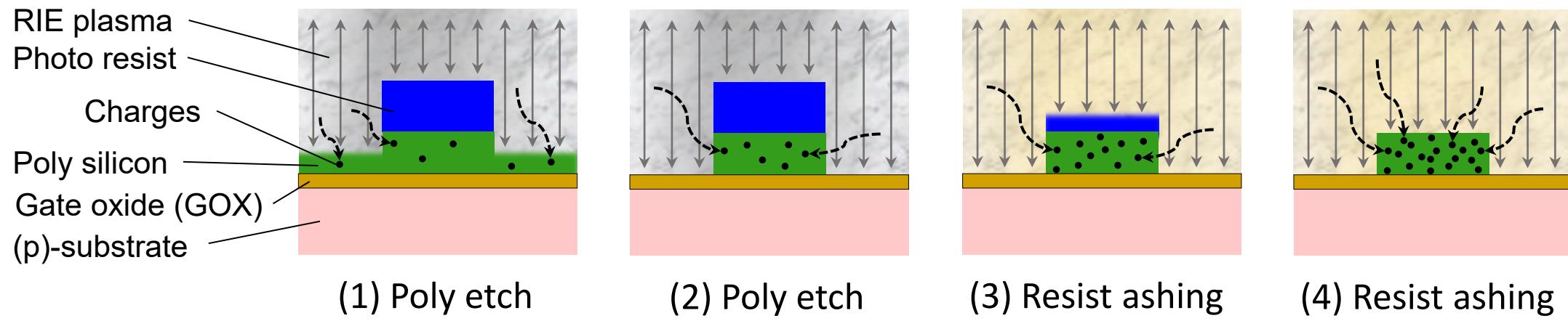


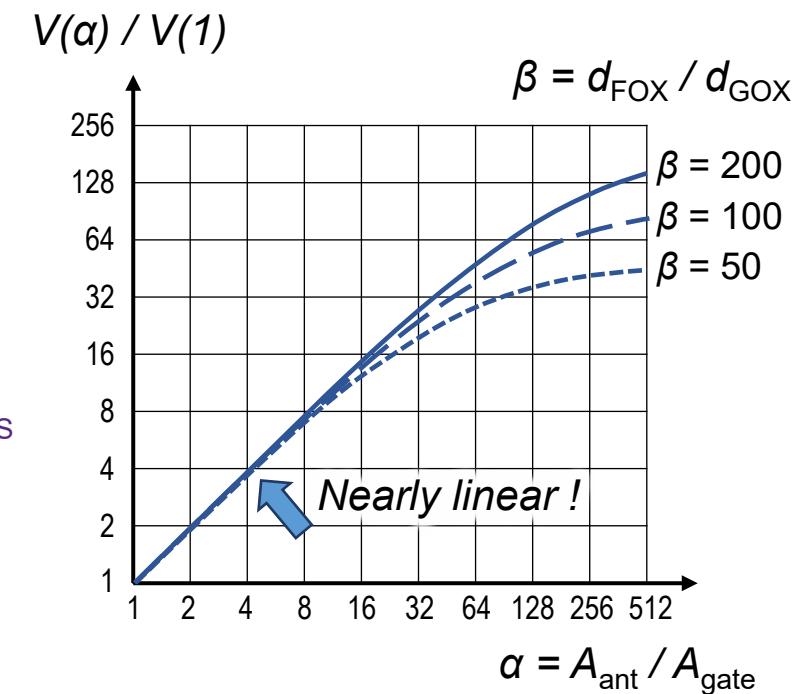
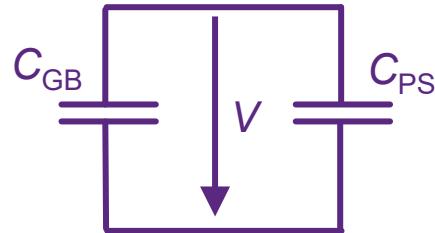
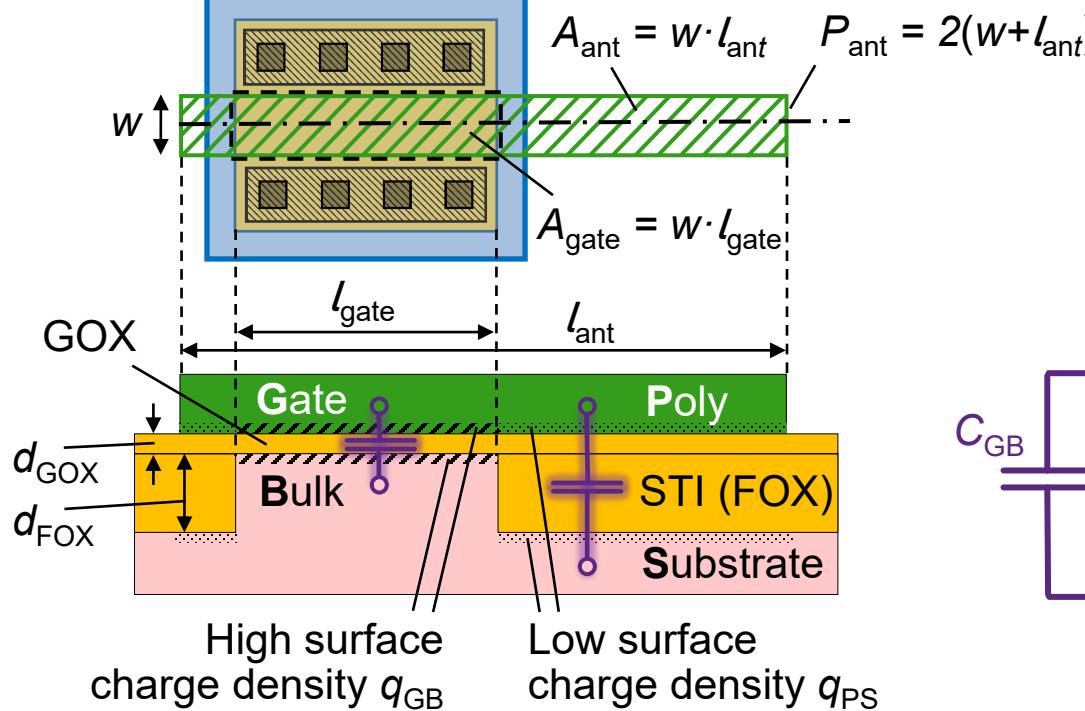
Single power domain

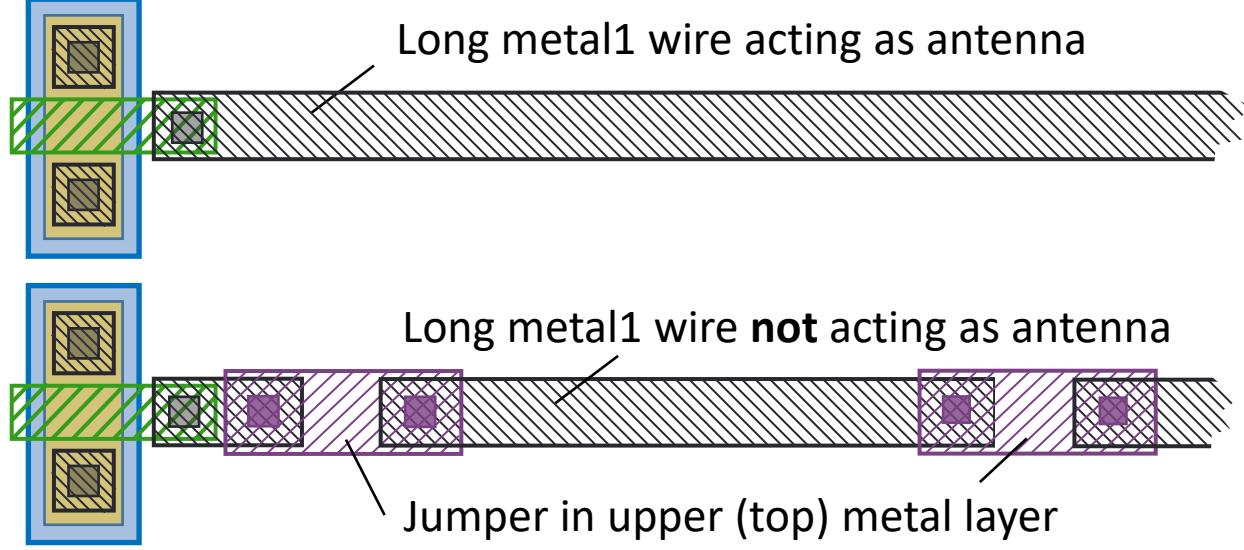
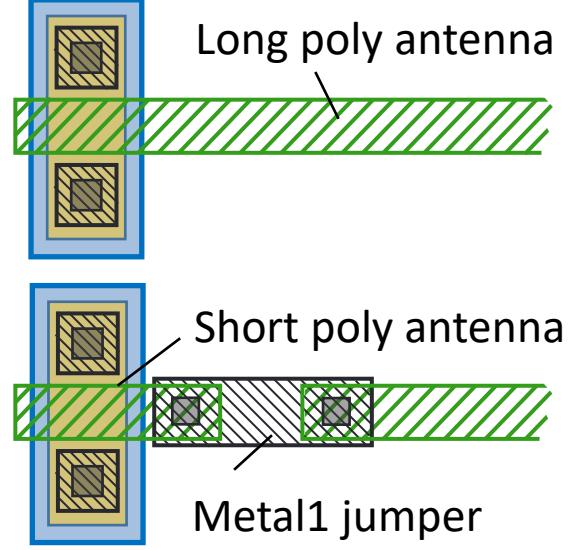


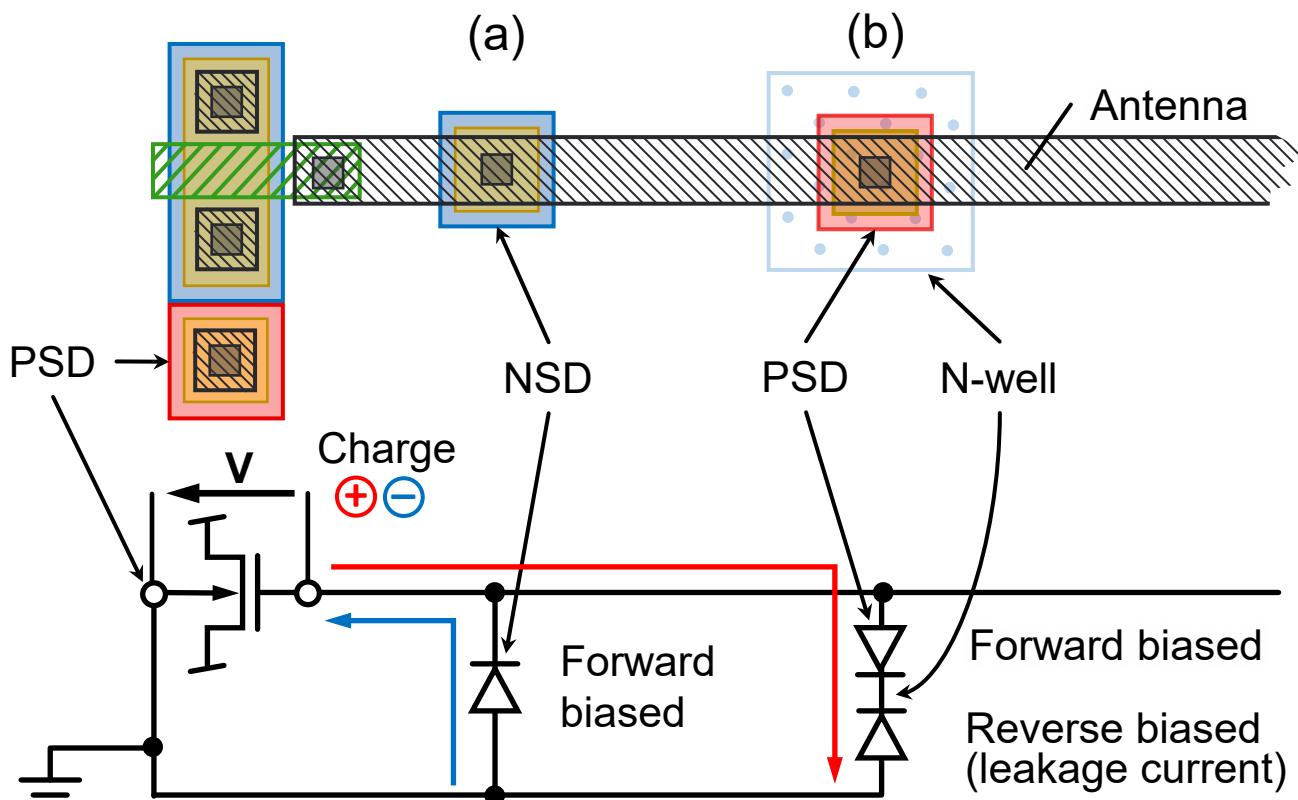
Multiple power domains



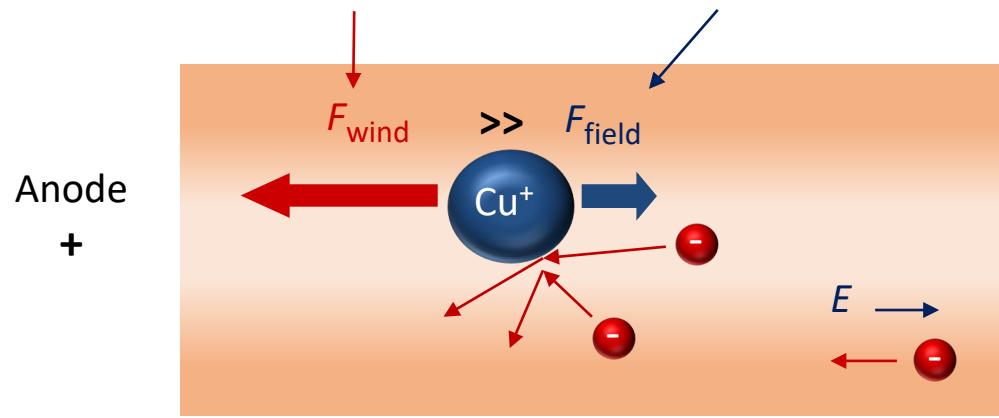




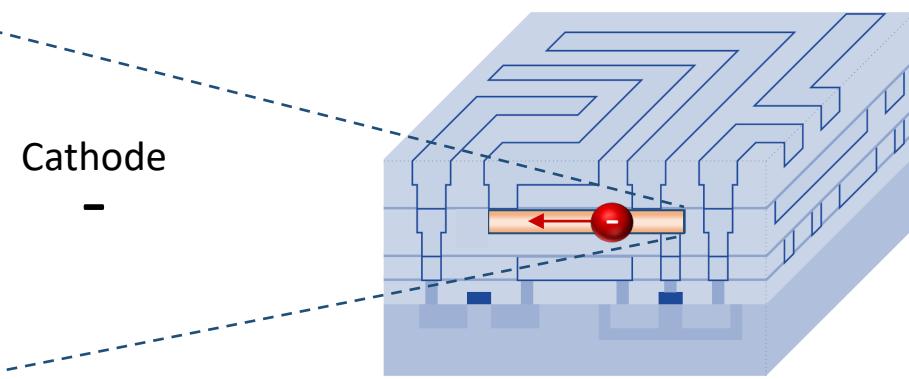




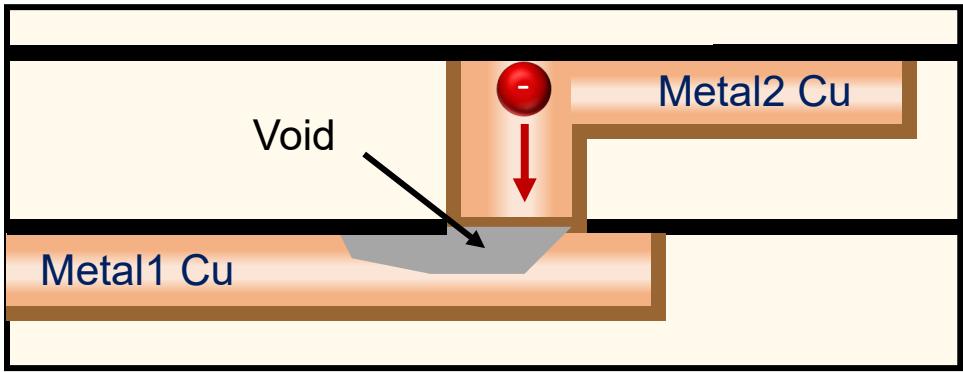
Force on metal ions (Cu^+)
resulting from momentum transfer
from the conduction electrons



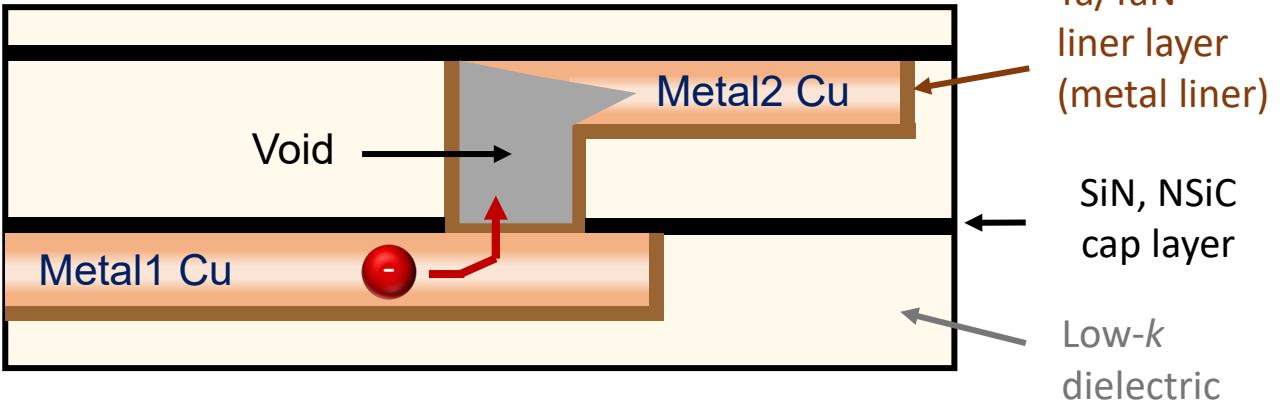
Interaction of
electric field on
metal ions

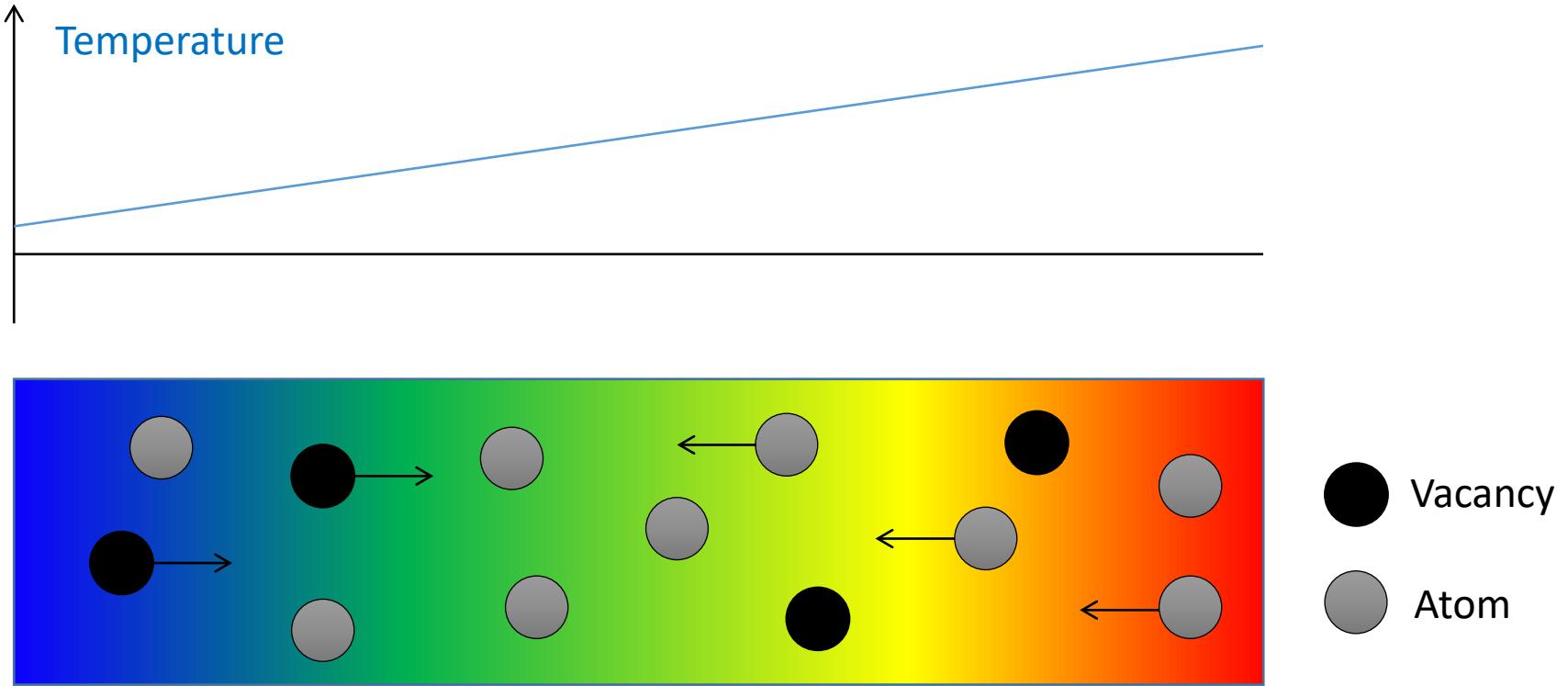


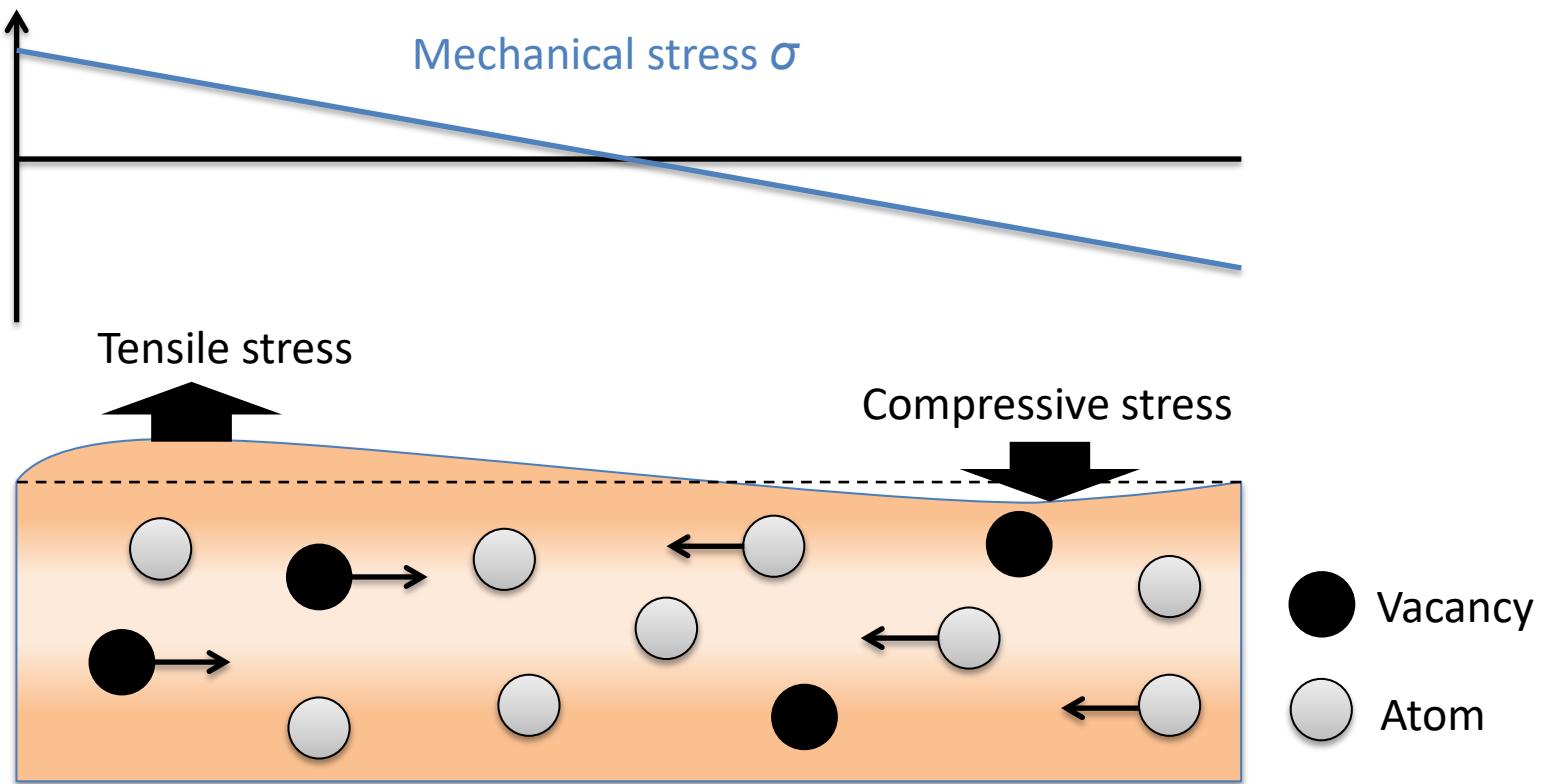
Line Depletion

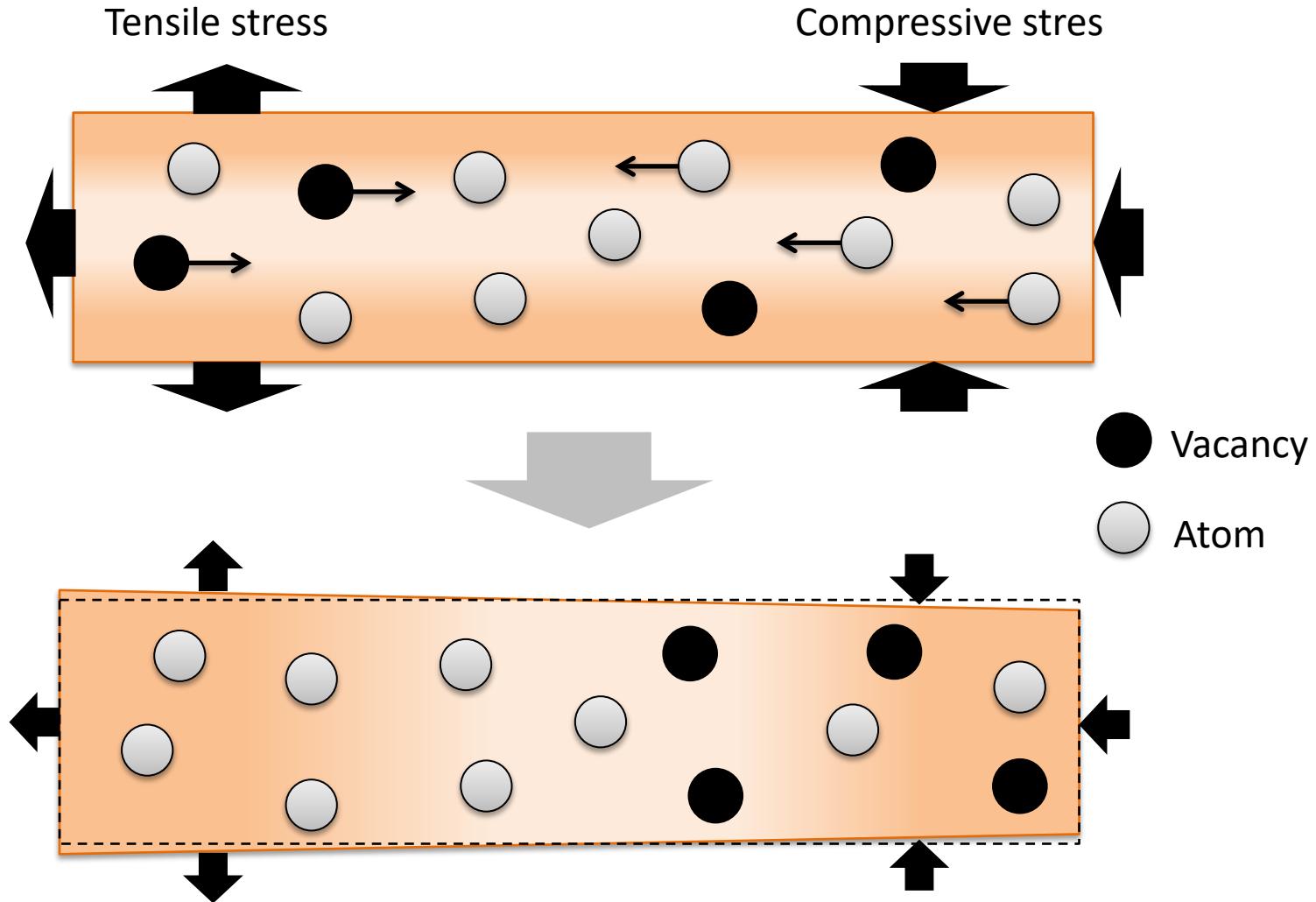


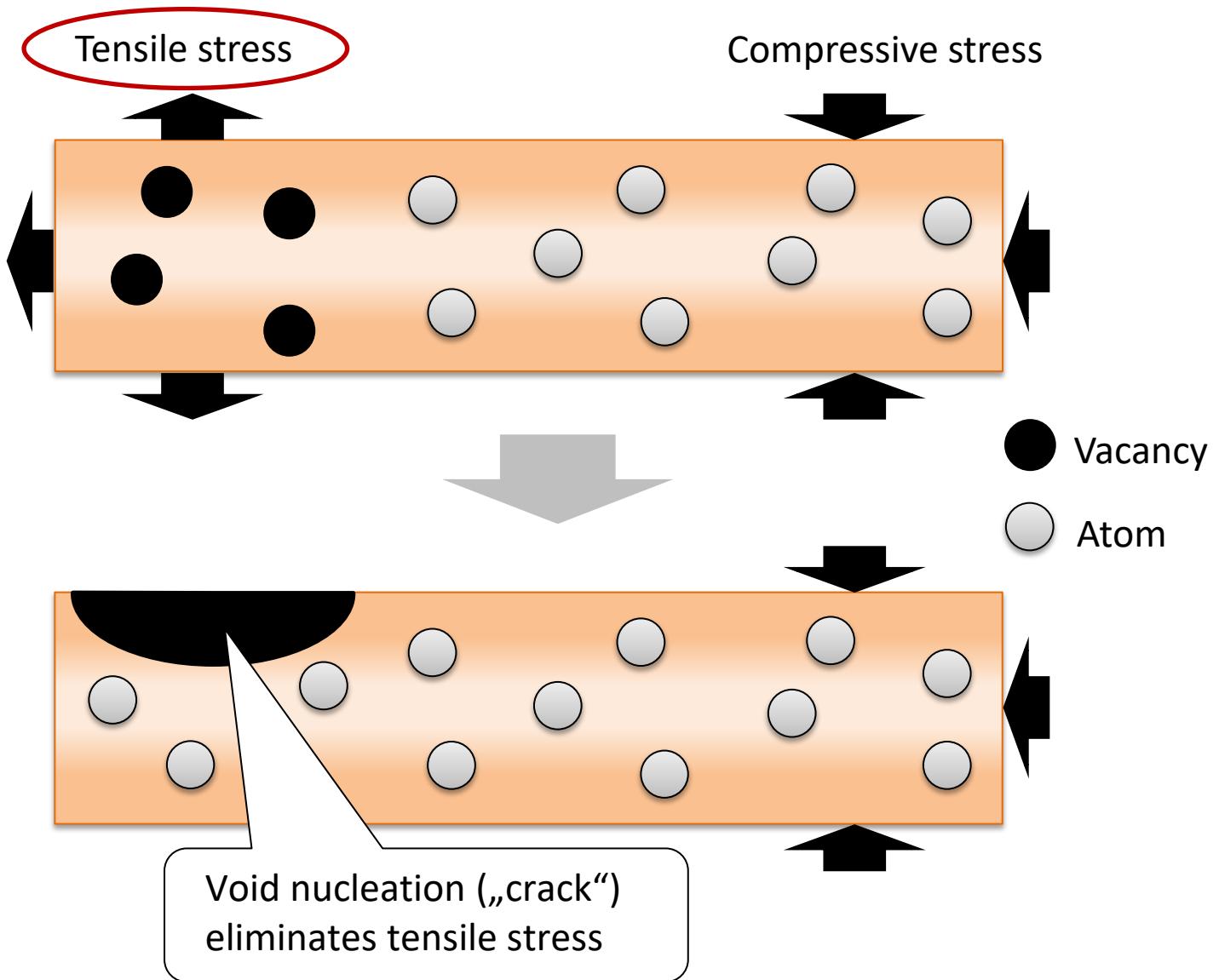
Via Depletion

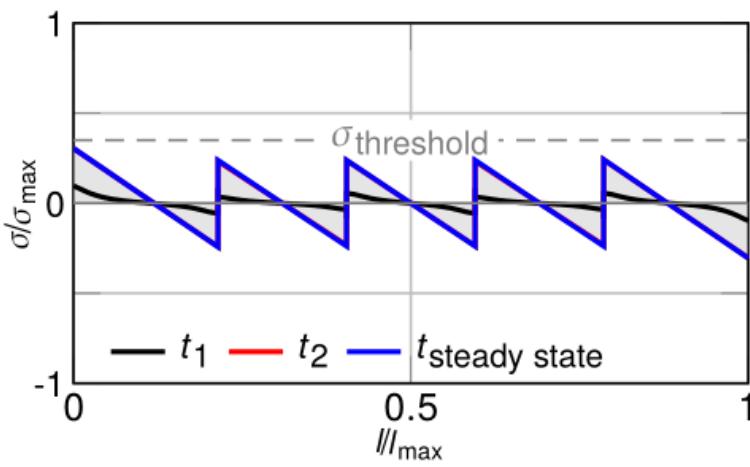
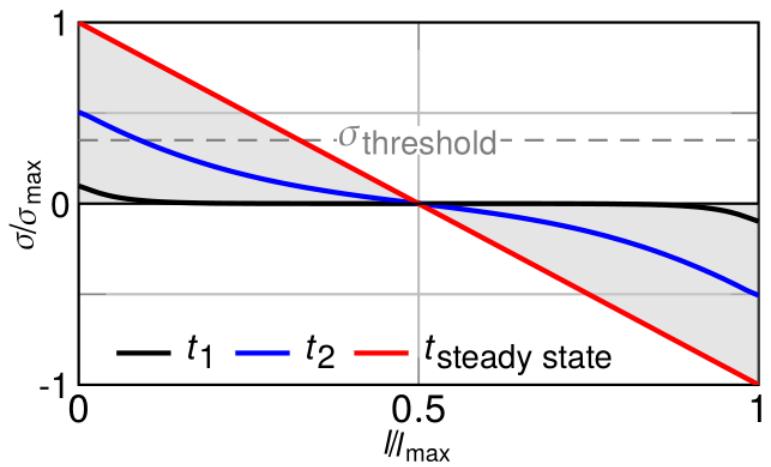
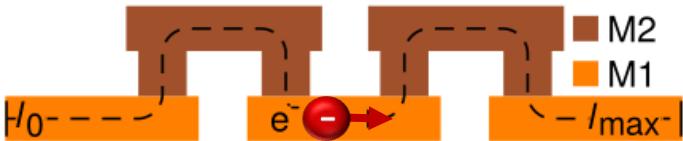


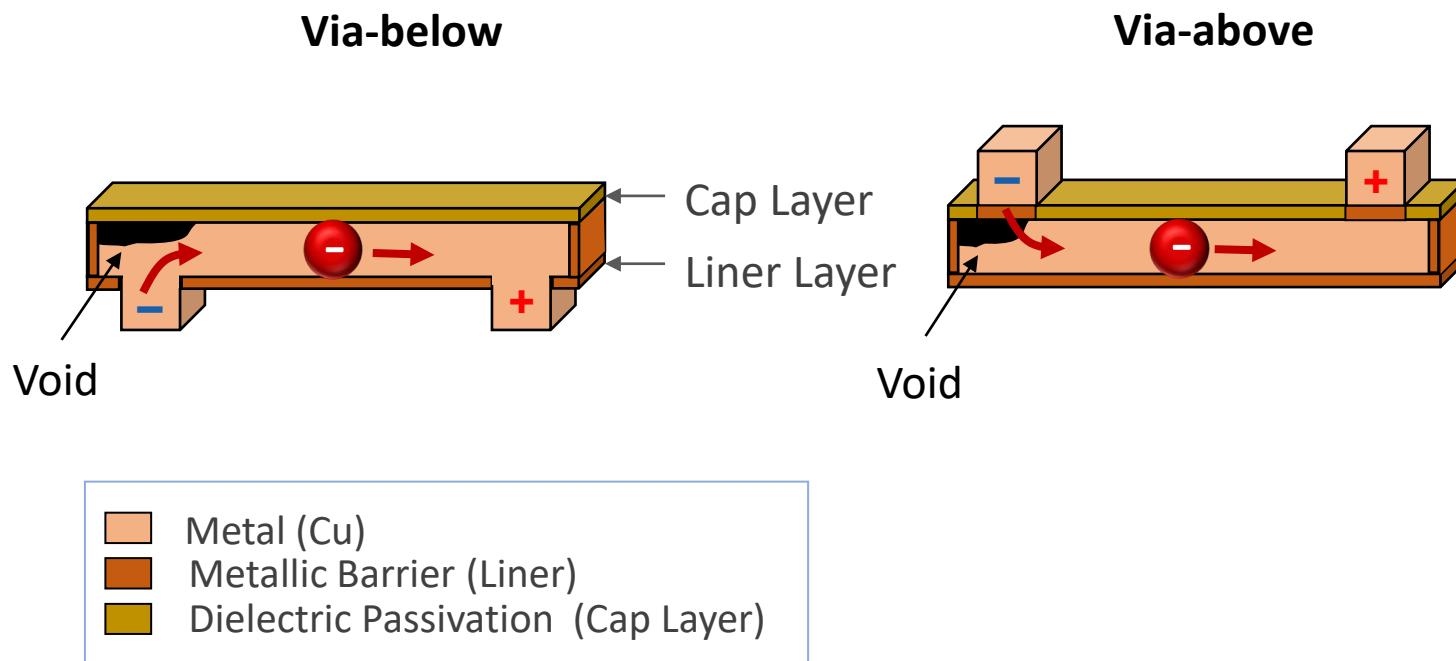


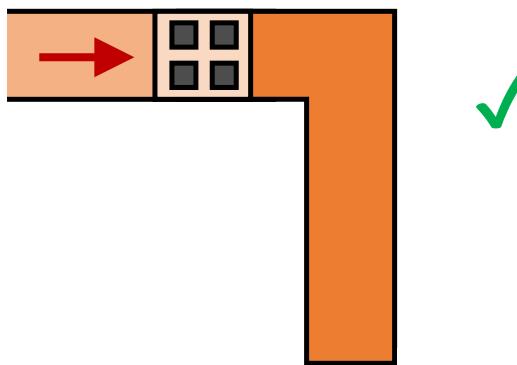
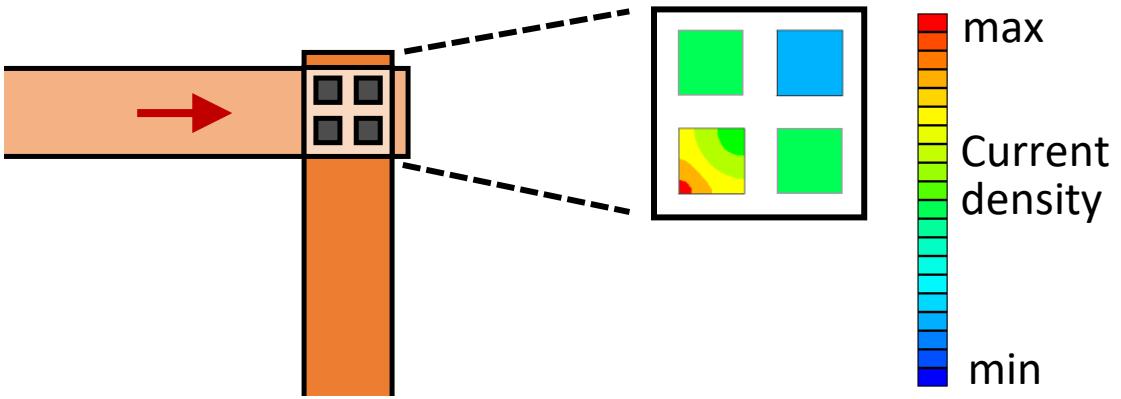
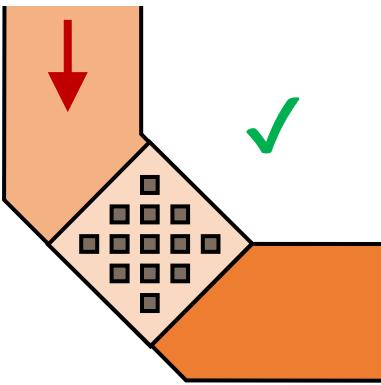
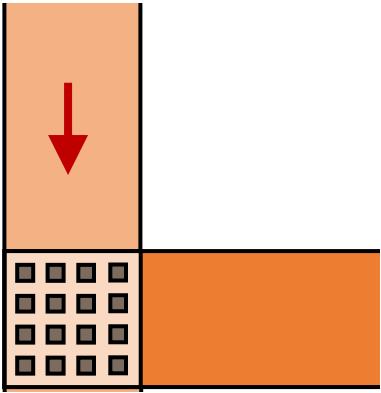


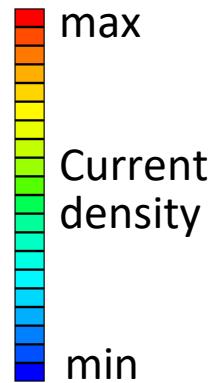
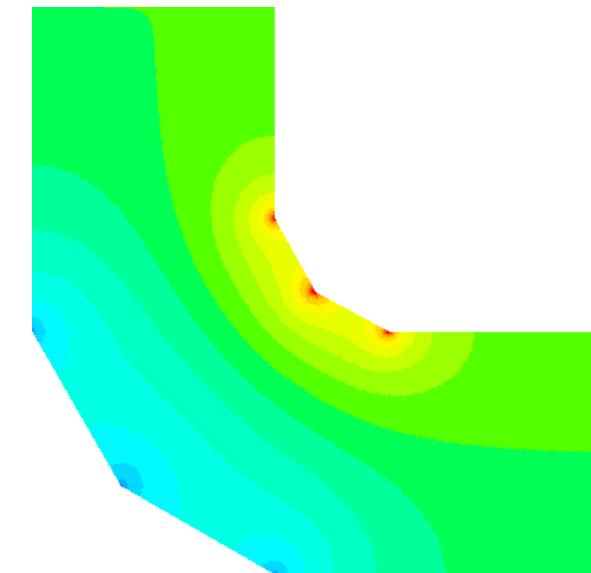
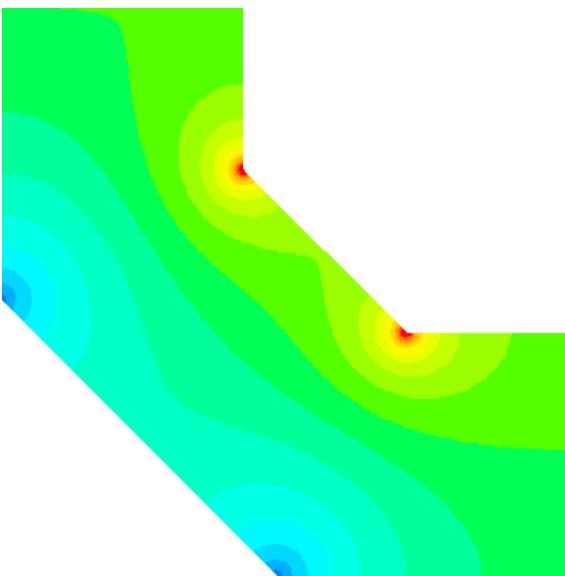
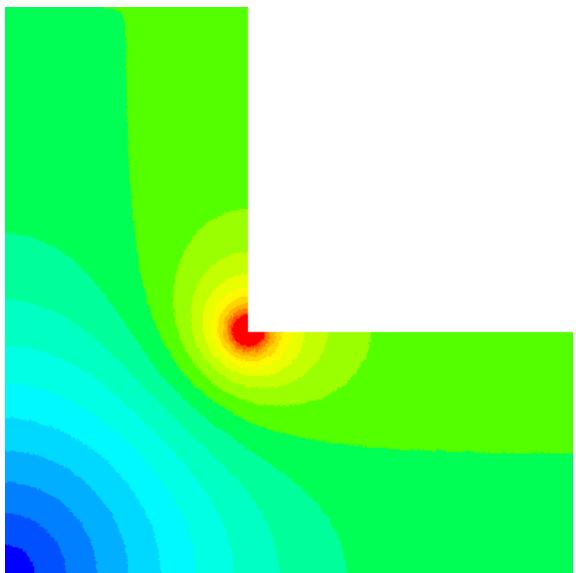


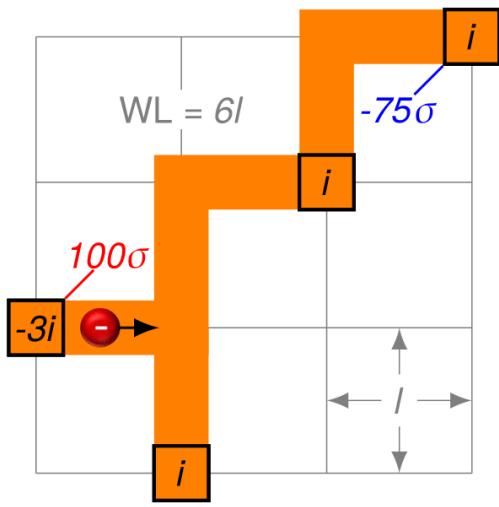




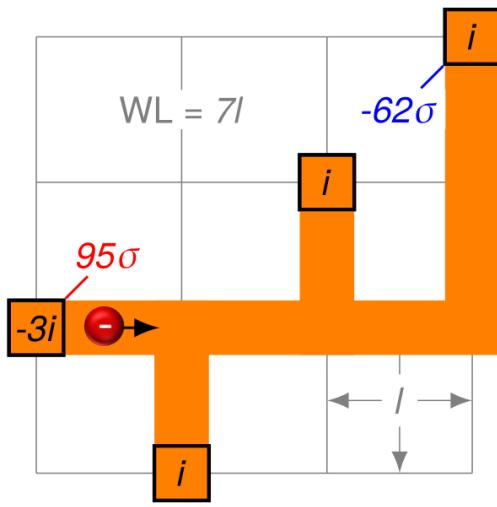




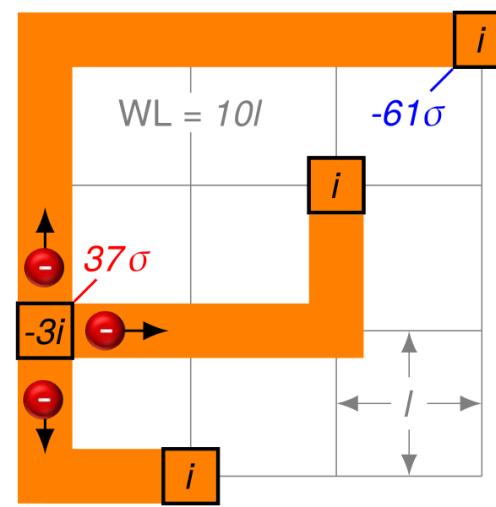




RMST net topology



Trunk net topology



Current-optimized
net topology