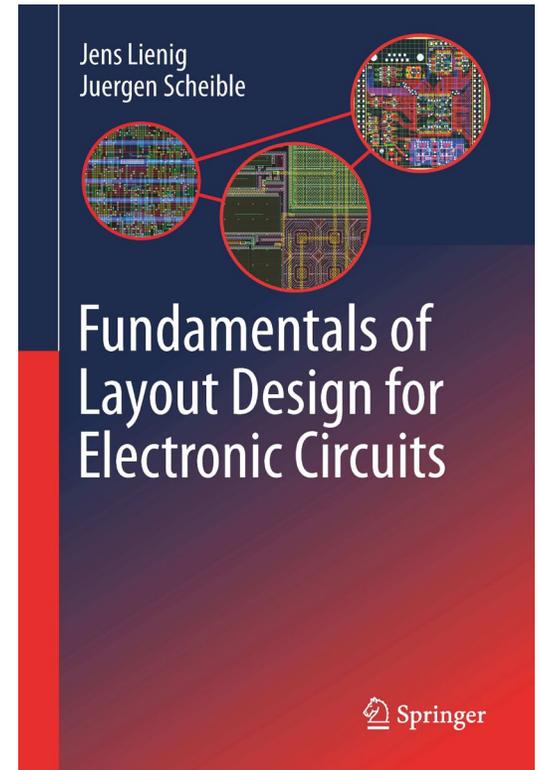


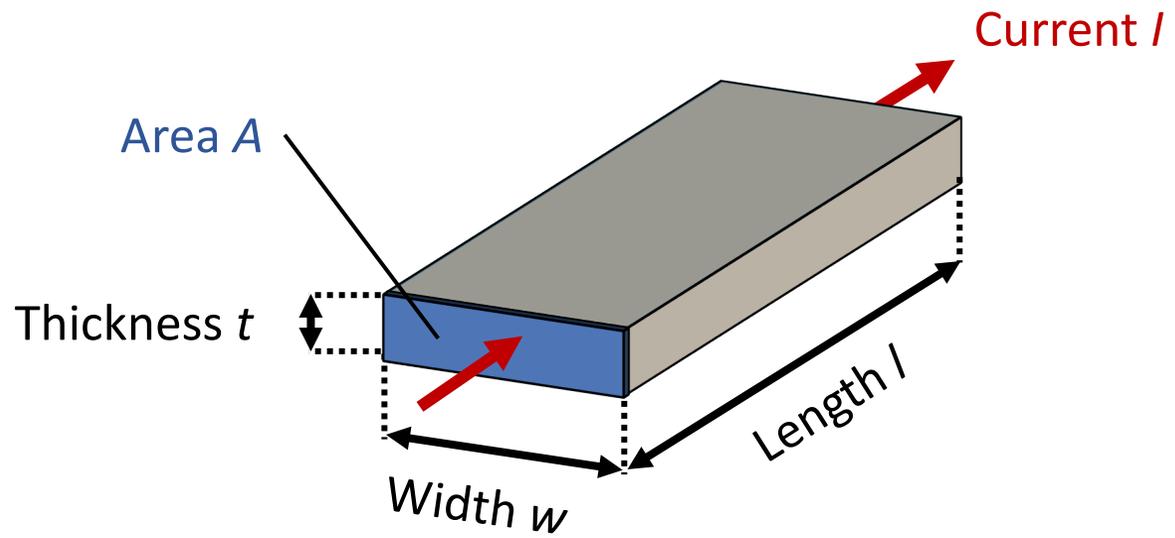
Chapter 6: Special Layout Techniques for Analog IC Design

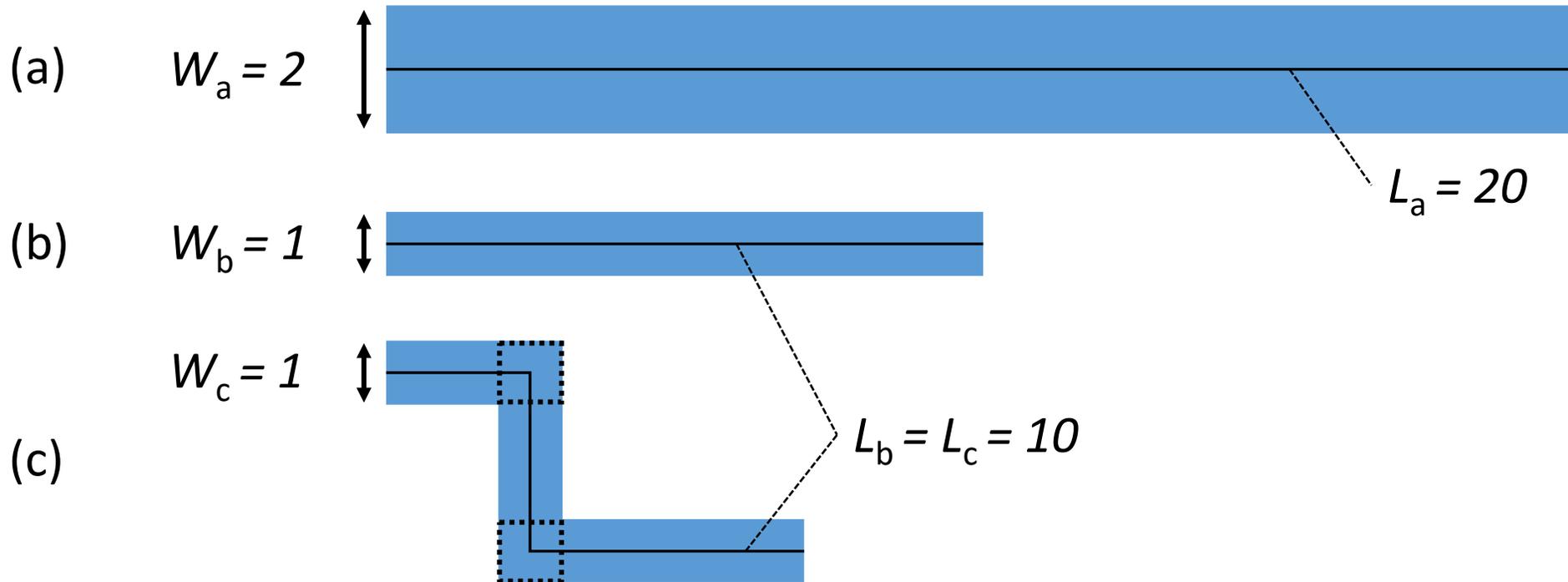
- 6.1 Sheet Resistance: Calculationg with Squares
- 6.2 Wells
- 6.3 Devices: Layout, Connection, and Sizing
- 6.4 Cell Generators: From Parameters to Layout
- 6.5 The Importance of Symmetry
- 6.6 Layout Matching Concepts



Chapter 6: Special Layout Techniques for Analog IC Design

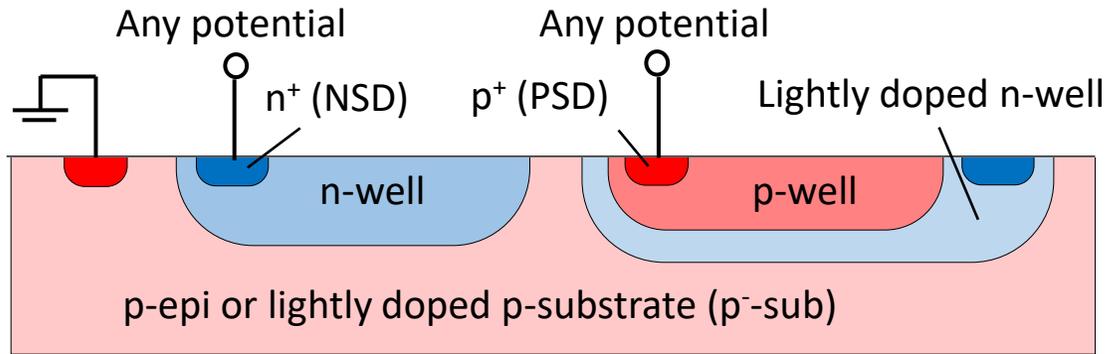
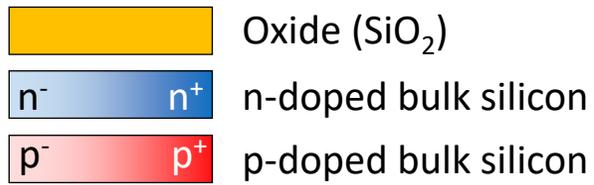
- 6.1 Sheet Resistance: Calculating with Squares**
- 6.2 Wells**
 - 6.2.1 Implementation
 - 6.2.2 Breakdown Voltage
 - 6.2.3 Voltage-Dependent Spacing Rules
- 6.3 Devices: Layout, Connection, and Sizing**
 - 6.3.1 Field-Effect Transistors (MOS-FETs)
 - 6.3.2 Resistors
 - 6.3.3 Capacitors
 - 6.3.4 Bipolar Transistors
- 6.4 Cell Generators: From Parameters to Layout**
 - 6.4.1 Overview
 - 6.4.2 Example
- 6.5 The Importance of Symmetry**
 - 6.5.1 Absolute and Relative Accuracy: The Big Difference
 - 6.5.2 Obtaining Symmetry by Matching Devices
- 6.6 Layout Matching Concepts**
 - 6.6.1 Matching Concepts for Internal Device Fringe Effects
 - 6.6.2 Matching Concepts for Unknown Gradients
 - 6.6.3 Matching Concepts for External Device Fringe Effects
 - 6.6.4 Matching Concepts for Known Gradients
 - 6.6.5 Matching Concepts for Orientation-Dependent Effects
 - 6.6.6 Summary of Matching Concepts





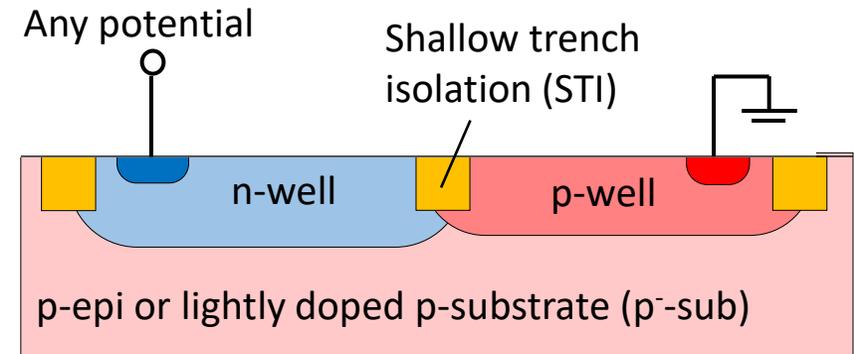
$$R_a = R_b = 10R_{\square}$$

$$R_c = 10R_{\square} - 2R_{\square} / 2 \approx 9R_{\square}$$

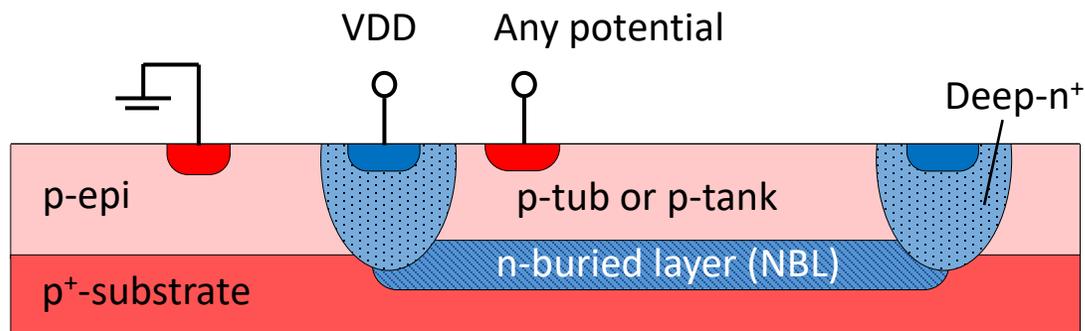


(a)

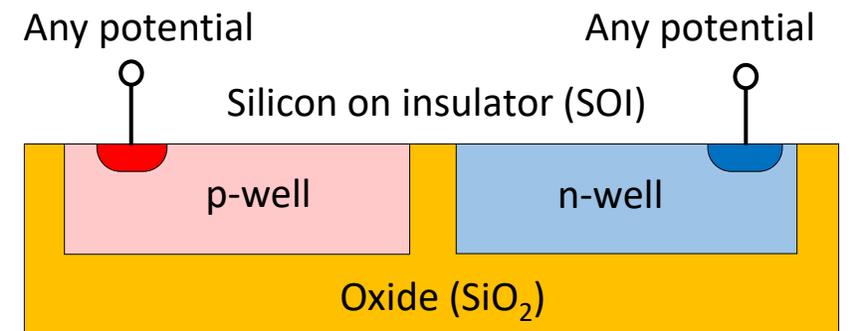
(b)



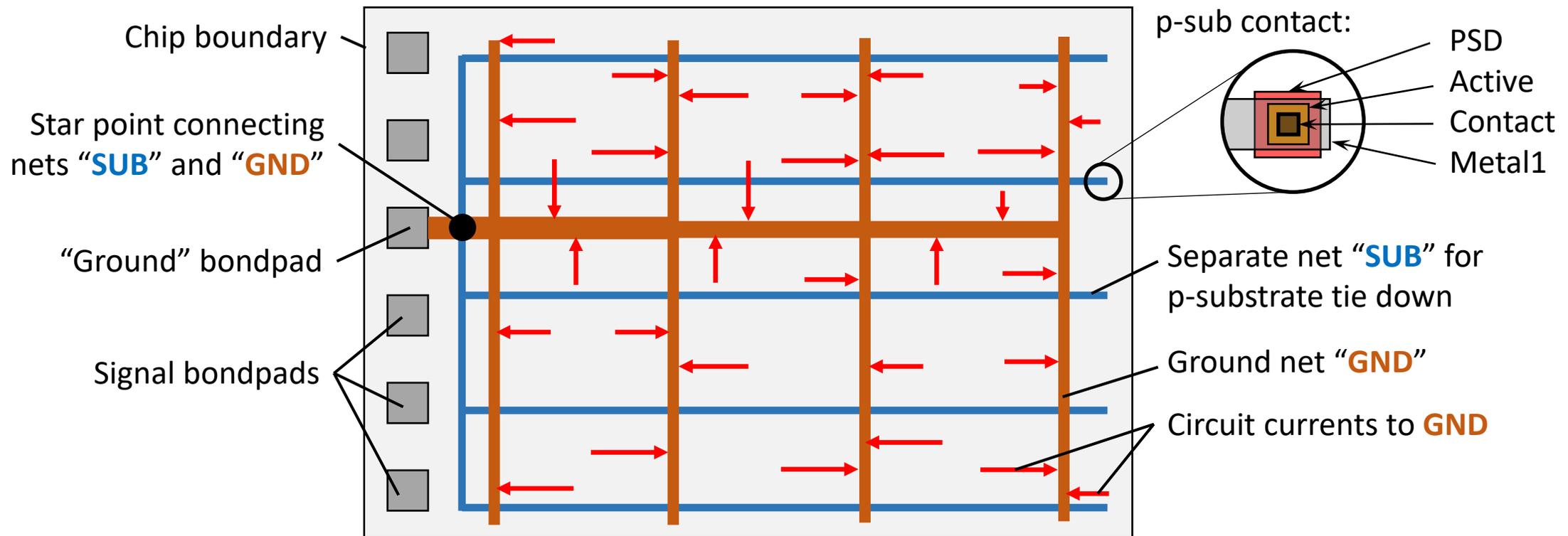
(c)



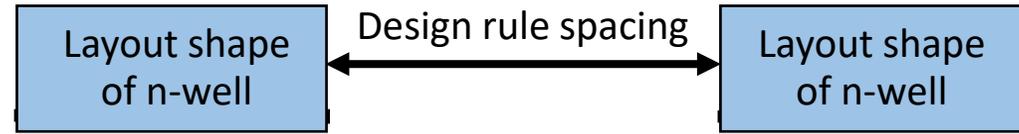
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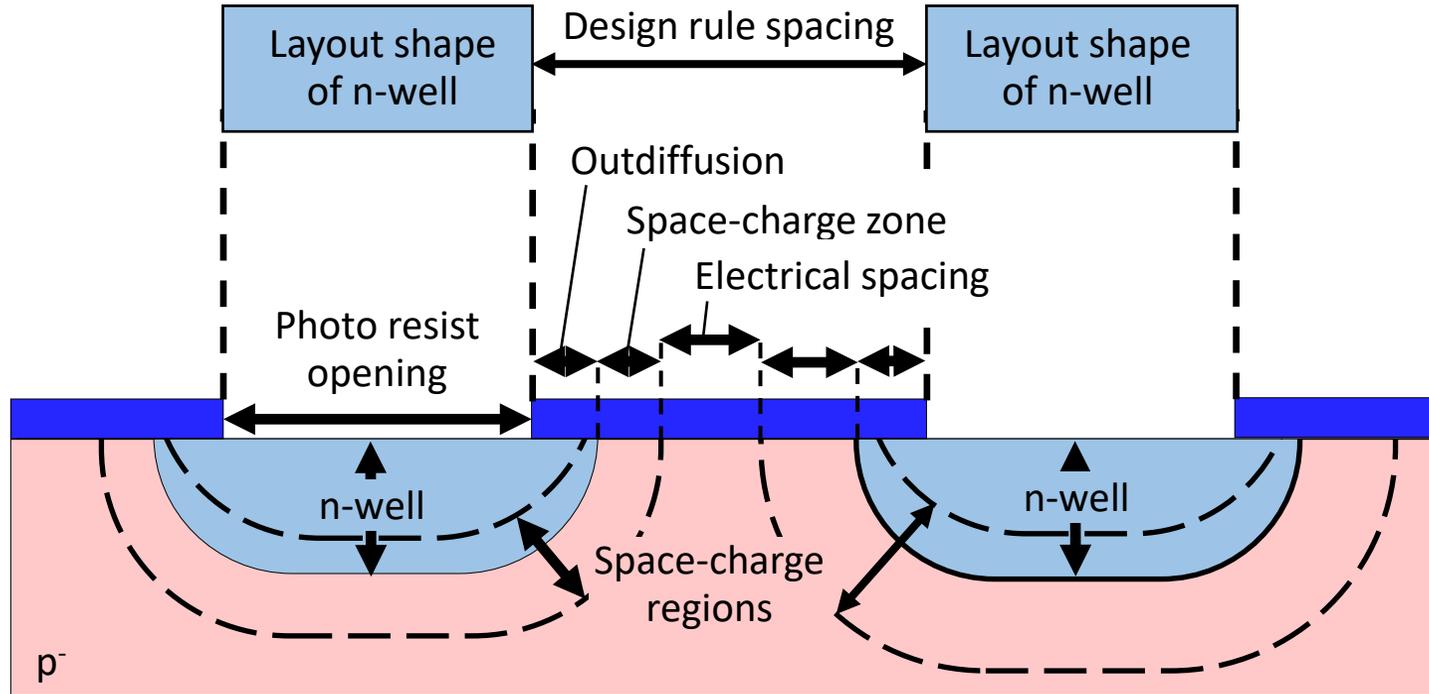
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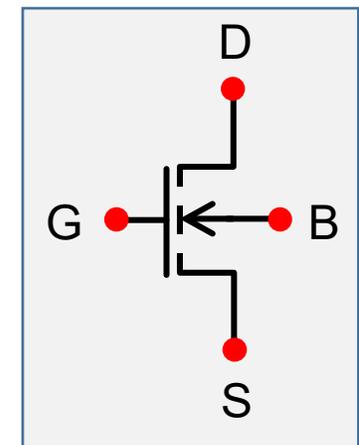
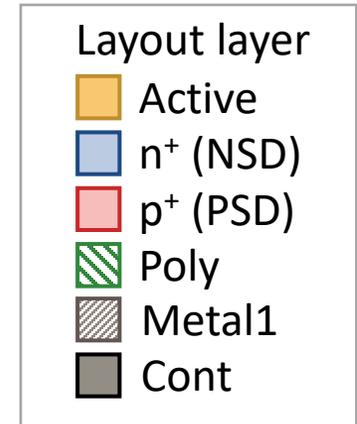
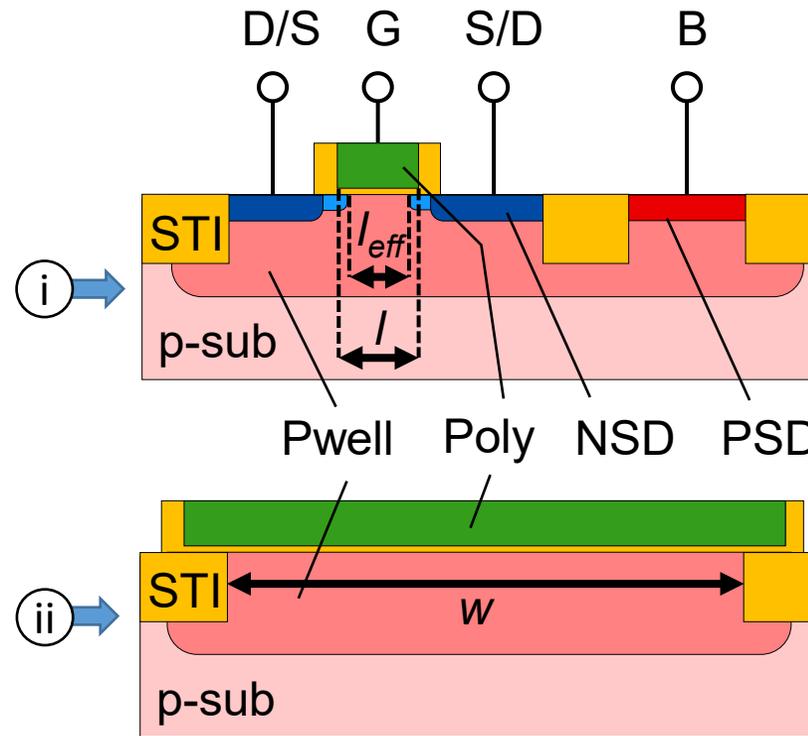
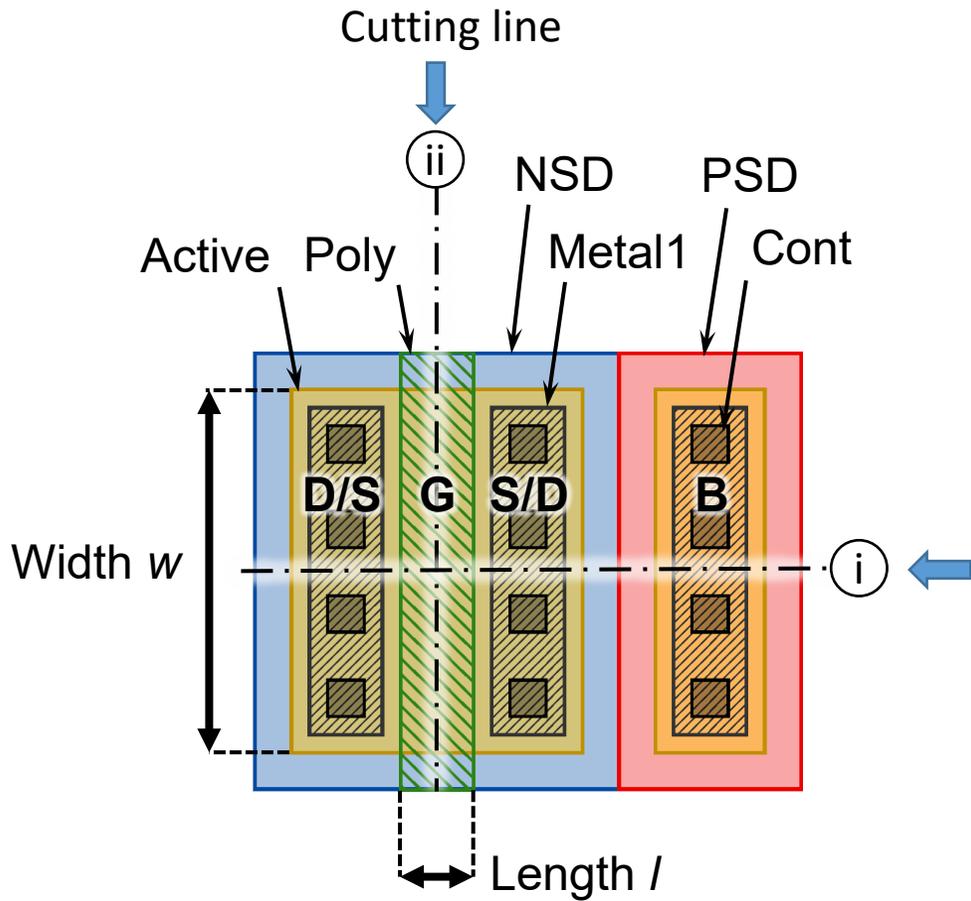


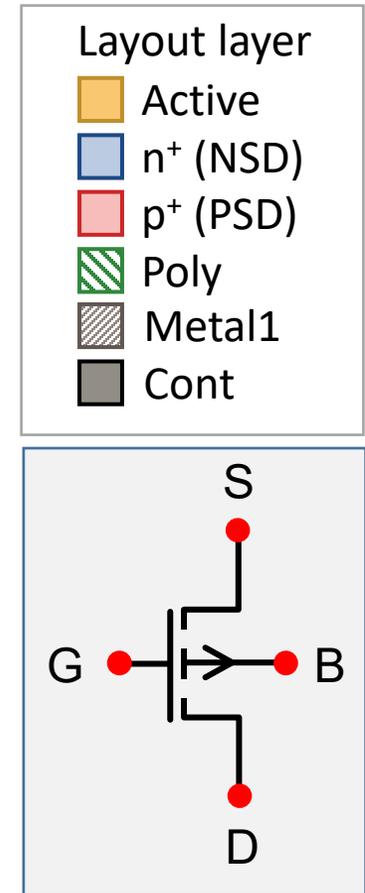
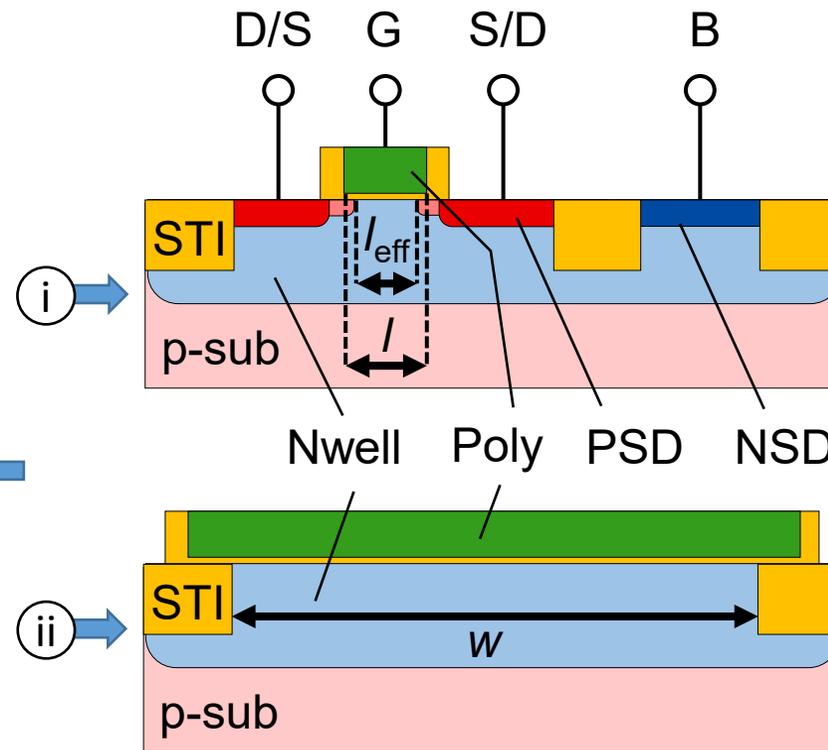
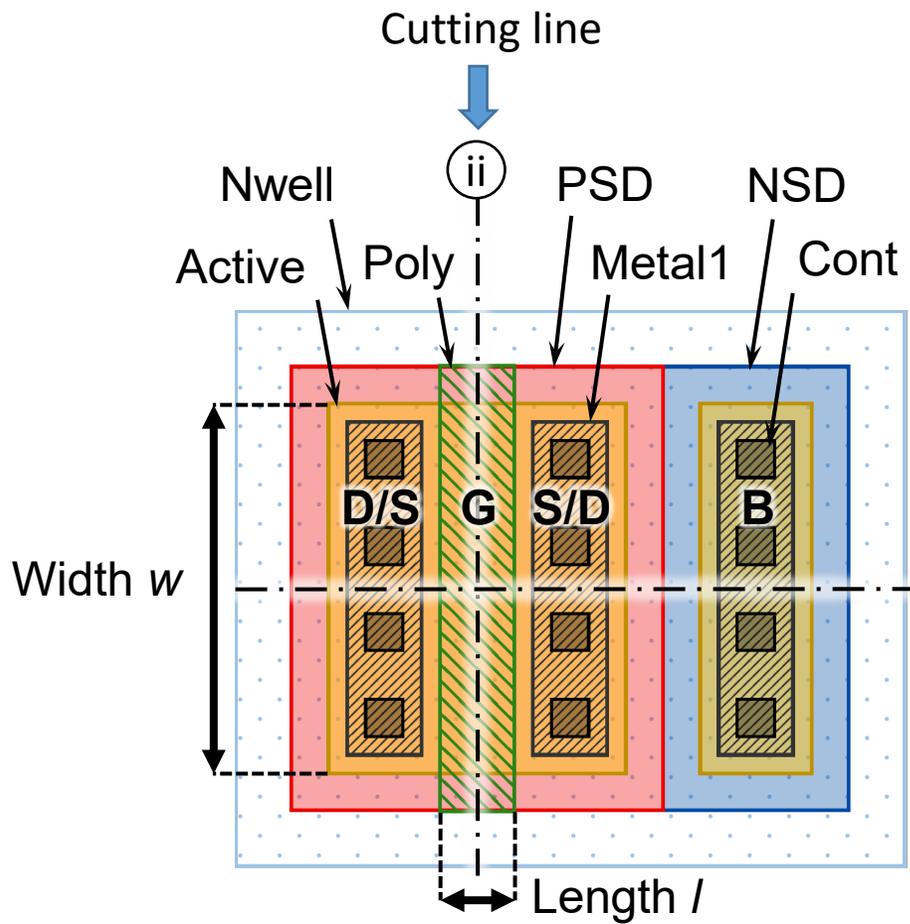
Layout/top view:

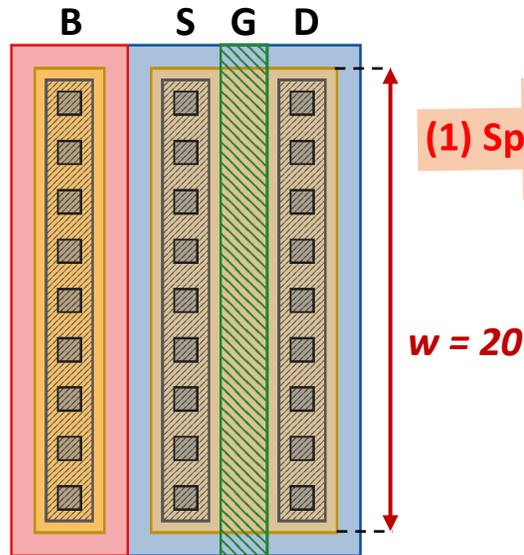
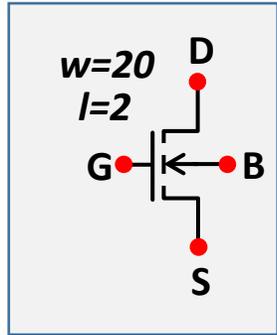


Sectional view:



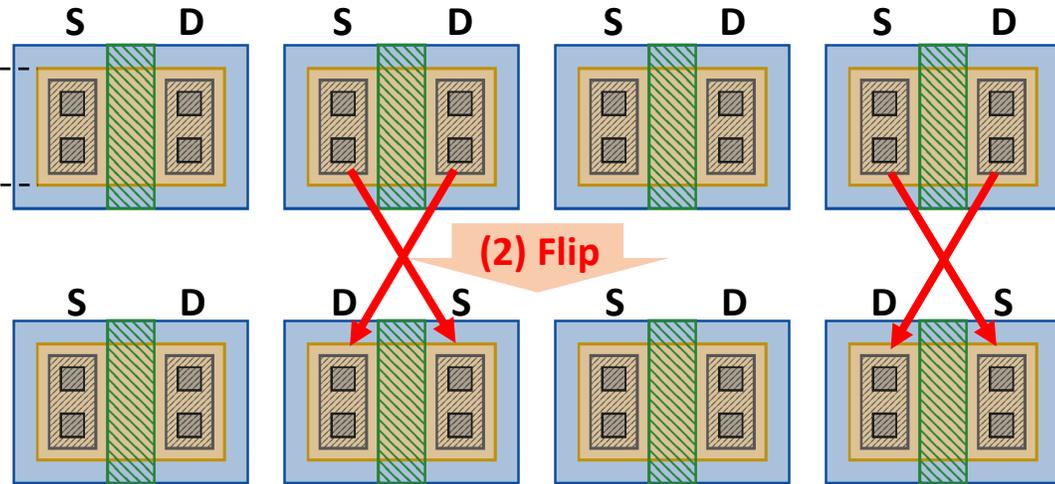






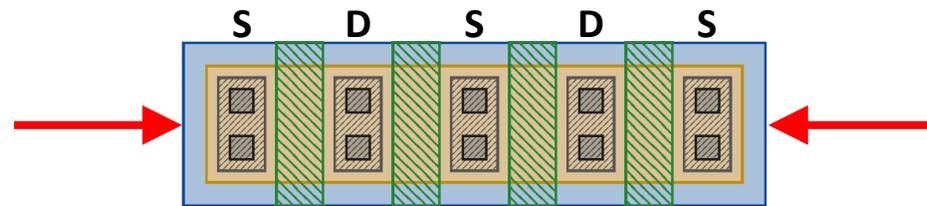
(1) Split

$w = 5$

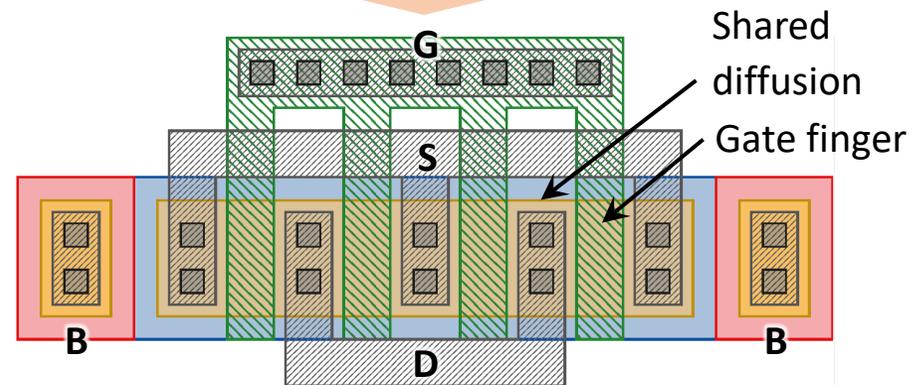
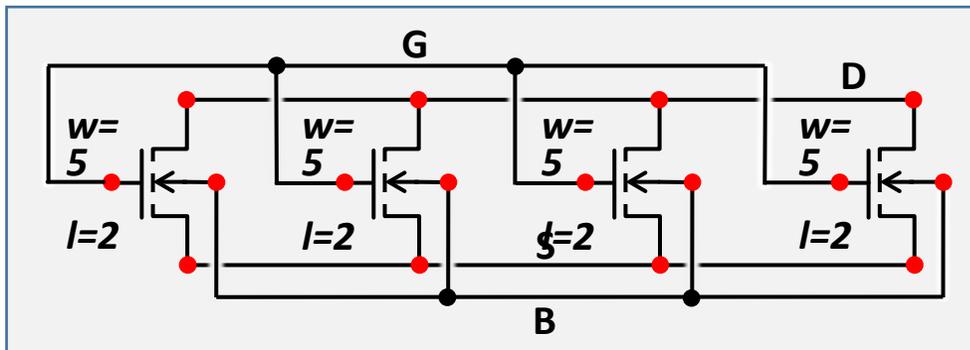


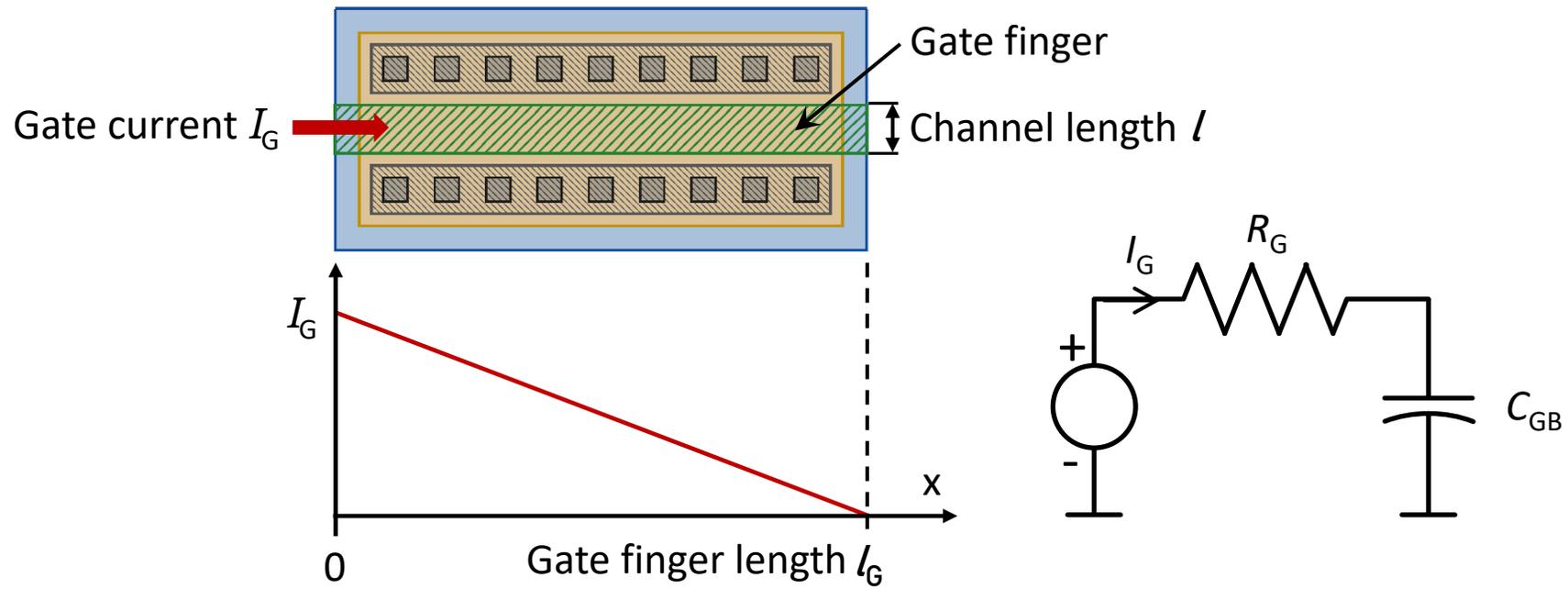
(2) Flip

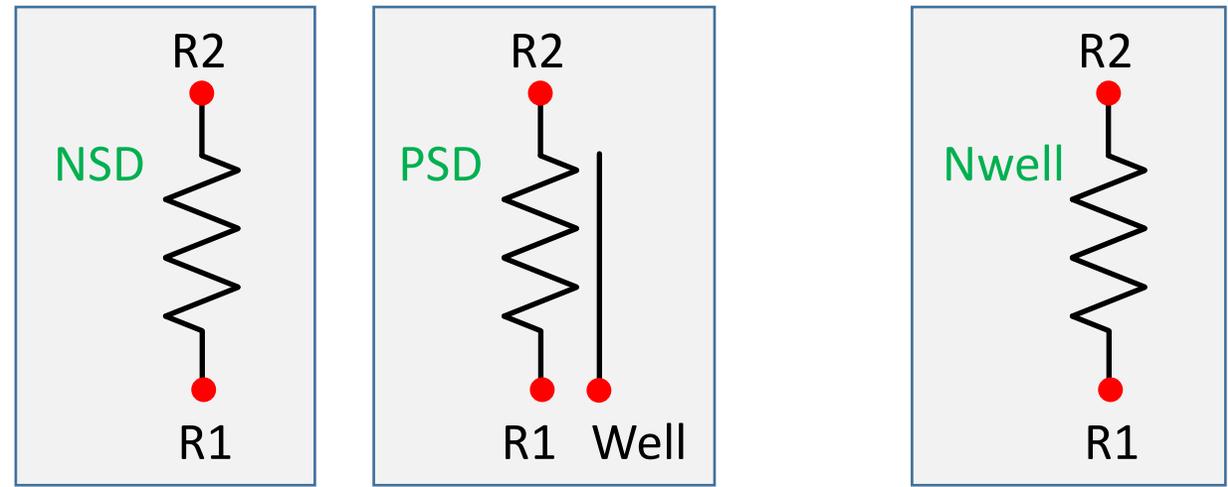
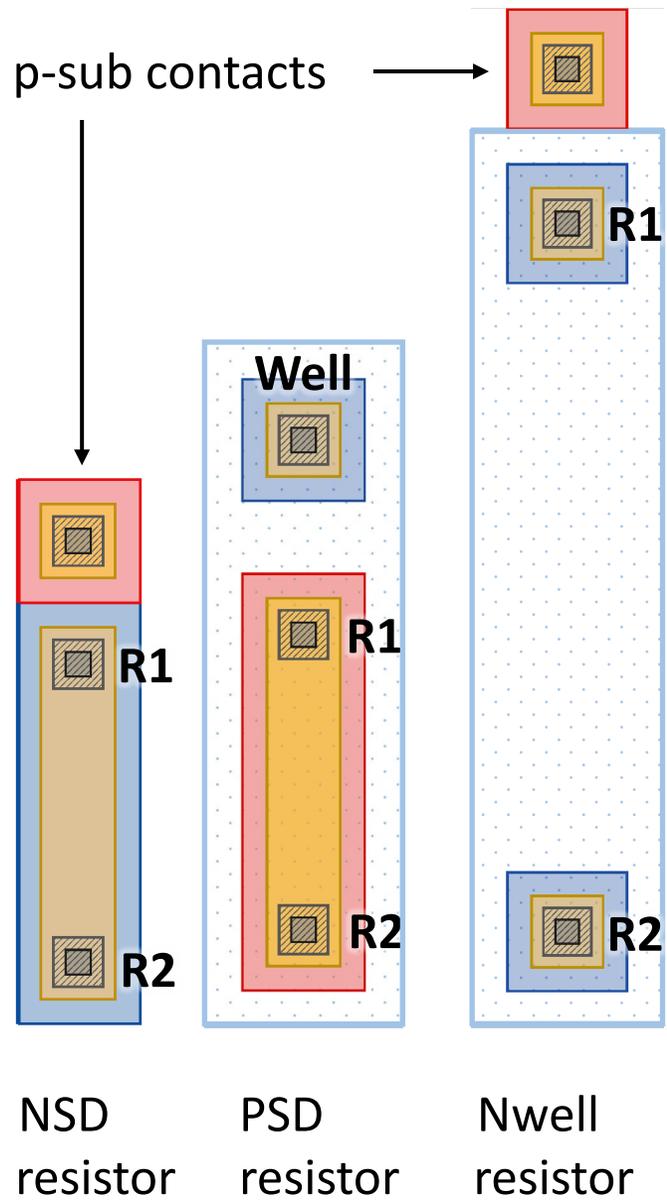
(3) Pack



(4) Route



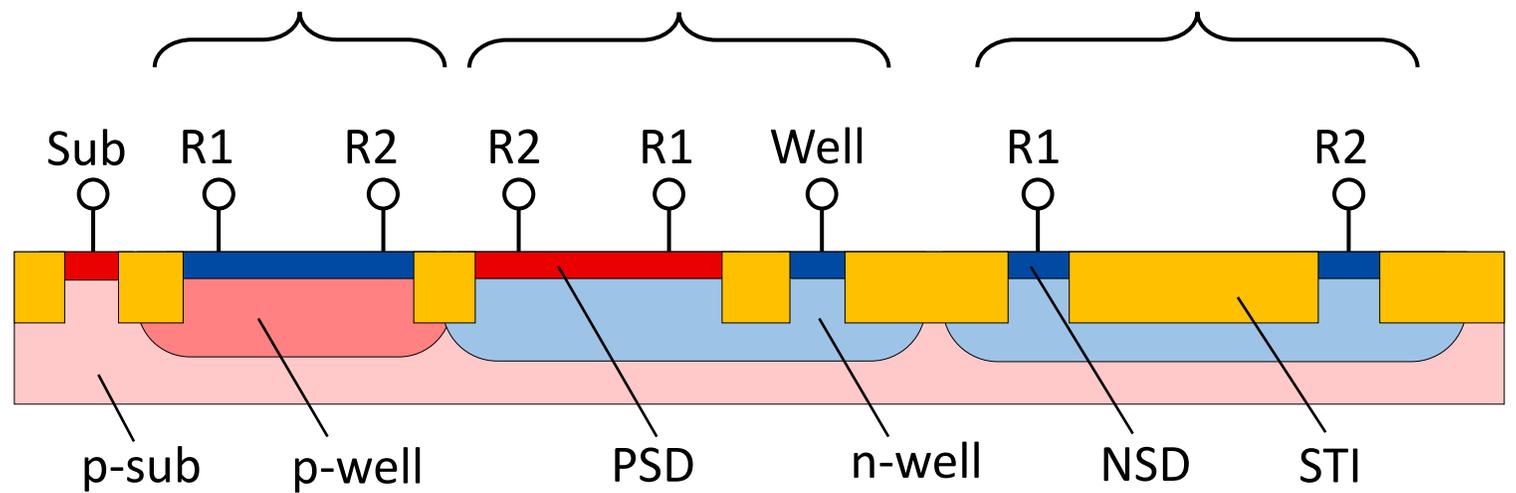


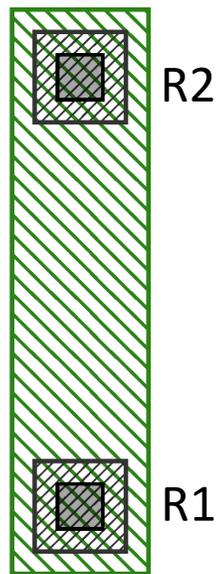


NSD resistor

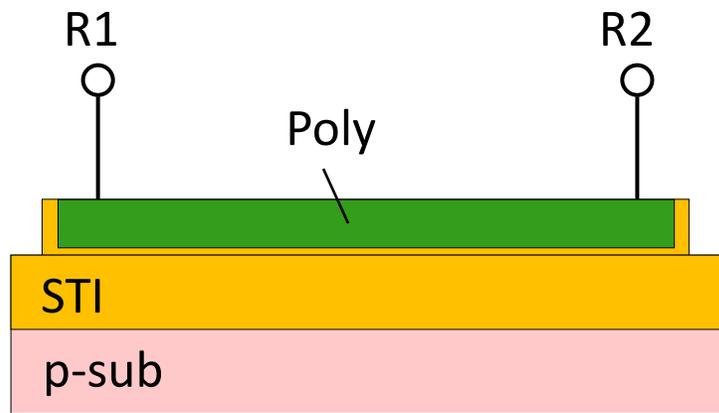
PSD resistor

Nwell resistor

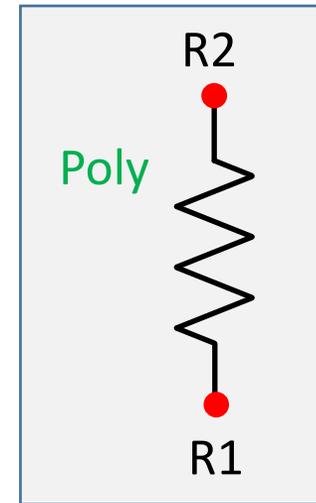




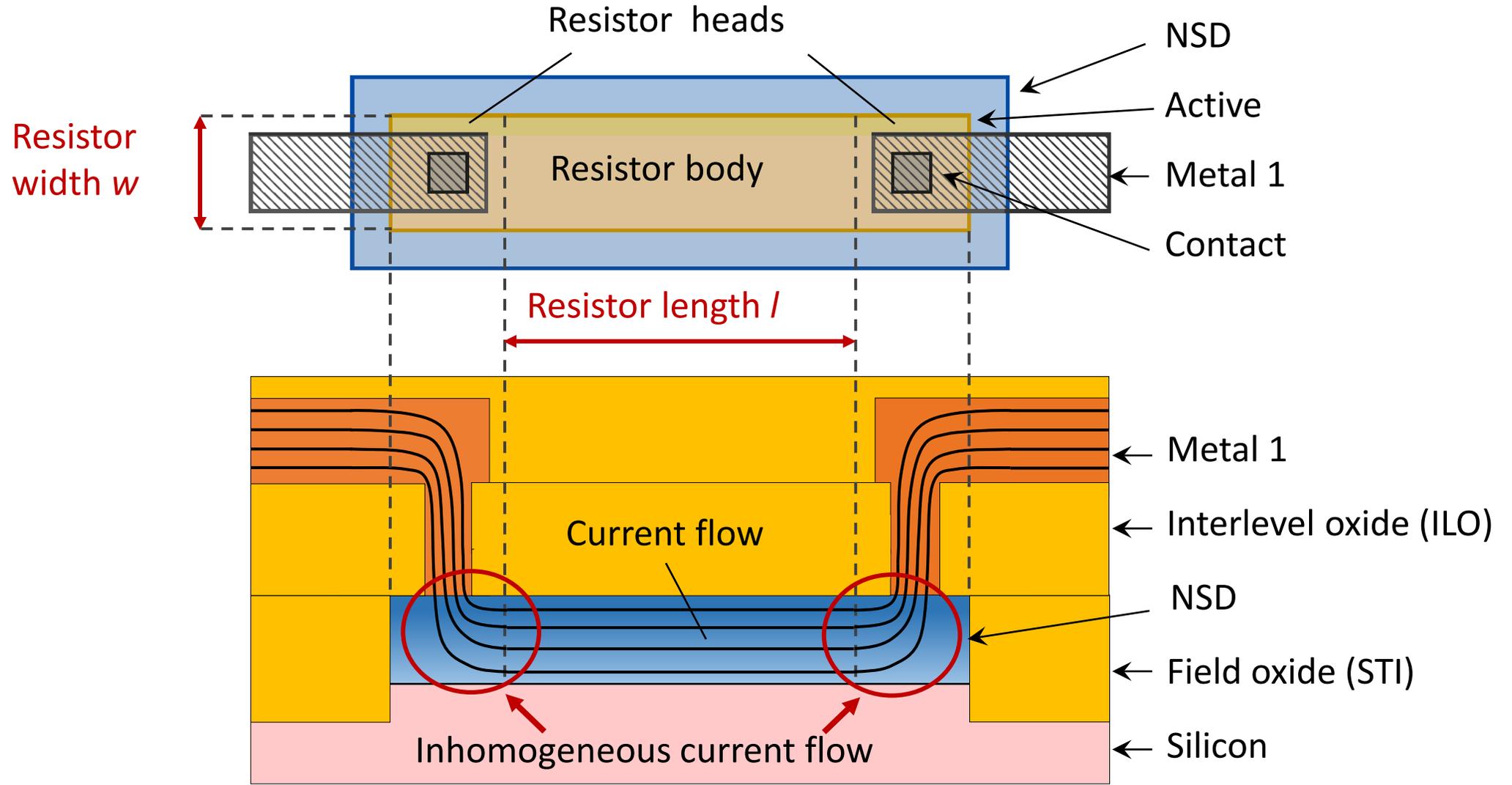
Layout

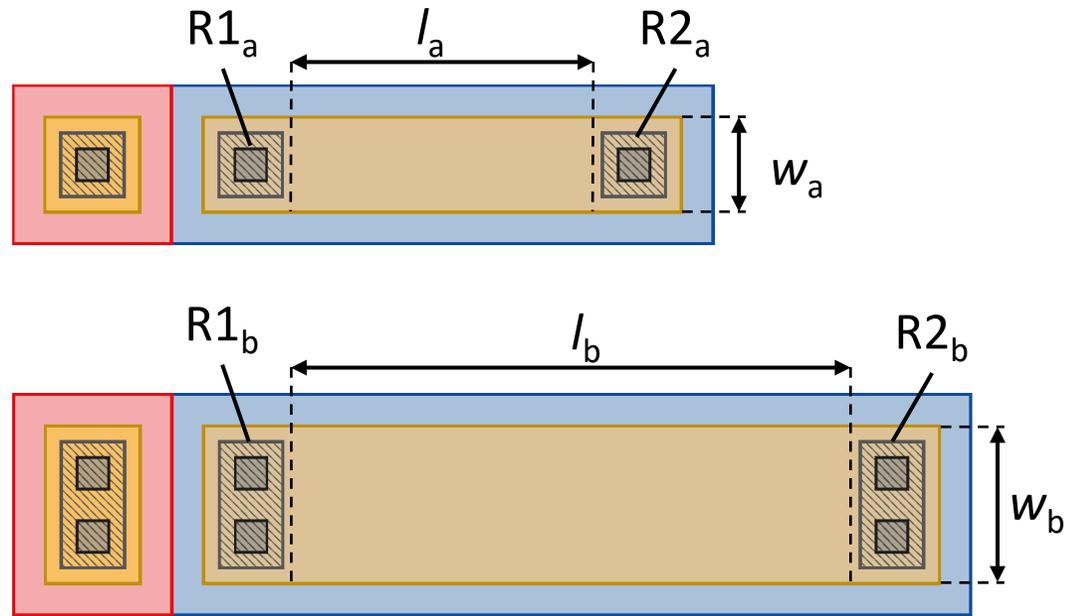


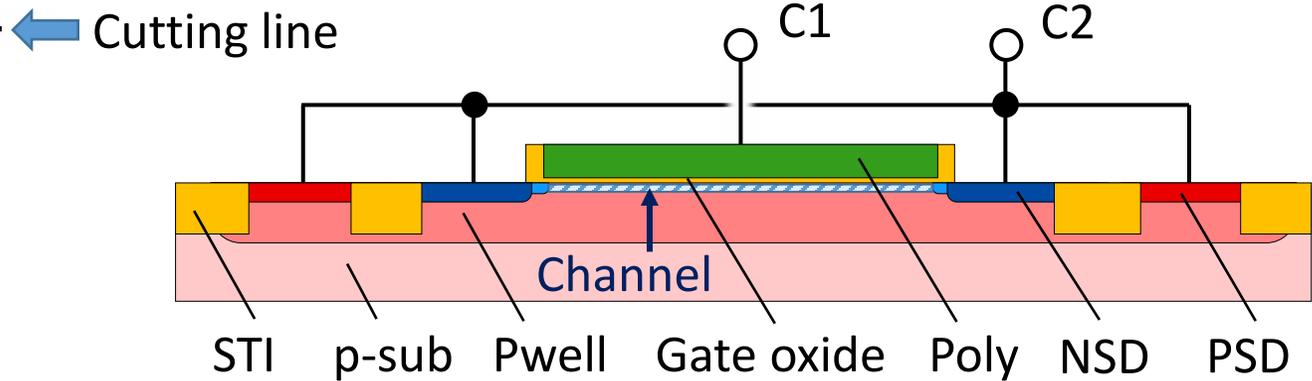
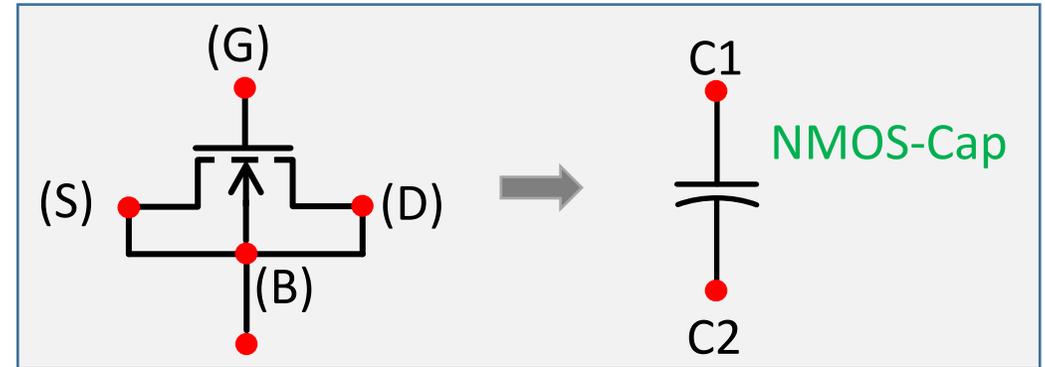
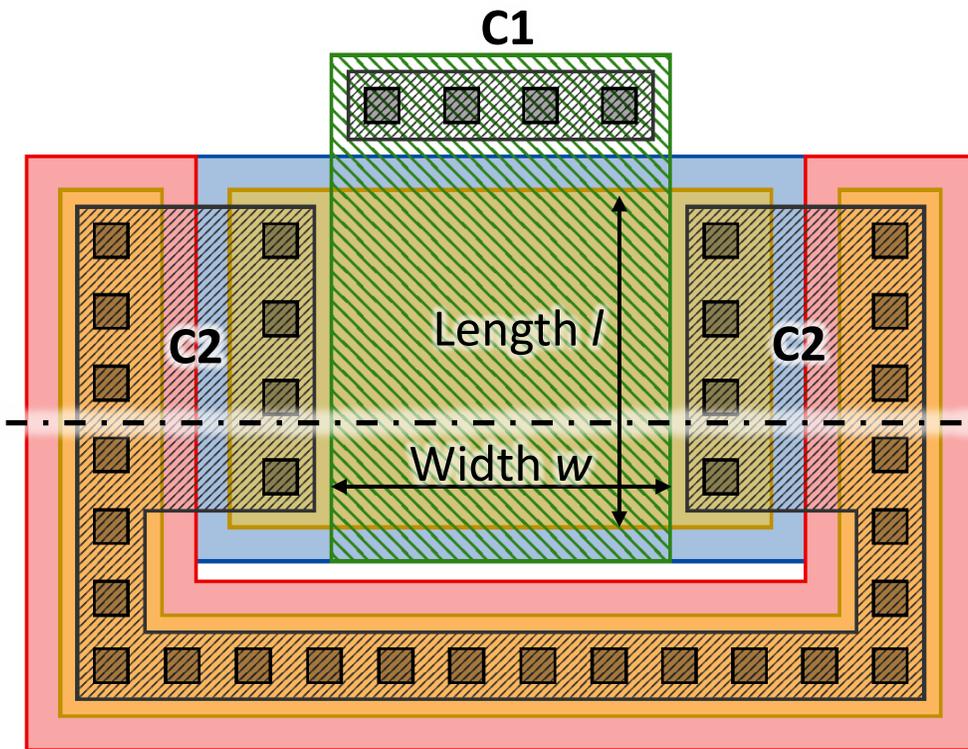
Sectional view

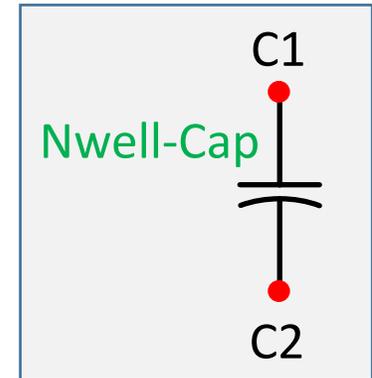
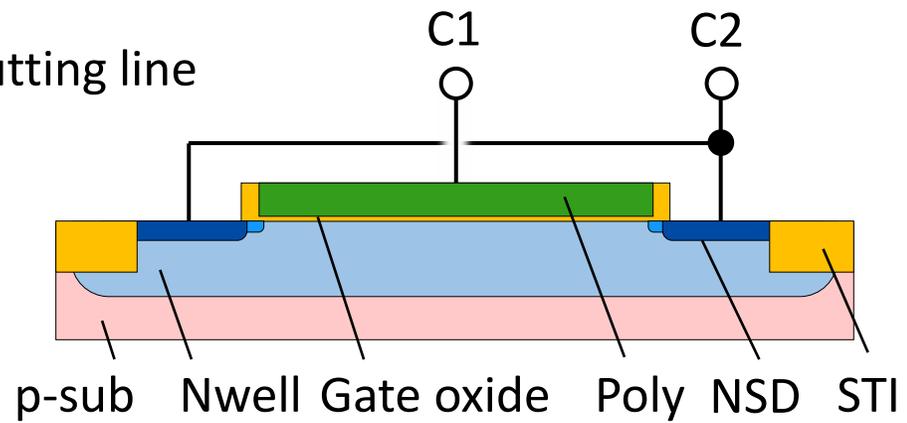
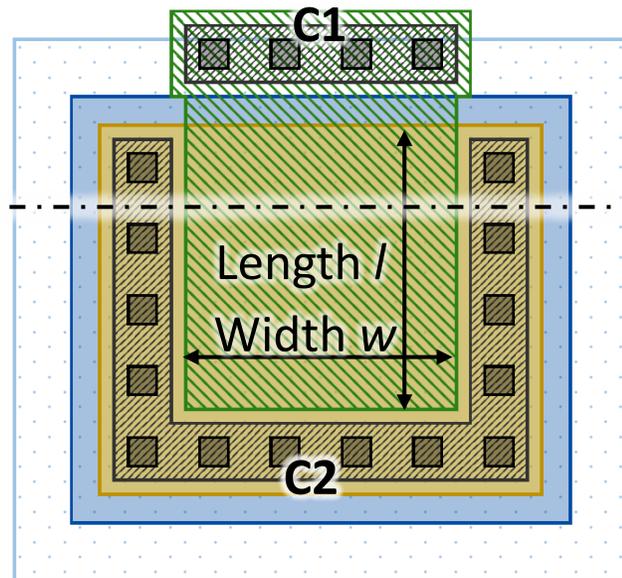


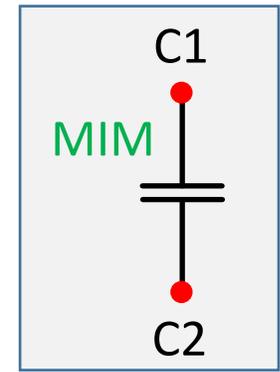
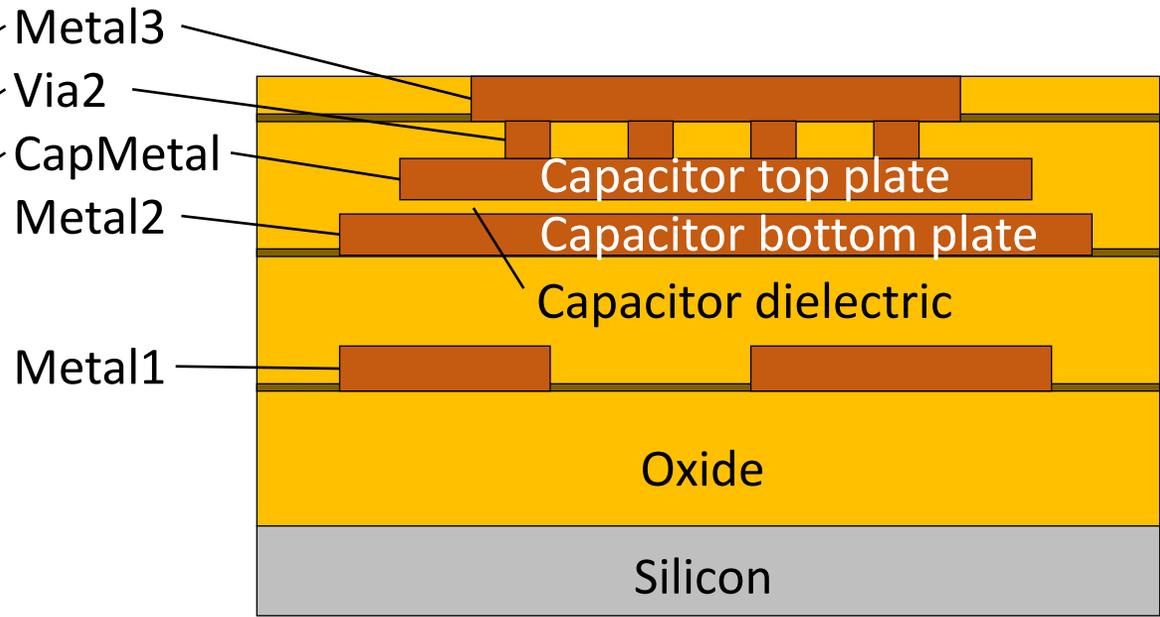
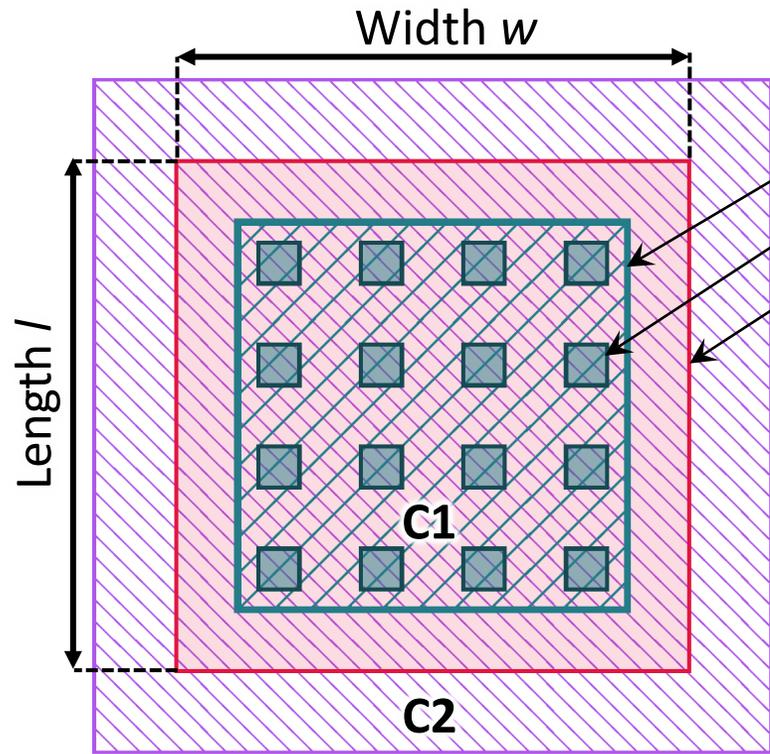
Schematic

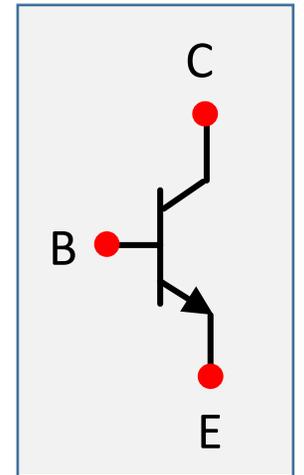
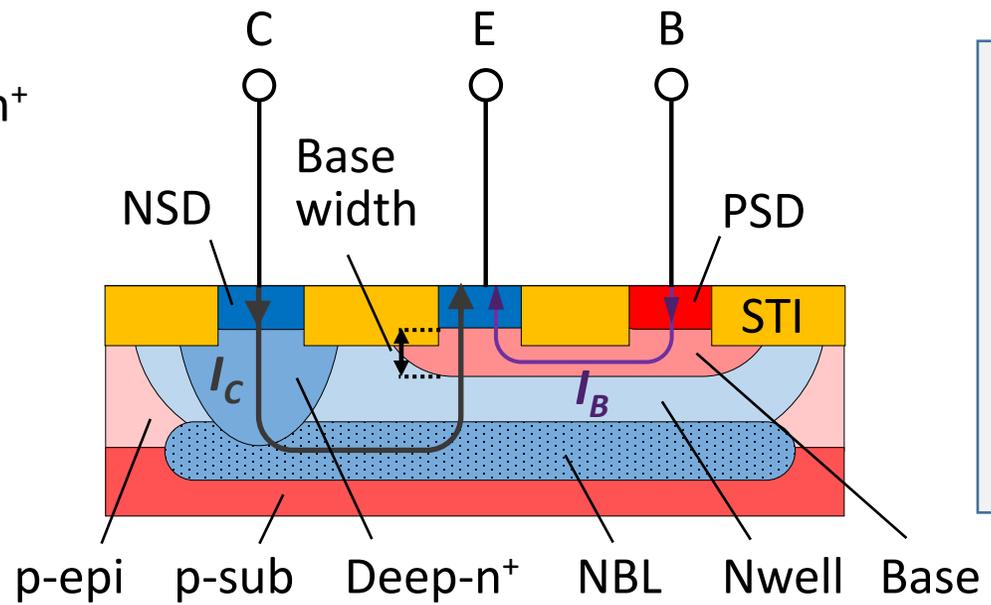
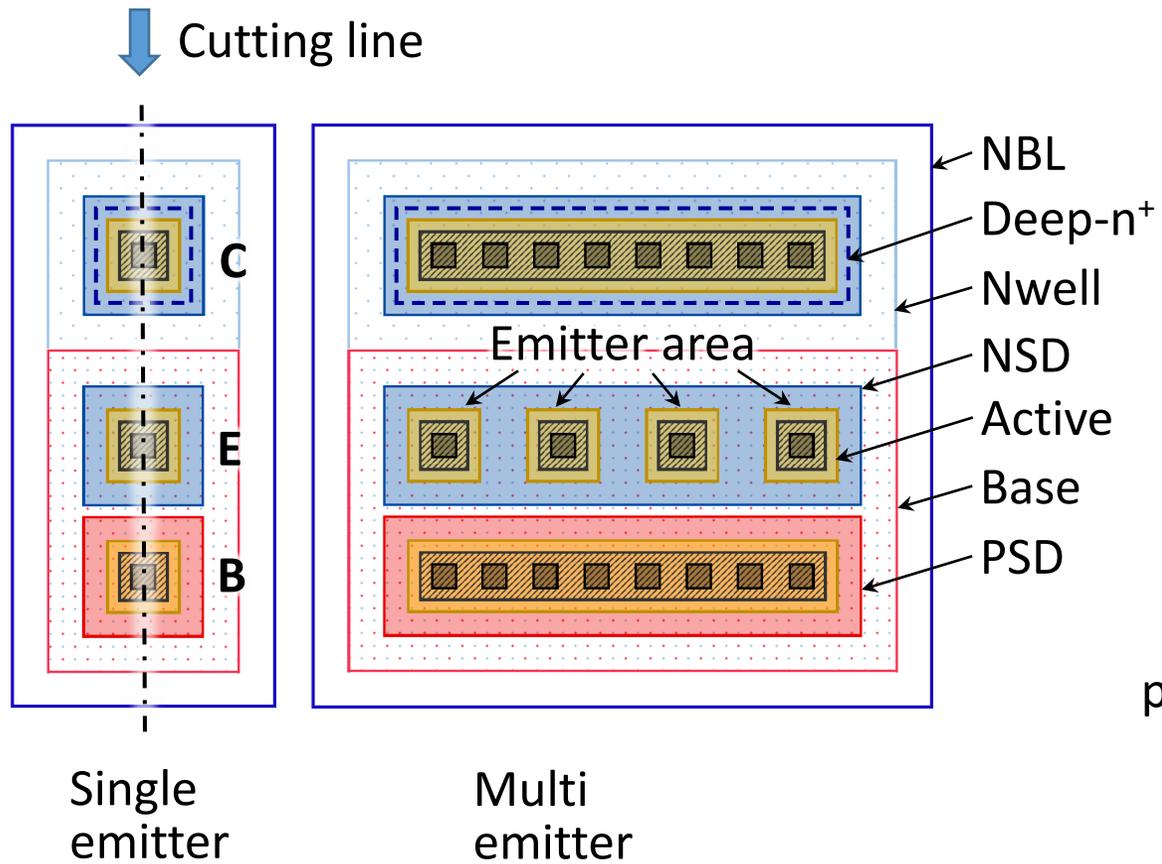


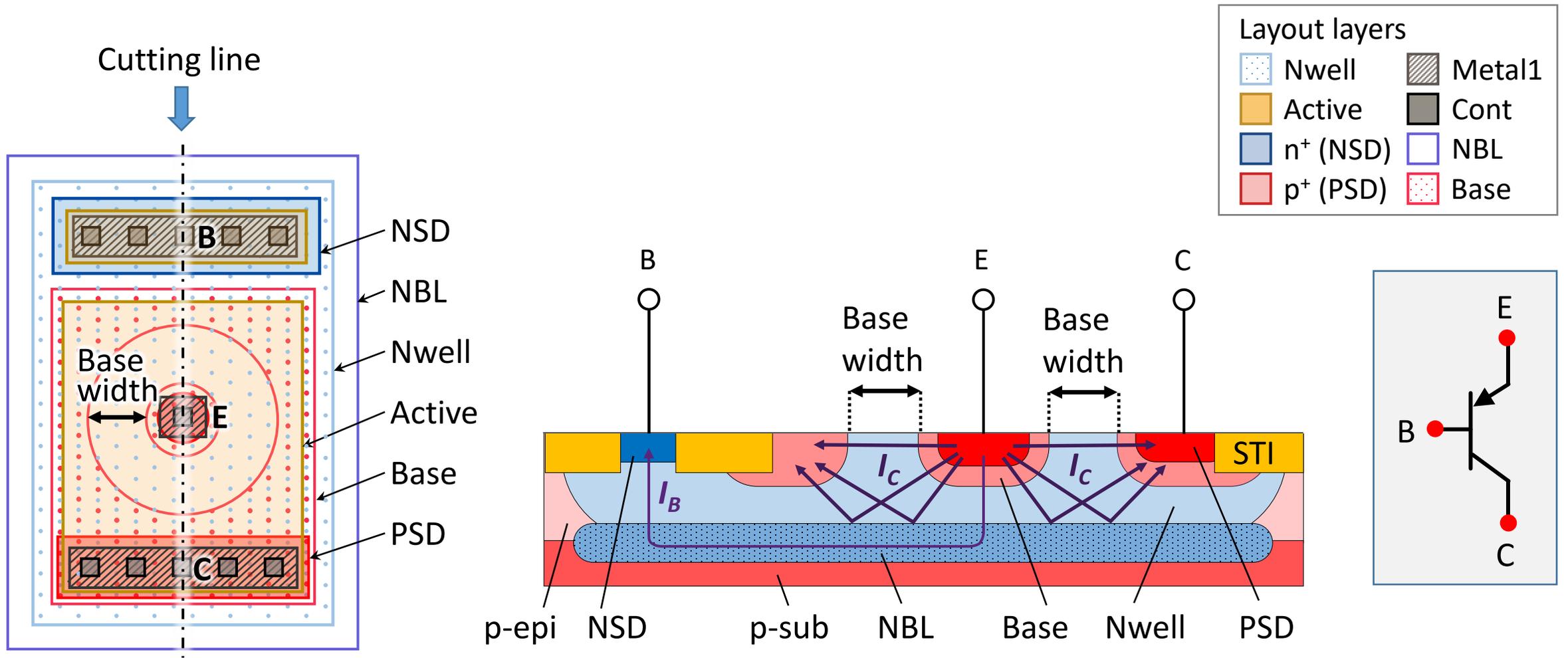


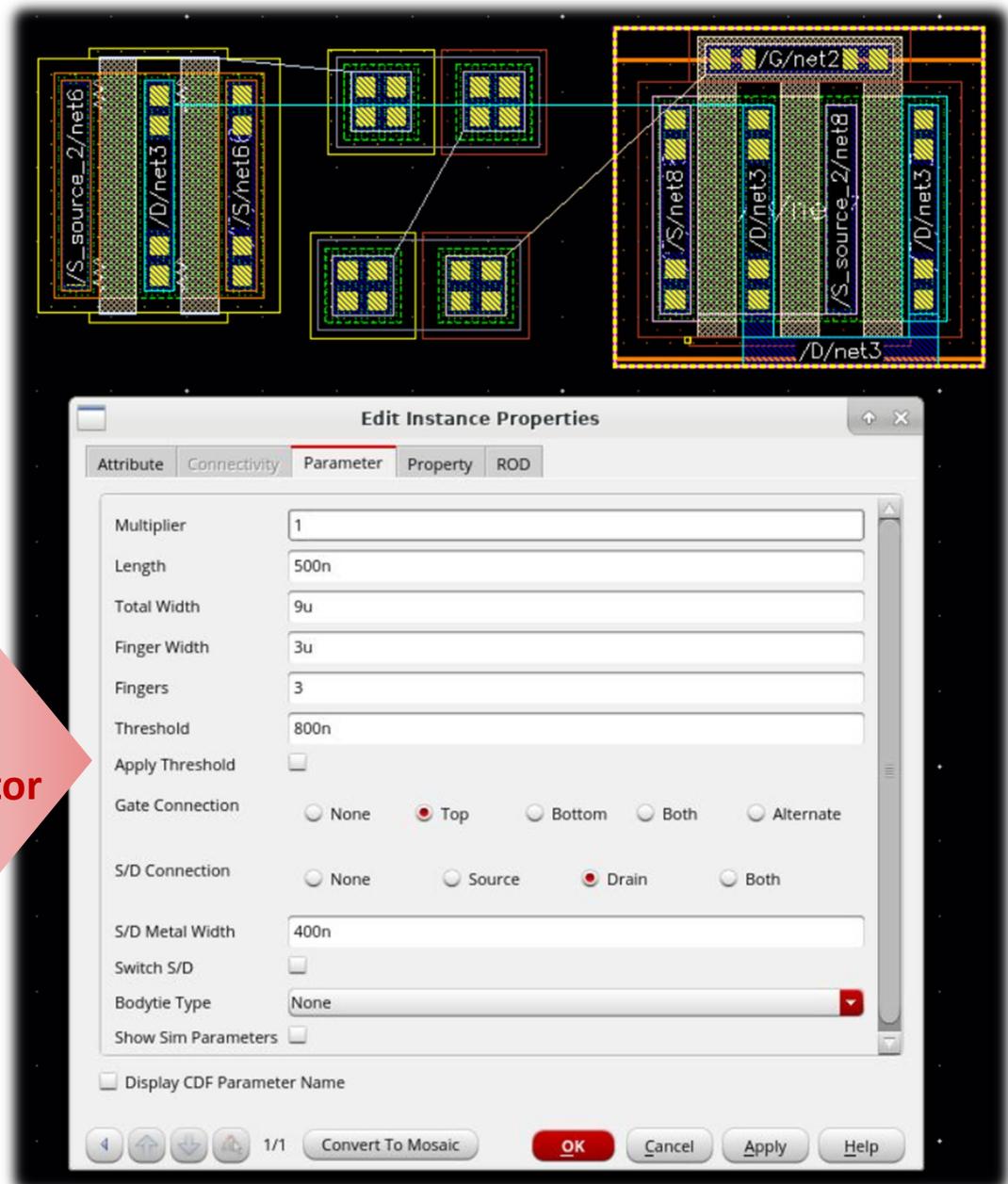
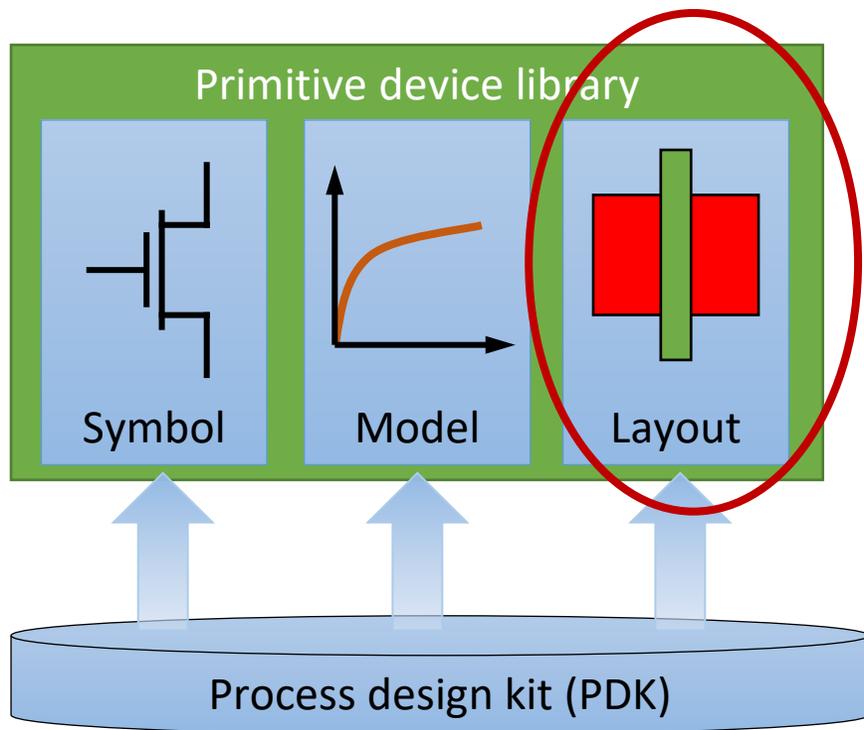




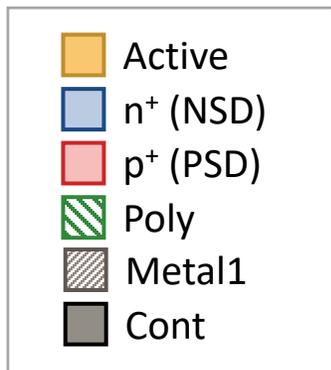
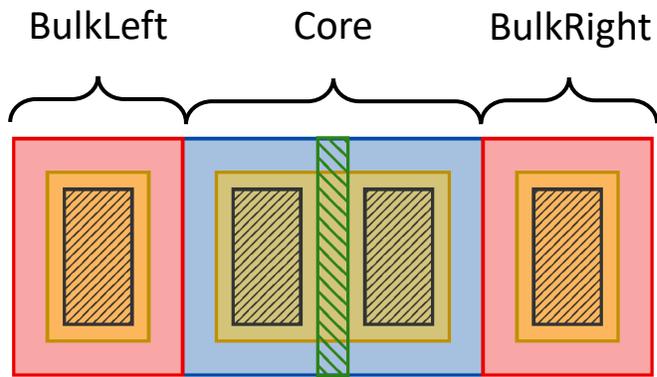




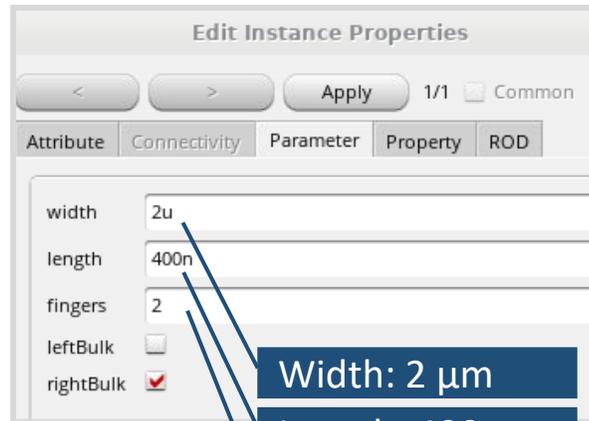




Command	Line	Parameters	
set	1	Active = list("Oxide" "drawing"), Poly = list("Poly" "drawing"), NSD = list("Nimp" "drawing"), PSD = list("Pimp" "drawing")	
block	2	"Create initial shapes."	
group	3	Shapes "nil"	LayerName {coordinates $x_1:y_1, x_2:y_2, x_3:y_3, x_4:y_4$ }
group	4	Core -	
rectangle	5	Active {-0.6:0.0, 0.78:0.0, 0.78:1.0, -0.6:1.0}	Create 5 rectangles for MOS-FET core
rectangle	6	Poly {0.0:-0.205, 0.18:-0.205, 0.18:1.205, 0.0:1.205}	
rectangle	7	NSD {-0.8:-0.2, 0.98:-0.2, 0.98:1.2, -0.8:1.2}	
rectangle	8	Metal1 {0.28:0.1, 0.68:0.1, 0.68:0.9, 0.28:0.9}	
rectangle	9	Metal1 {-0.5:0.1, -0.1:0.1, -0.1:0.9, -0.5:0.9}	
group	10	BulkLeft "nil"	
rectangle	11	Active {-1.6:0.0, -1.0:0.0, -1.0:1.0, -1.6:1.0}	Create 3 rectangles for left bulk contact
rectangle	12	PSD {-1.8:-0.2, -0.8:-0.2, -0.8:1.2, -1.8:1.2}	
rectangle	13	Metal1 {-1.5:0.1, -1.1:0.1, -1.1:0.9, -1.5:0.9}	
group	14	BulkRight "nil"	
rectangle	15	Active {1.18:0.0, 1.78:0.0, 1.78:1.0, 1.18:1.0}	Create 3 rectangles for right bulk contact
rectangle	16	PSD {0.98:-0.2, 1.98:-0.2, 1.98:1.2, 0.98:1.2}	
rectangle	17	Metal1 {1.28:0.1, 1.68:0.1, 1.68:0.9, 1.28:0.9}	
block	18	"Stretch transistor channel."	
set	19	fFingerWidth = width - 1	Calculate stretch lengths
set	20	fLength = length - 0.18	
stretch	21	{Group Shapes} east <fLength:0 R0>	Perform stretch operations
stretch	22	{Group Shapes} north <0:fFingerWidth R0>	
block	23	"Create fingers through duplication."	
set	24	fPitch = 0	
repeat	25	"finger" [f: fingers - 1]	Copy (fingers-1) times the MOS-FET core with (fPitch) in x-direction
set	26	fPitch = (finger+1)*(0.78+fLength)	
copy	27	{Group Core} <fPitch:0 R0> "t" "t" - must	Move right bulk (fPitch) in x-direction
move	28	{Group BulkRight} <fPitch:0 R0>	
merge	29	{F: (append (group ("Core") (layer evalstring("Active"))) (layer evalstring("NSD"))))}	
block	30	"Keep or delete bulks."	
unless	31	[f: leftBulk]	Delete bulk contacts depending on values of „leftBulk“ and „rightBulk“
delete	32	{Group BulkLeft}	
unless	33	[f: rightBulk]	Create 1 dummy contact
delete	34	{Group BulkRight}	
block	35	"Create contact holes."	
rectangle	36	oCont Cont {0.0:-0.5, 0.2:-0.5, 0.2:-0.3, 0.0:-0.3}	Pitch Overlap
fill	37	{Name oCont} {F: (append (layer evalstring("Metal1")) [f: 0.4] [f: 0.4] "nil" [f: 0.1] "distribute" "distribute")}	Fill all Metal1 with this contact shape
delete	38	{Name oCont}	Delete dummy contact

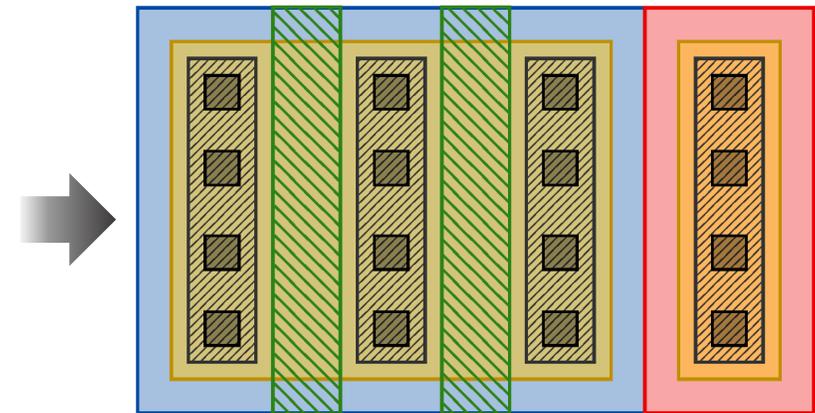


Initial layout



Width: 2 μm
Length: 400 nm
Fingers: 2

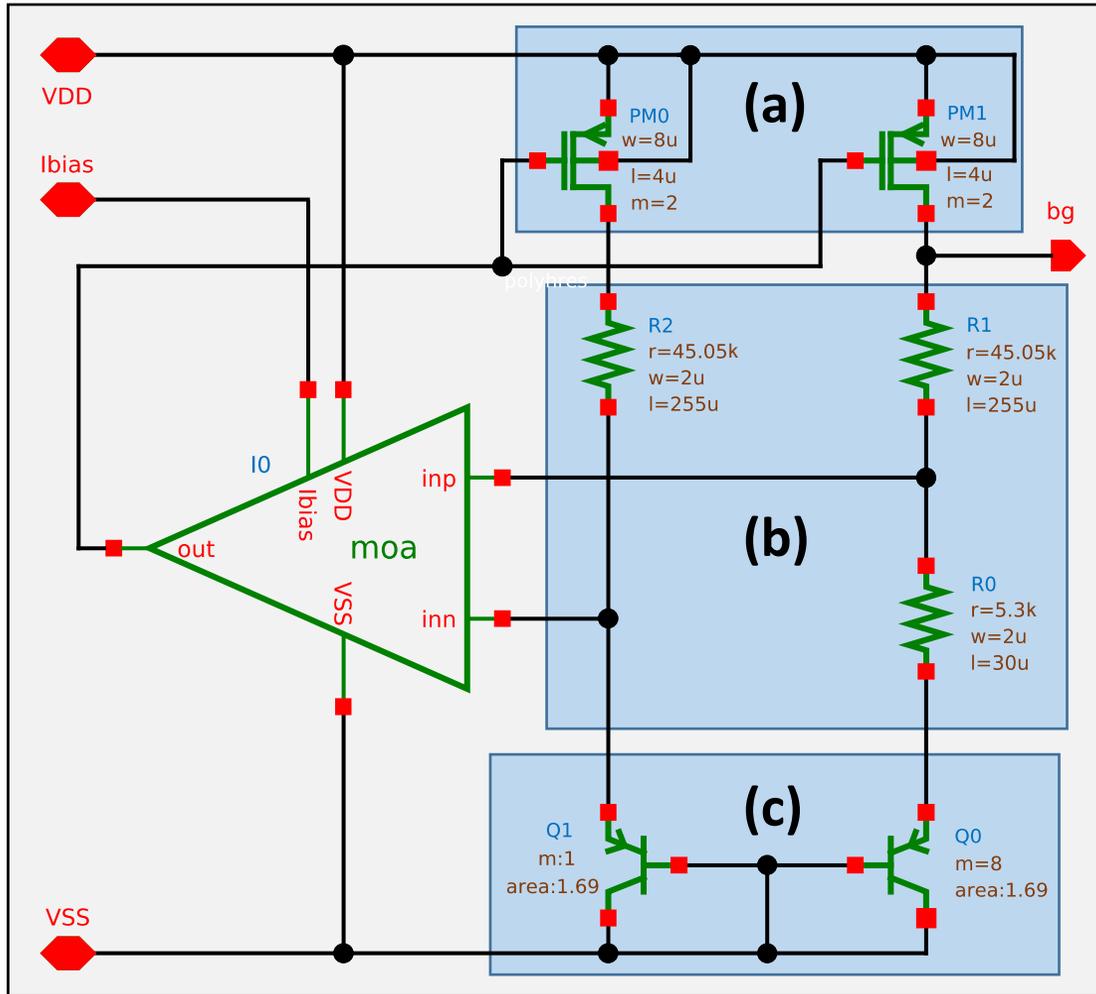
PCell menu



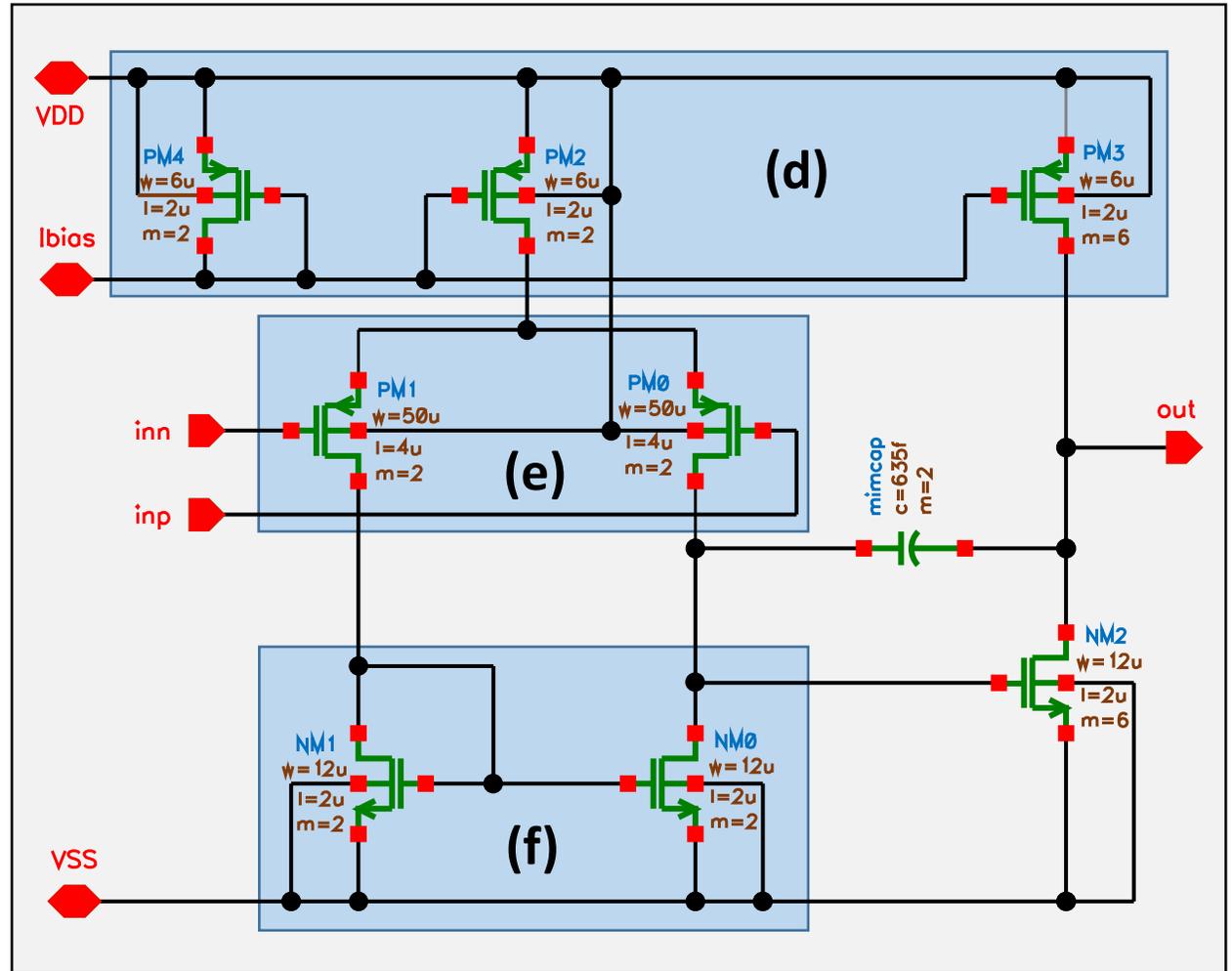
Generated PCell instance

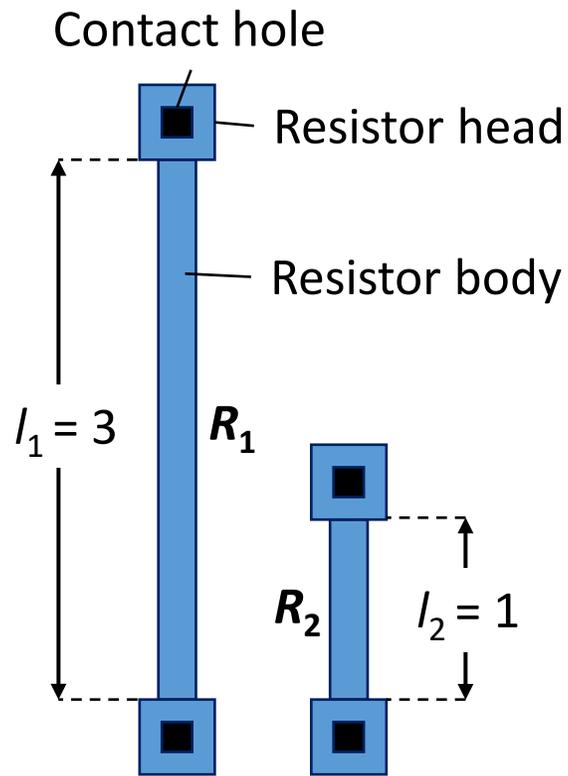
Manufacturing-specific “distance” (fabrication history)		Relative accuracy
Within a fab	From lot to lot	$\pm 30\%$
Within a lot	From wafer to wafer	$\pm 20\%$
Within a wafer	From reticle section to reticle section	$\pm 15\%$
Within a reticle	From chip to chip	$\pm 10\%$
Within a chip	Arbitrary	$\pm 5\%$
Within a chip	With further layout measures	$\pm 1\%$ to $\pm 0.01\%$

Bandgap

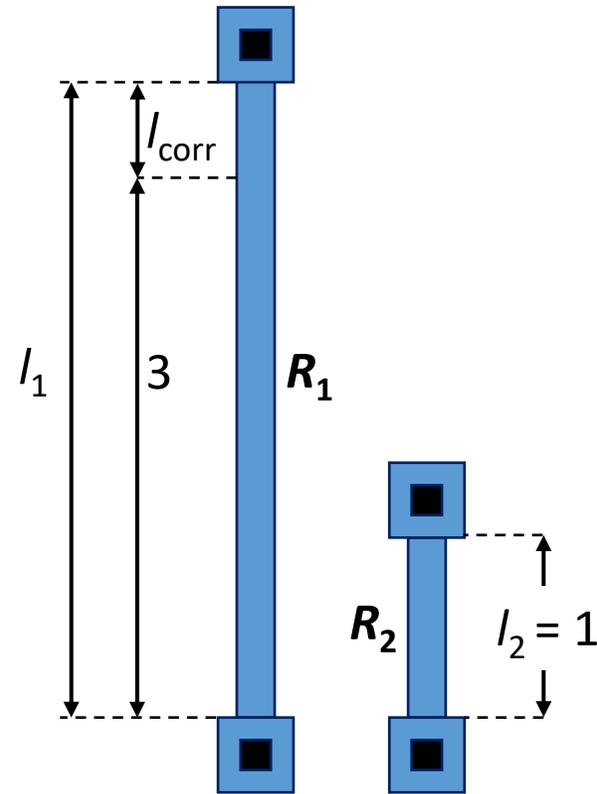


Miller opamp „moa“

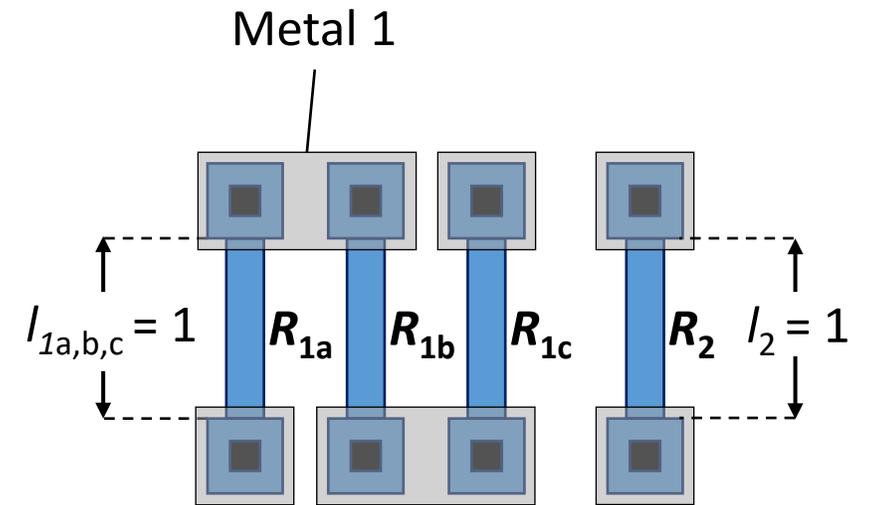




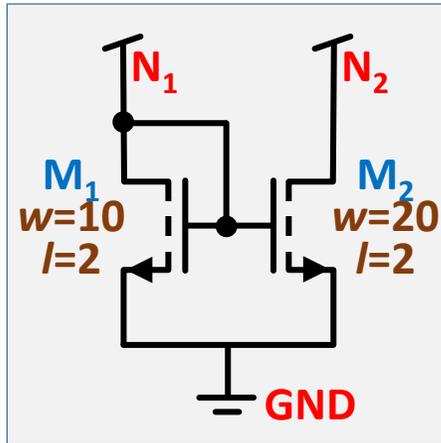
$R_1 < 3R_2 \rightarrow$ **no matching!**



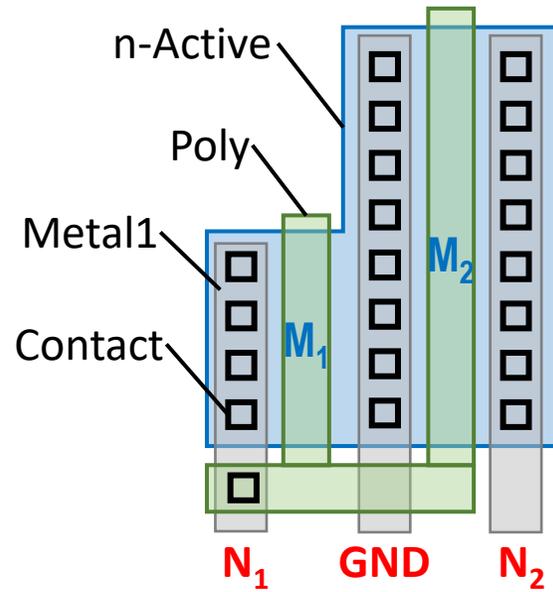
$R_1 \approx 3R_2 \rightarrow$ **bad matching!**



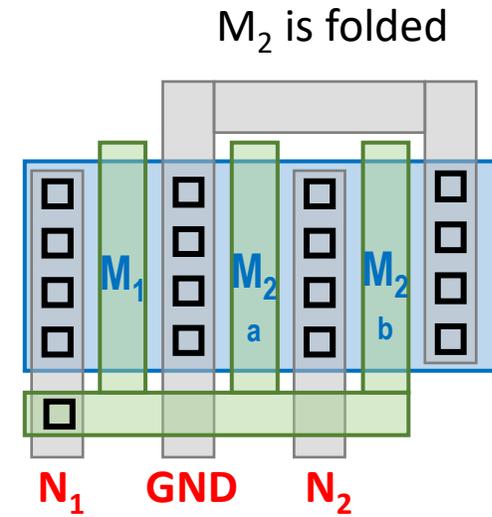
$R_1 = 3R_2 \rightarrow$ **good matching!**



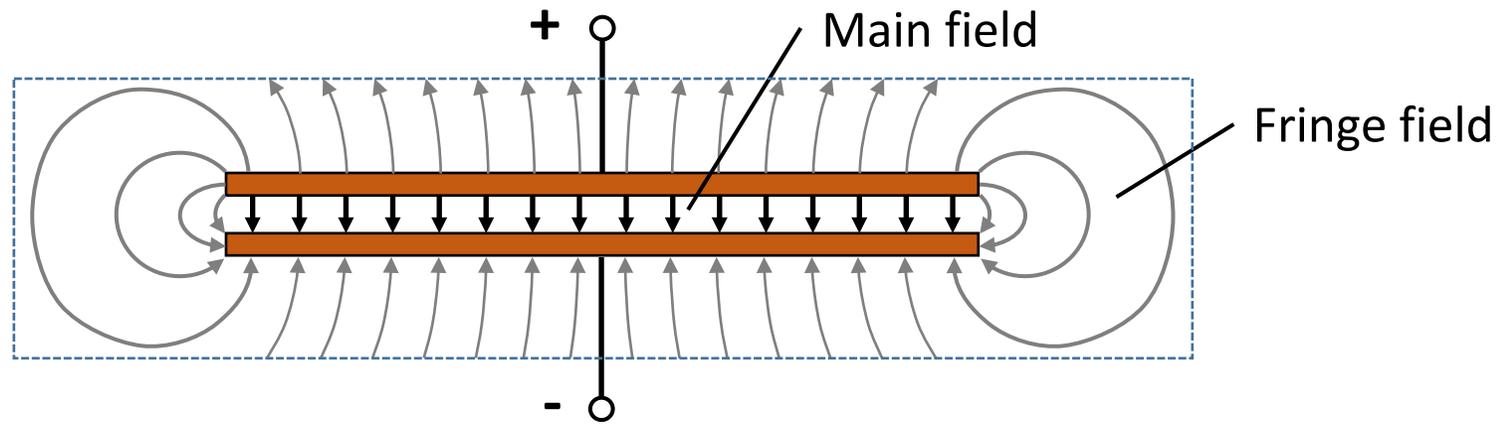
Current mirror circuit

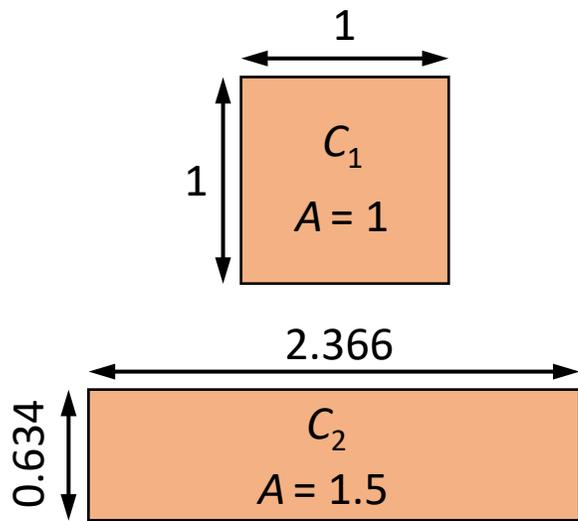


No splitting → **bad matching!**

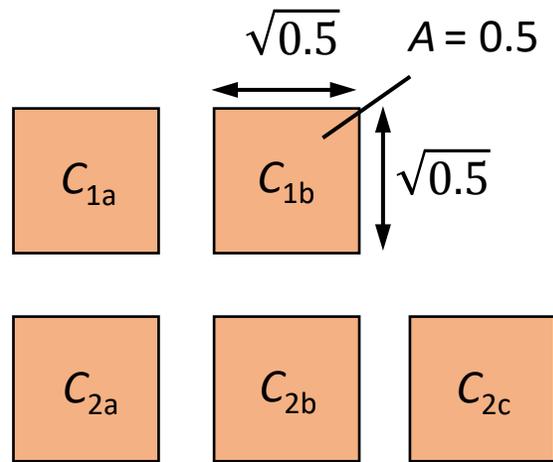


Splitting → **good matching!**

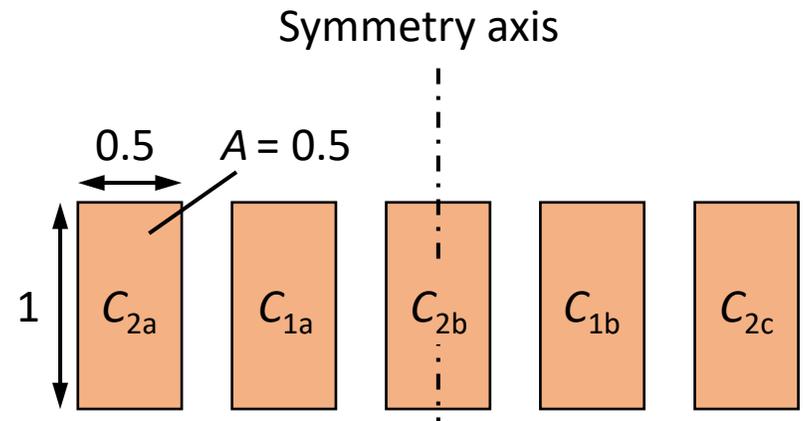




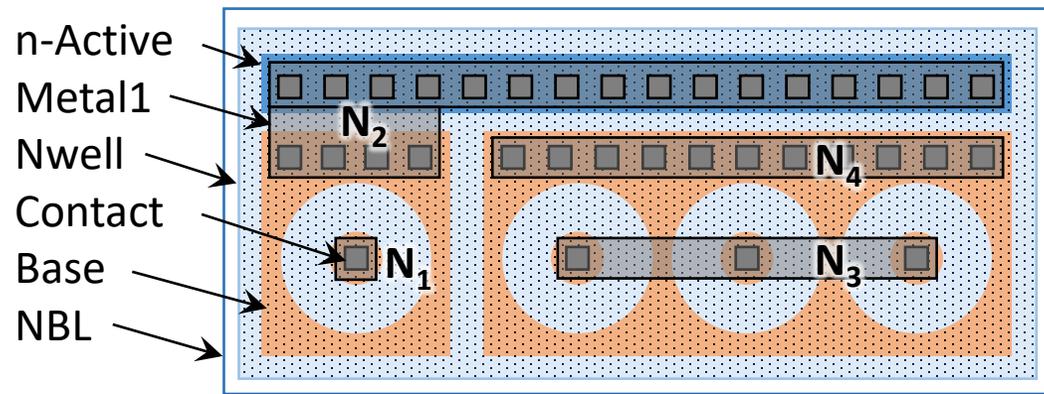
Minimum matching



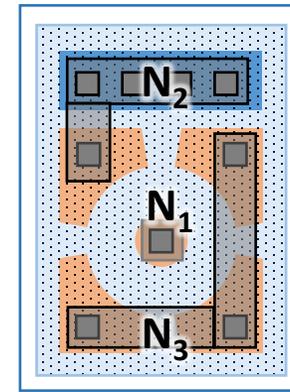
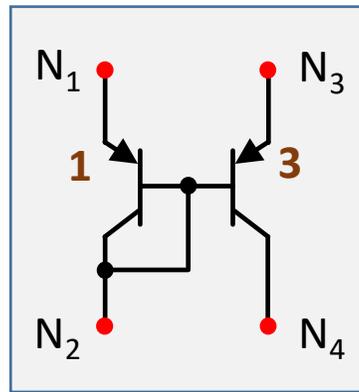
Good matching



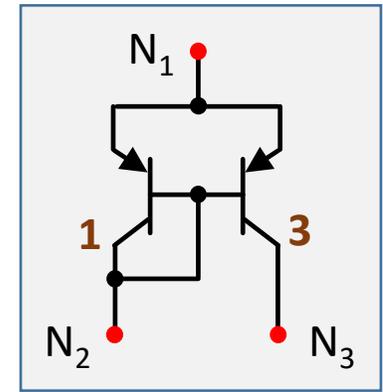
Very good matching

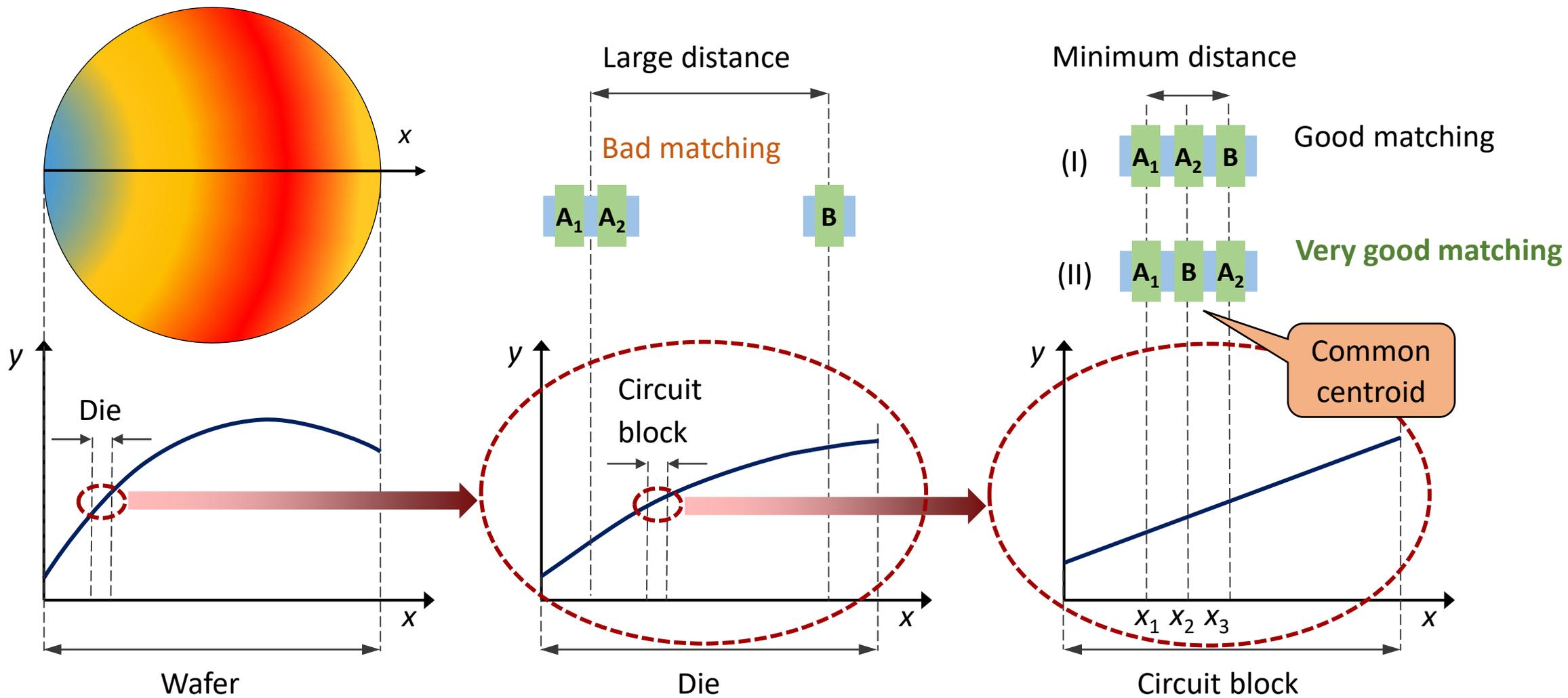


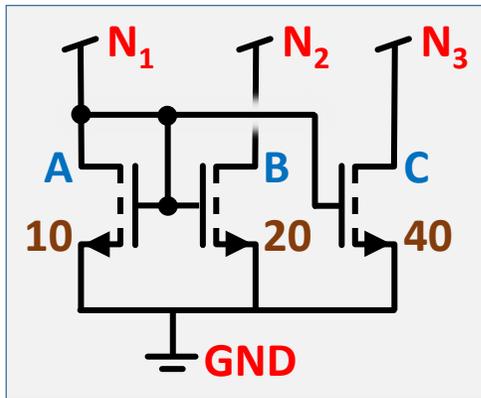
Multi-emitter PNP transistor



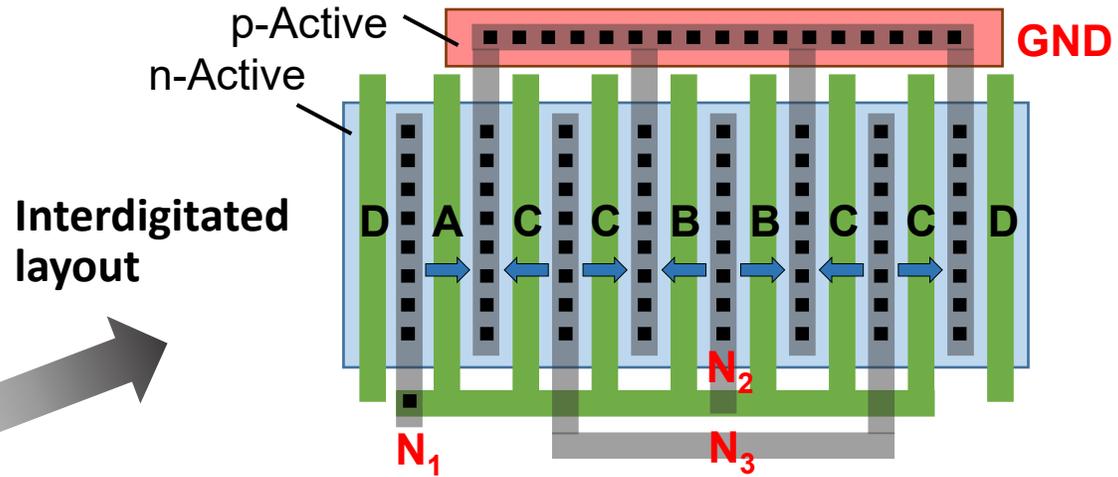
Multi-collector PNP transistor



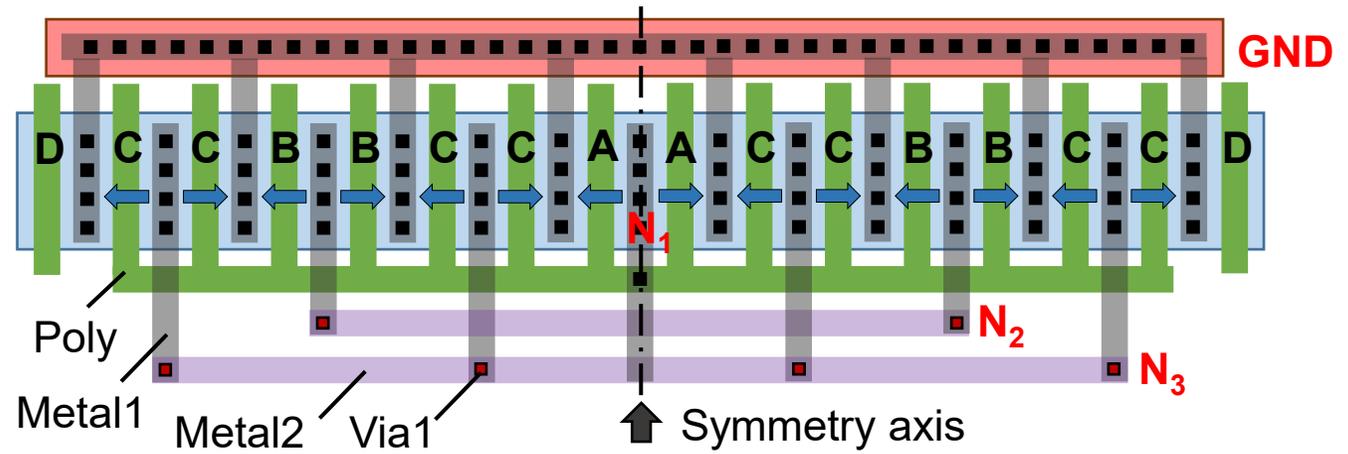


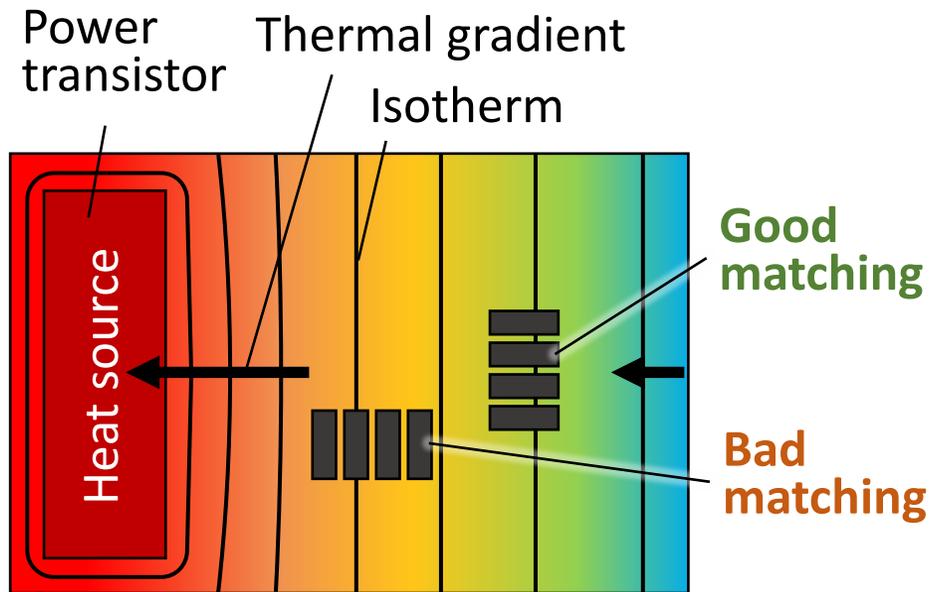


Current mirror schematic

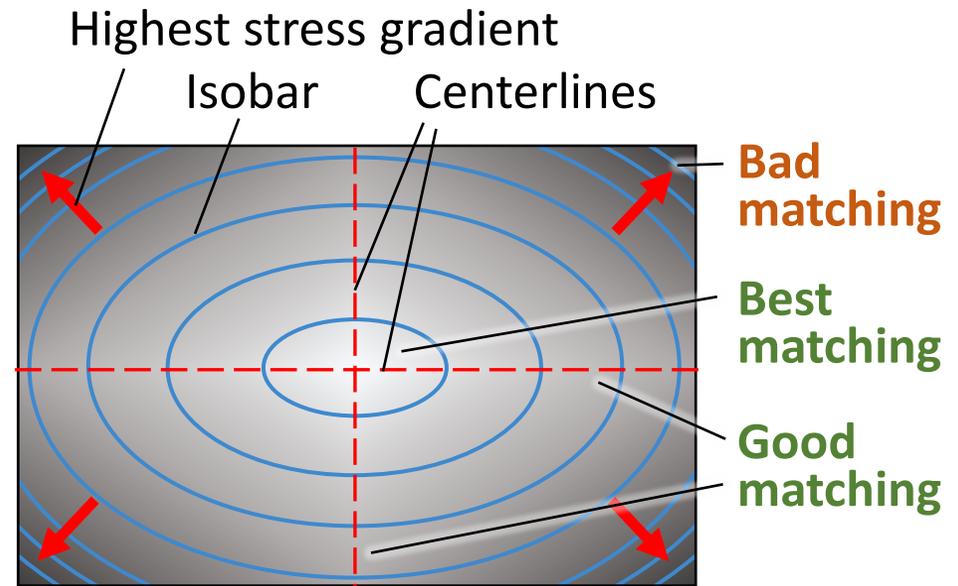


Common centroid layout

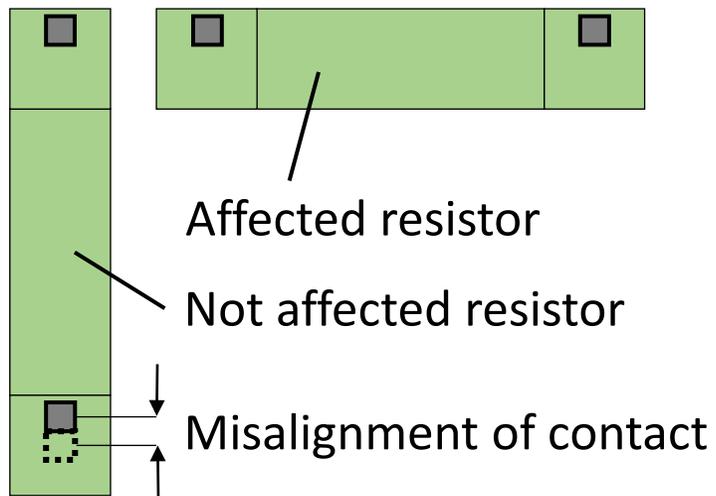




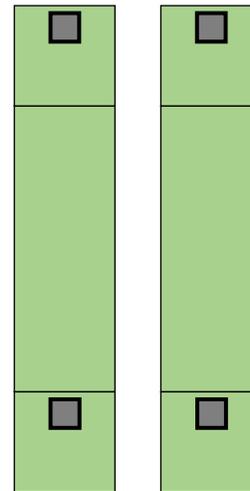
Thermal distribution



Mechanical stress



Bad matching

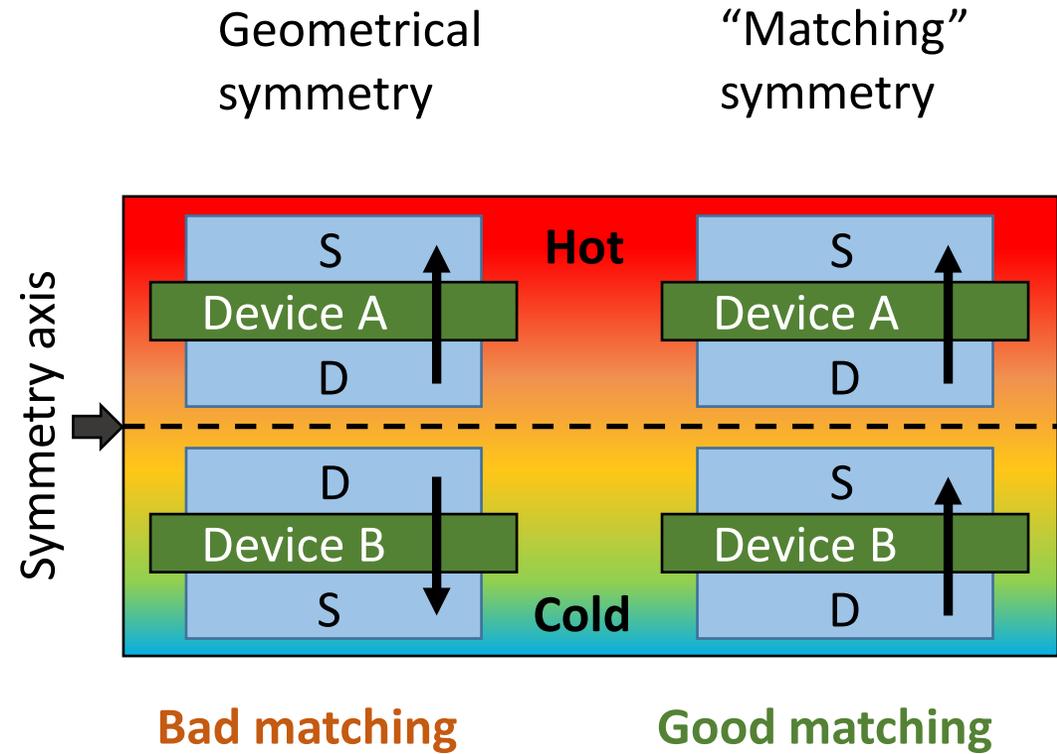
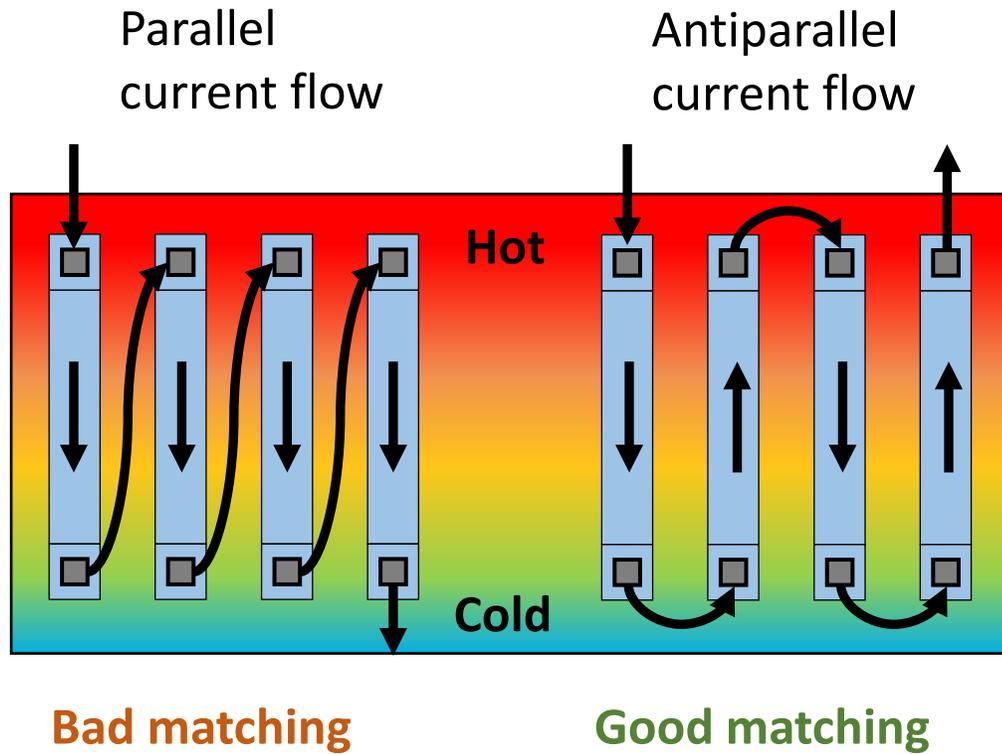


Good matching



Both resistors are affected in the same way

Good matching



(a) Matching for normal requirements	Devices	Effect / explanation
Same device type	all	Prerequisite for matching!
Same size and shape (Splitting in identical basic elements)	all	Internal device fringe effects (Sect. 6.6.1)
Minimum distance	all	Unknown gradients (Sect. 6.6.2)
Same orientation	R, T	Alignment tolerances, carrier mobility (Sect. 6.6.5)
Same ratio of area to perimeter as an alternative to splitting	C	Internal device fringe effects (Sect. 6.6.1)
(b) Matching for higher requirements		
Interdigitation 1- or 2-dimensional	all	Unknown gradients (Sect. 6.6.2)
Same temperature (placing along isotherms)	all	Thermal gradient (known gradient) (Sect. 6.6.4)
Same environment (dummy elements)	all	External device fringe effects (Sect. 6.6.3)
Consider current flow direction	R, T	Thermoelectric effect (Sect. 6.6.5)
Increase dimensions	R, T	Internal device fringe effects (Sect. 6.6.1)
Distance to well border $>1\mu\text{m}$	M	Well proximity effect (Sect. 6.6.3)
(c) Matching for highest requirements		
Common centroid layout	all	Unknown gradients (Sect. 6.6.2)
Placement in low stress chip regions	all	Carrier mobility (Sect. 6.6.5)
Symmetrical routing	all	Depending on circuit function