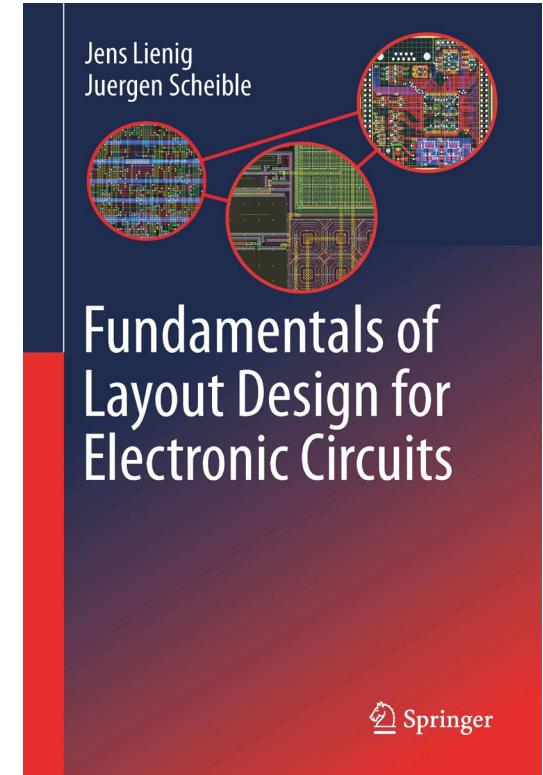


- 5.1 Generating a Netlist Using Hardware Description Language
- 5.2 Generating a Netlist Using Symbolic Design Entry
- 5.3 Primary Steps in Physical Design
- 5.4 Verification
- 5.5 Layout Post Processing



# Chapter 5: Steps in Physical Design: From Netlist Generation to Layout Post Processing

## 5.1 Generating a Netlist Using Hardware Description Language

- 5.1.1 Overview and History
- 5.1.2 Elements and Example
- 5.1.3 Flow

## 5.2 Generating a Netlist Using Symbolic Design Entry

- 5.2.1 Overview
- 5.2.2 Elements and Examples
- 5.2.3 Netlist Generation

## 5.3 Primary Steps in Physical Design

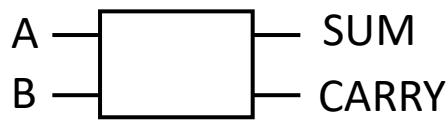
- 5.3.1 Partitioning and Floorplanning
- 5.3.2 Placement
- 5.3.3 Routing
- 5.3.4 Physical Design Using Symbolic Compaction
- 5.3.5 Physical Design Using Standard Cells
- 5.3.6 Physical Design of Printed Circuit Boards

## 5.4 Verification

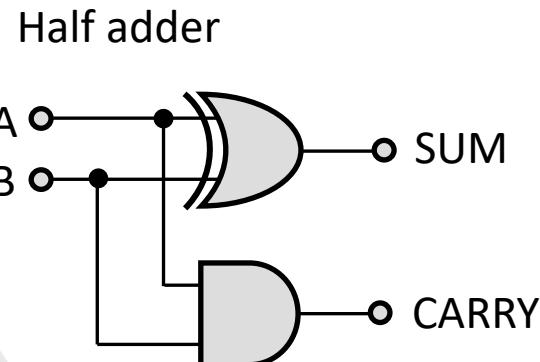
- 5.4.1 Fundamentals
- 5.4.2 Formal Verification
- 5.4.3 Functional Verification: Simulation
- 5.4.4 Timing Verification
- 5.4.5 Geometric Verification: DRC, ERC
- 5.4.6 Extraction and LVS

## 5.5 Layout Post Processing

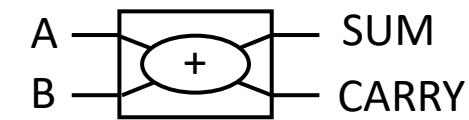
Entity with  
interface description



```
entity HALFADDER is
    port(A, B      : in bit;
         SUM, CARRY: out bit);
end entity HALFADDER;
```

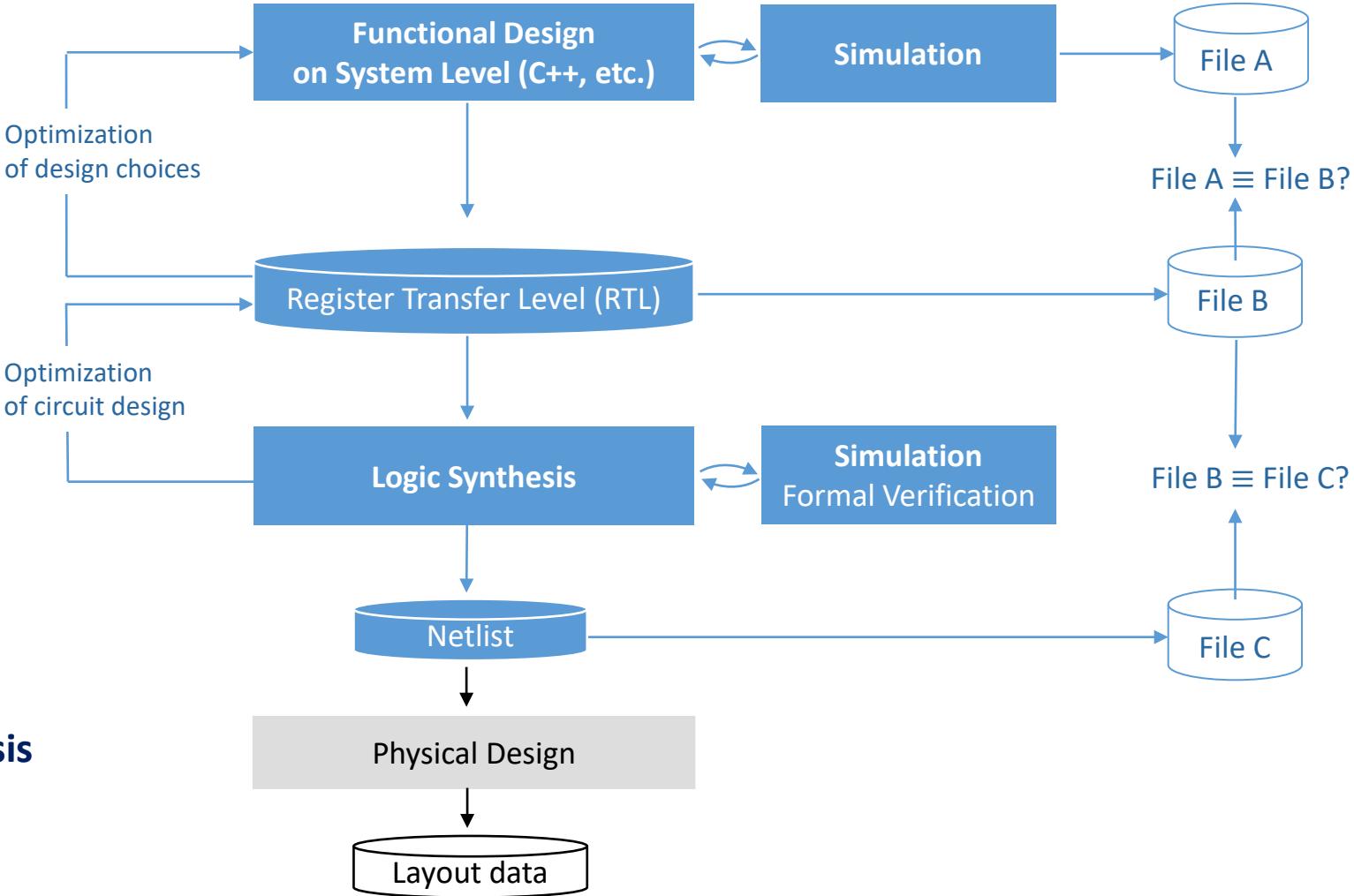


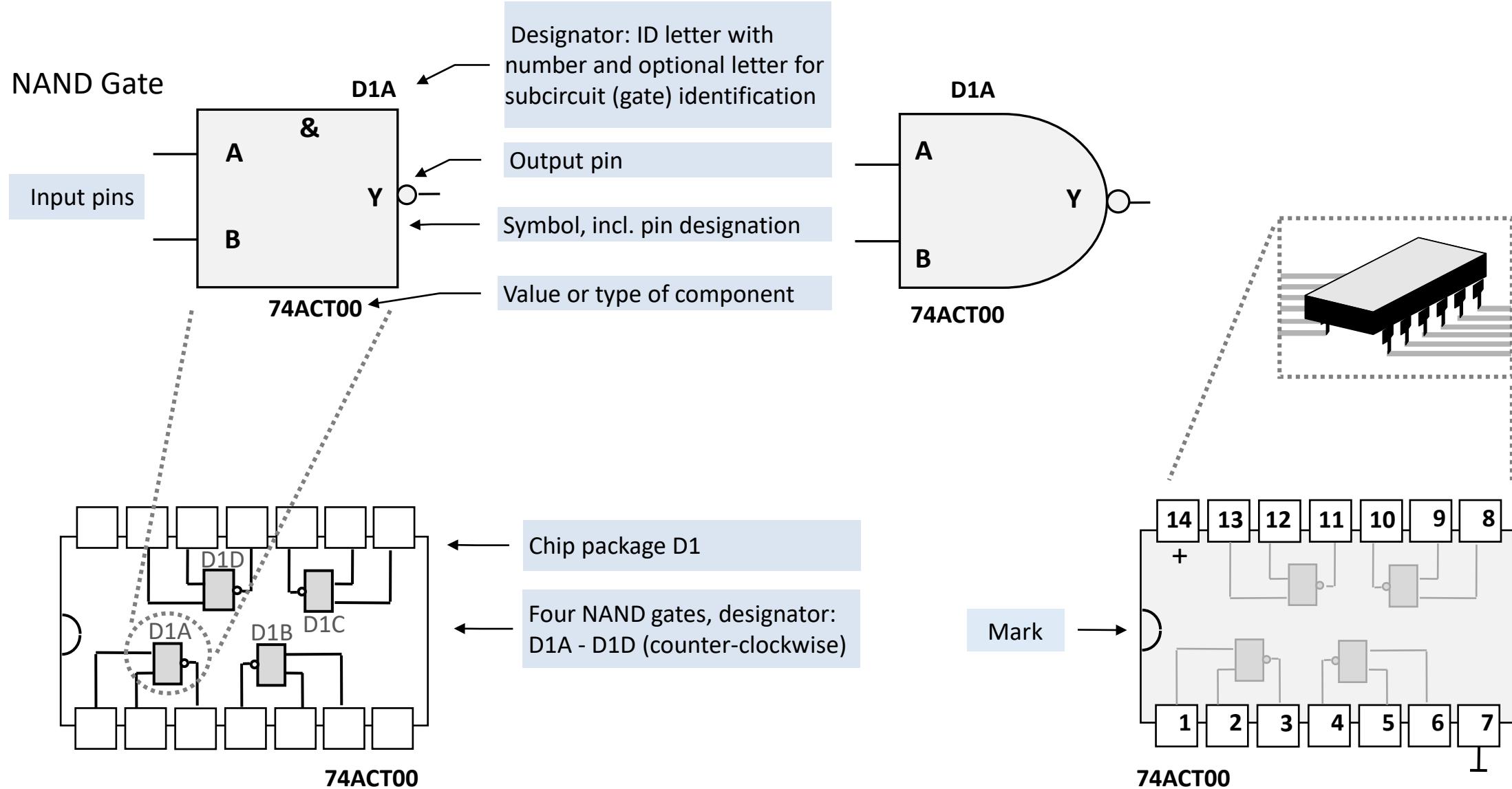
Architecture with  
implementation



```
architecture RTL of HALFADDER is
begin
    SUM  <= A xor B;
    CARRY <= A and B;
end architecture RTL;
```

## Behavior Level Synthesis

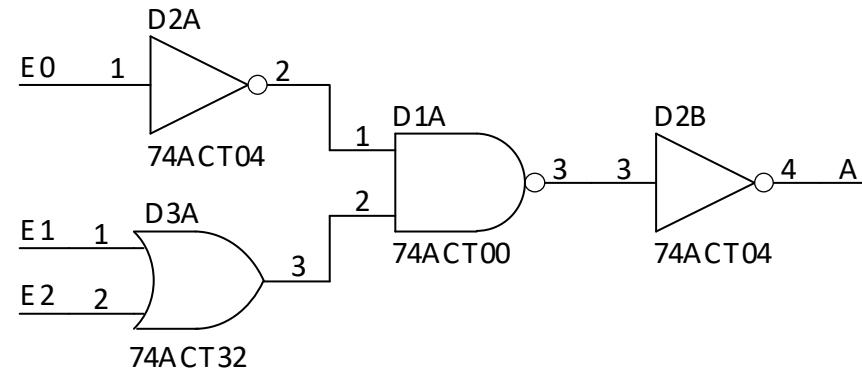
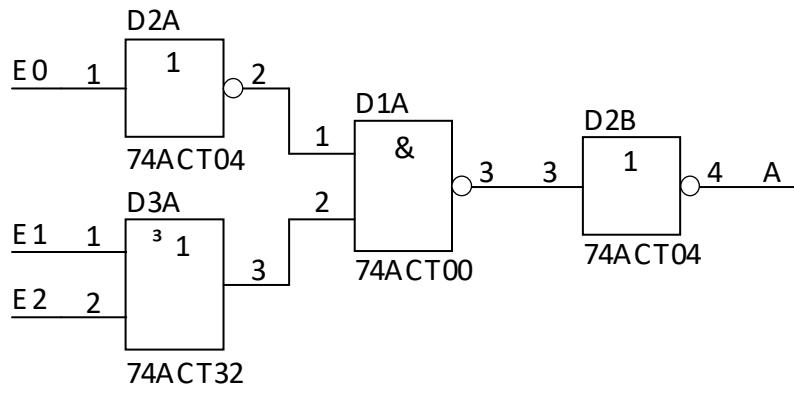


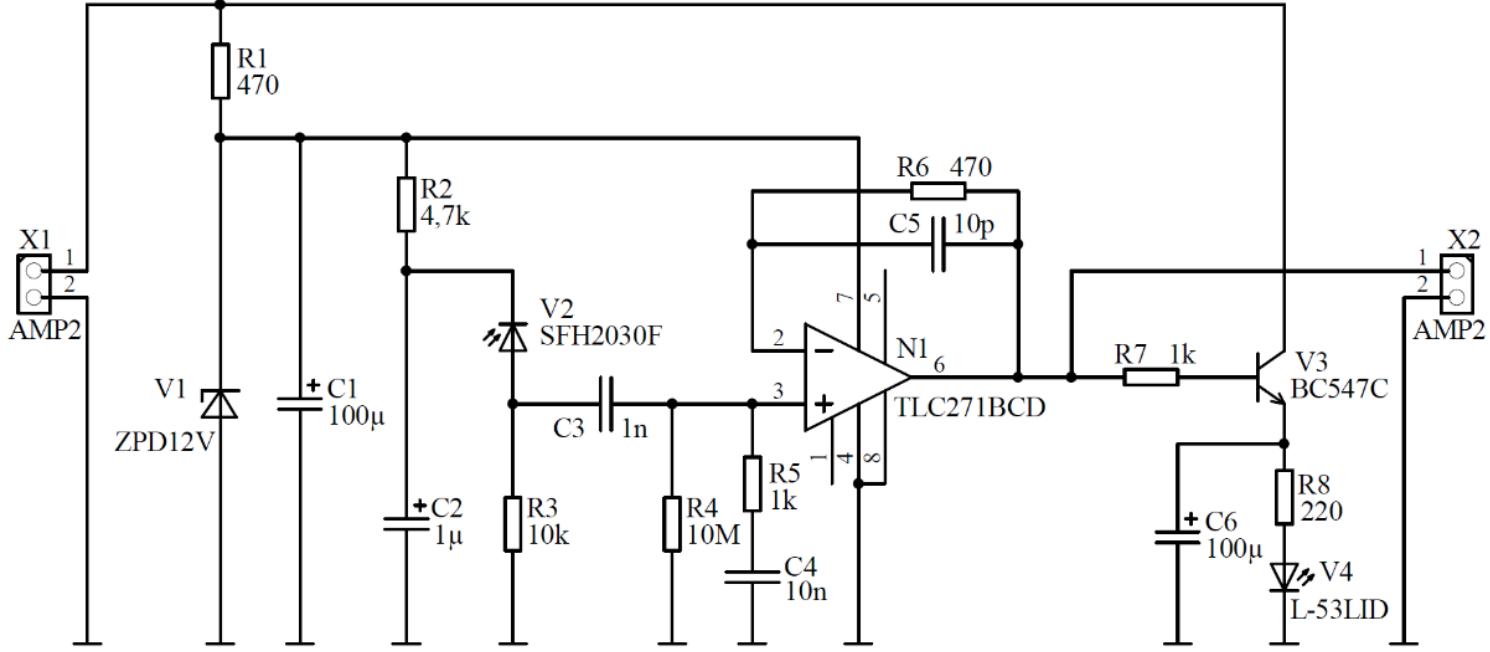


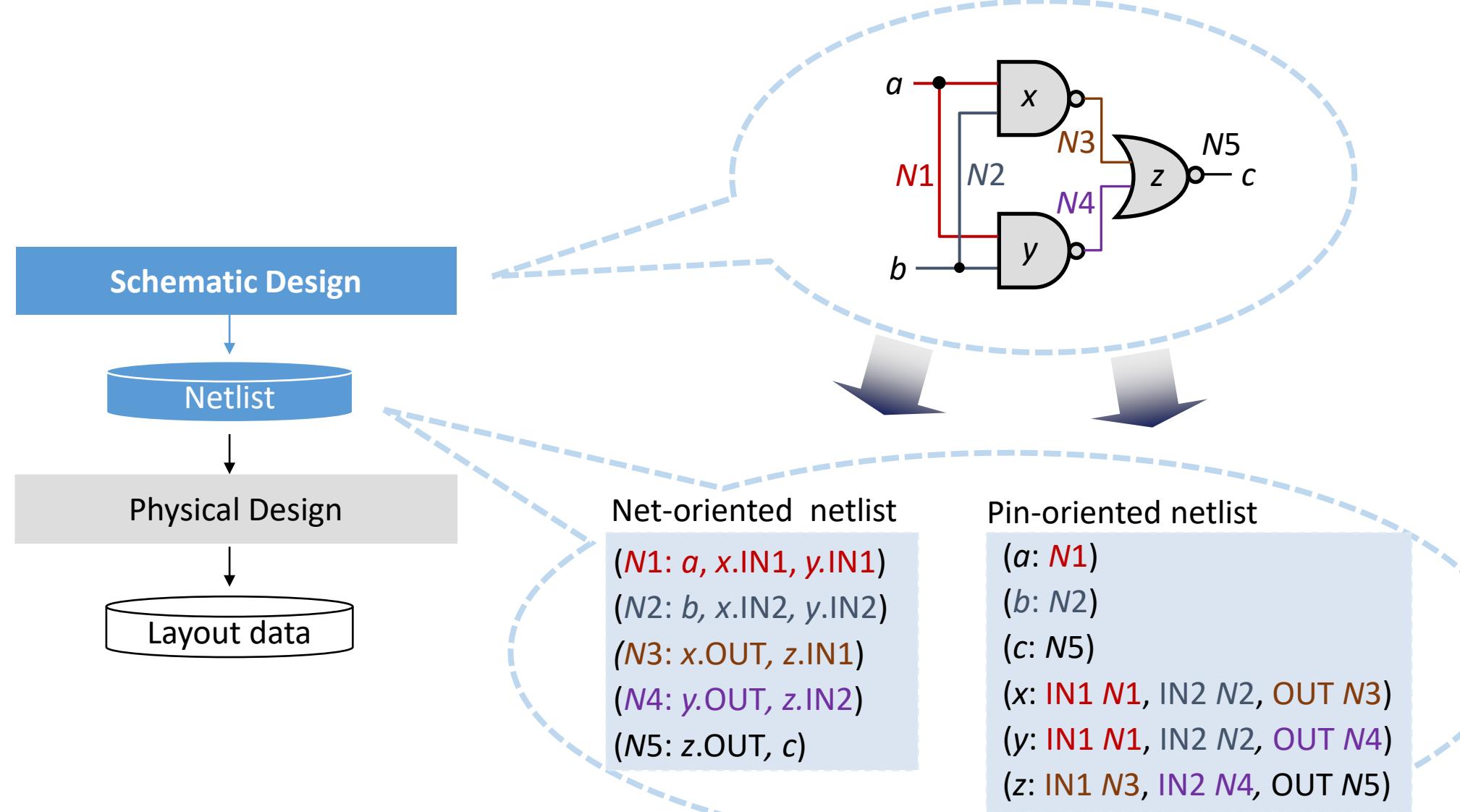
IEEE/IEC symbol	Description	Alternative/distinctive shape
	Primary cell, secondary cell, storage battery The longer line represents the positive pole, the shorter one the negative pole.	
	Ground symbols	
	DC voltage source	
	Resistor	
	Resistor, adjustable	
	Capacitor	
	Inductor, coil, winding, choke (without core)	
	Semiconductor diode; (triangle = anode, bar = cathode)	
	Light emitting diode (LED)	

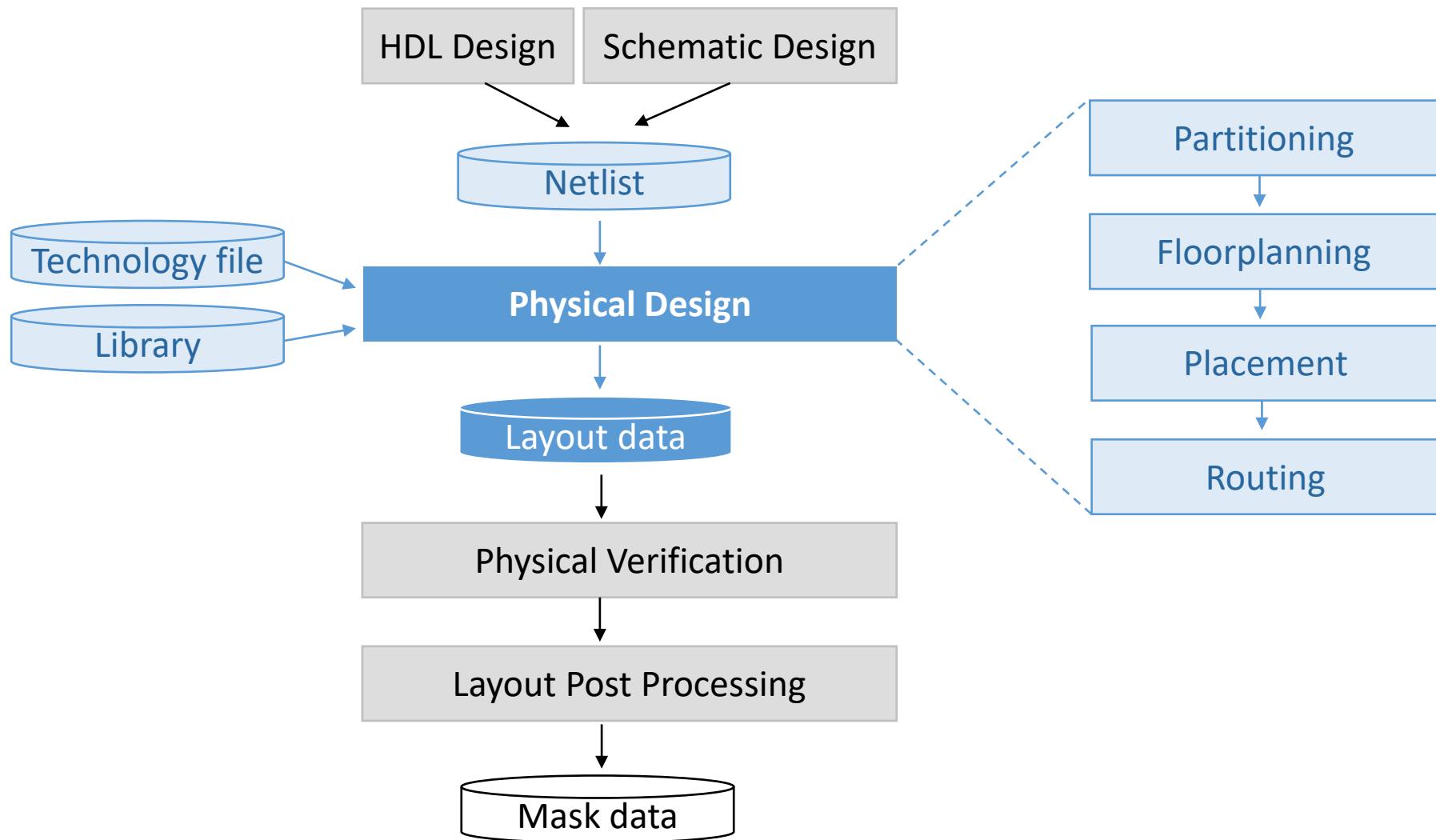
IEEE/IEC symbol	Description	Alternative/distinctive shape
	pnp-transistor	
	n-channel p-channel Junction FET	
	n-channel p-channel Enhancement MOSFET	
	n-channel p-channel (n-MOS) (p-MOS) Enhancement MOSFET (digital representation)	
	n-channel p-channel Depletion MOSFET	
	Photo transistor (n-pn model)	

IEEE/IEC symbol	Description	Alternative/distinctive shape
	Inverter	
	AND gate	
	NAND (AND with negated output)	
	OR gate	
	NOR (OR with negated output)	
	D-Flipflop	
	Operational amplifier	



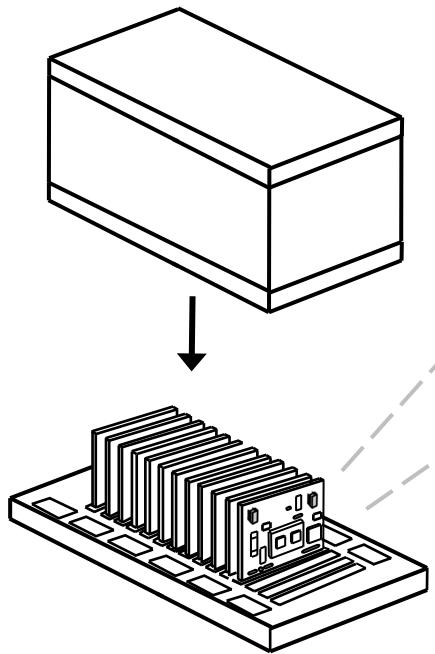






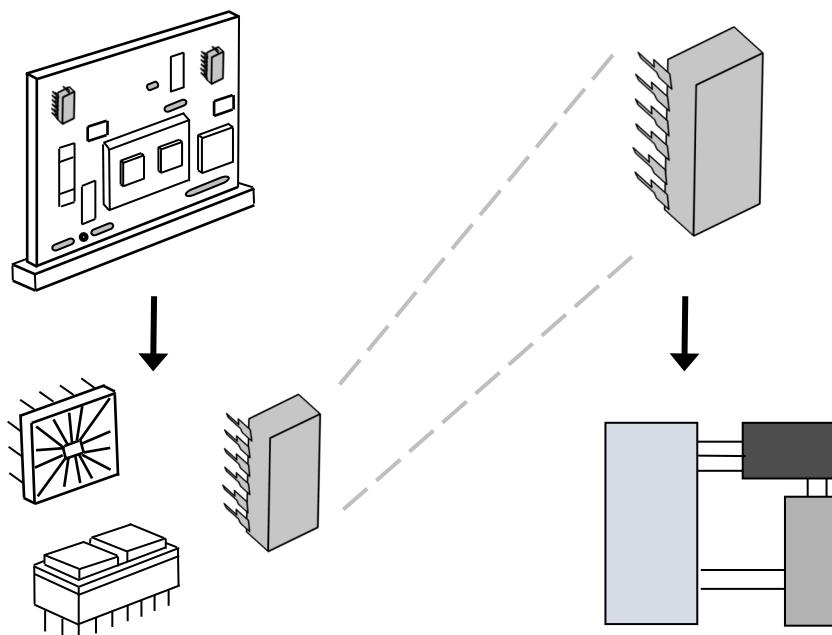
### **System level**

Each subsystem (PCB) can be designed and manufactured independently



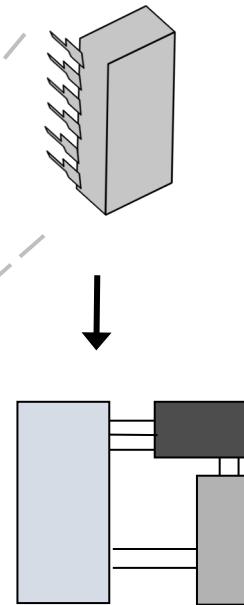
### **Board level**

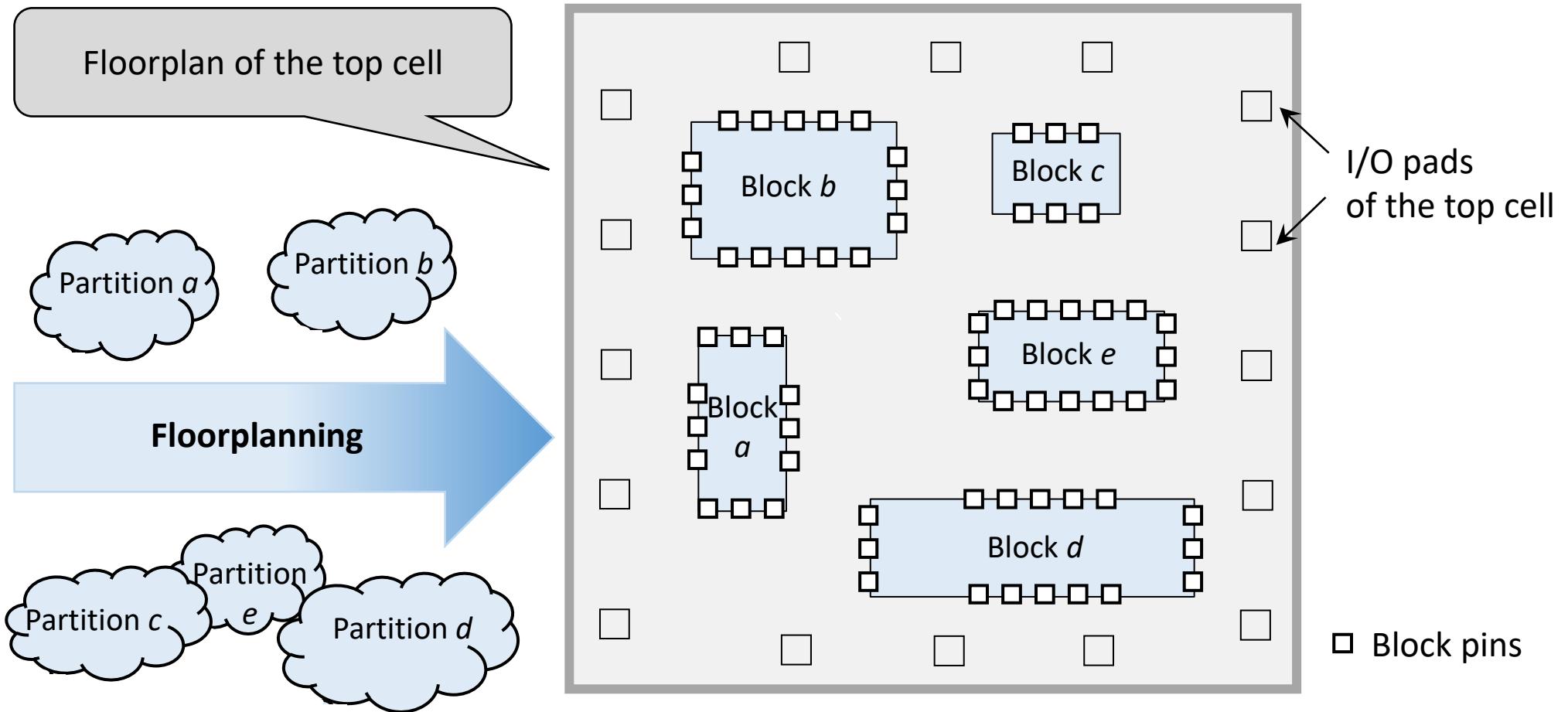
Determining subcircuits that can be realized as separate units (ICs, MCMs)

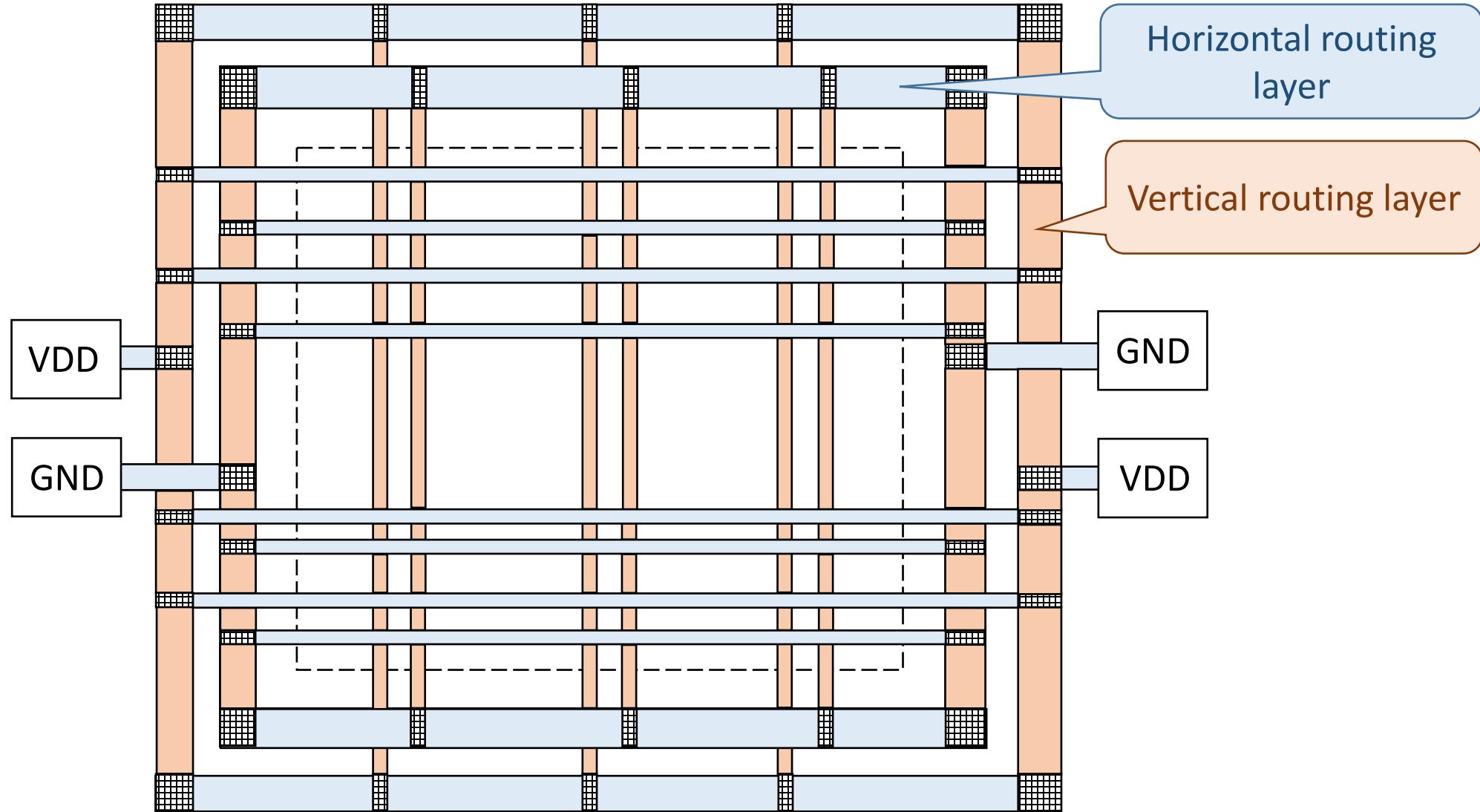


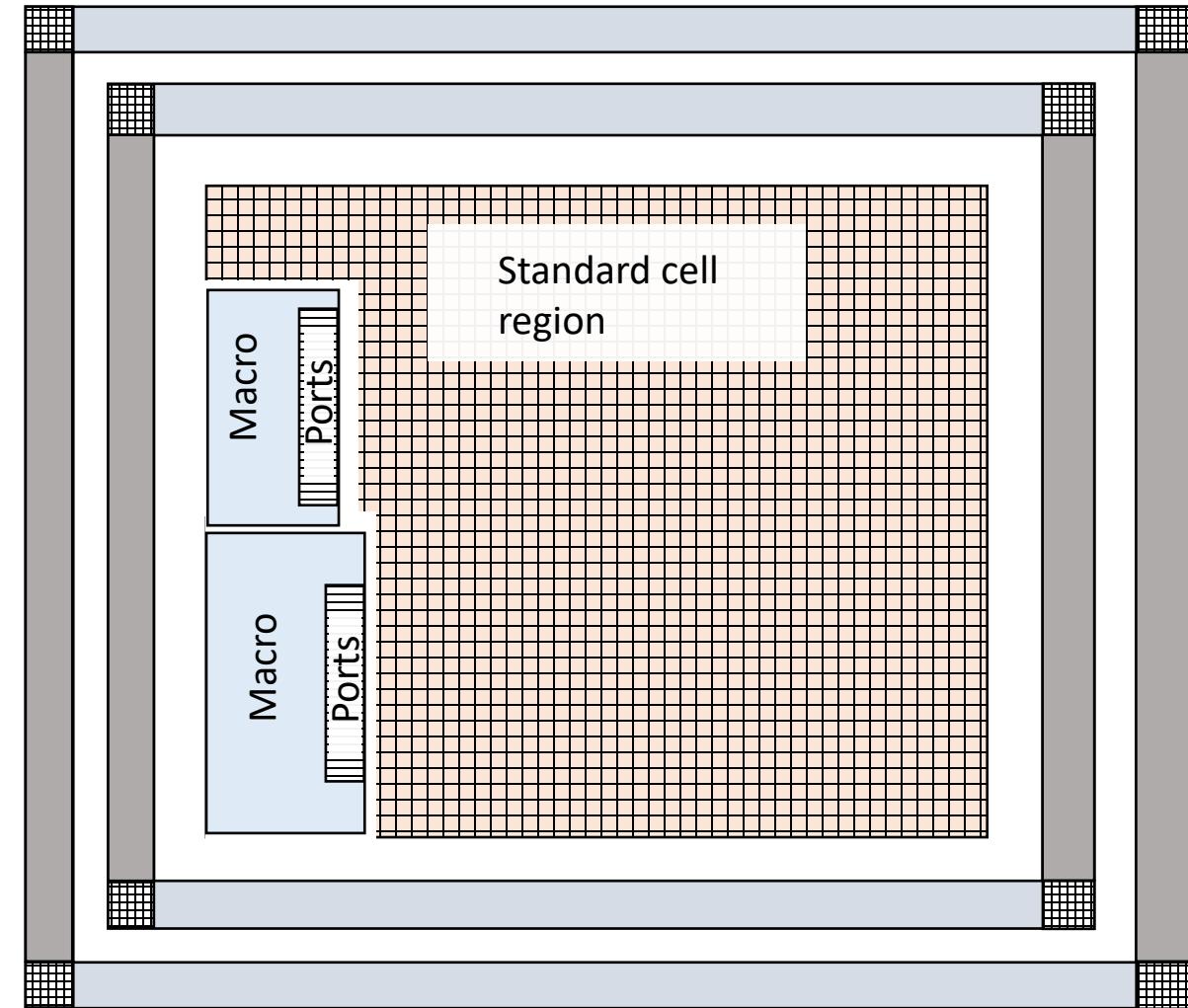
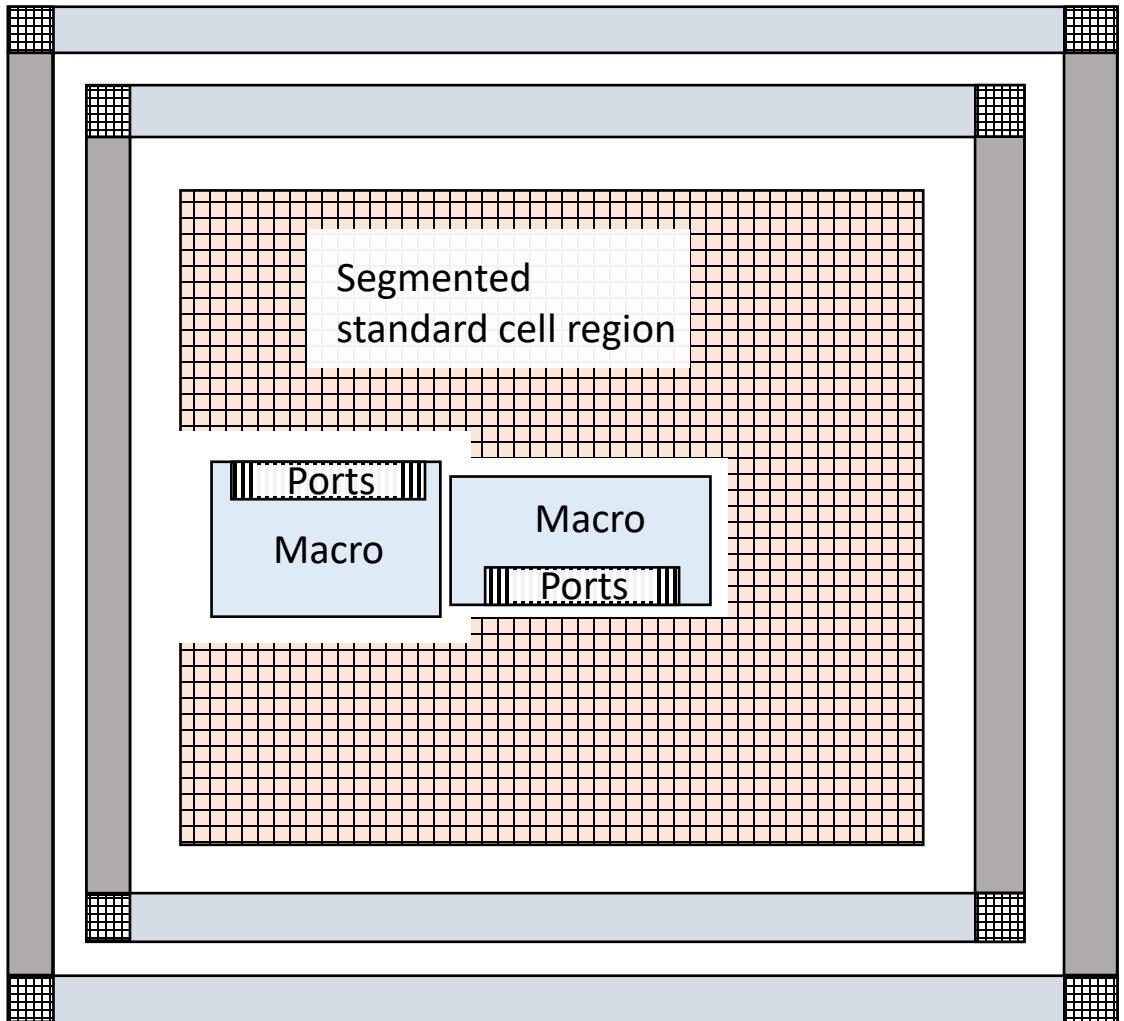
### **Chip level**

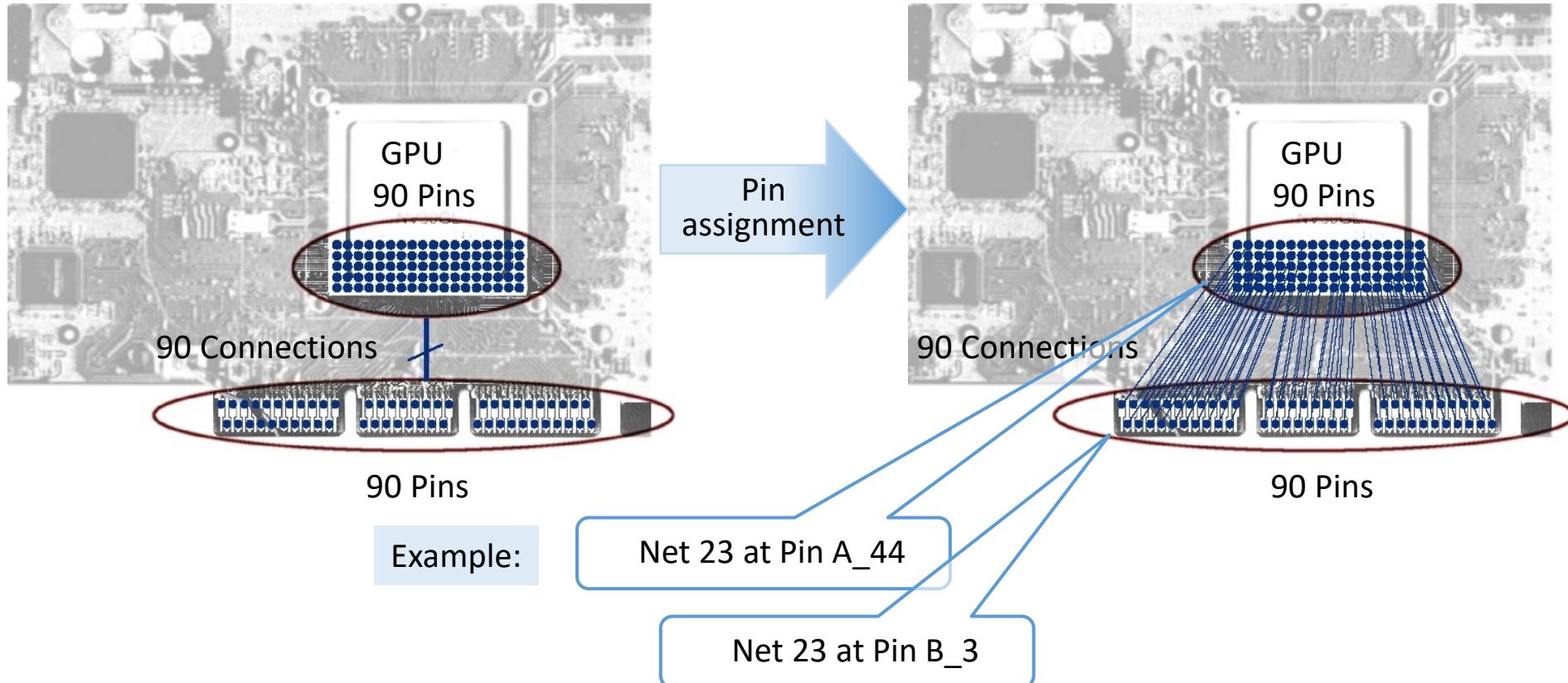
ICs are partitioned into smaller blocks that can be designed independently for the purpose of reducing complexity

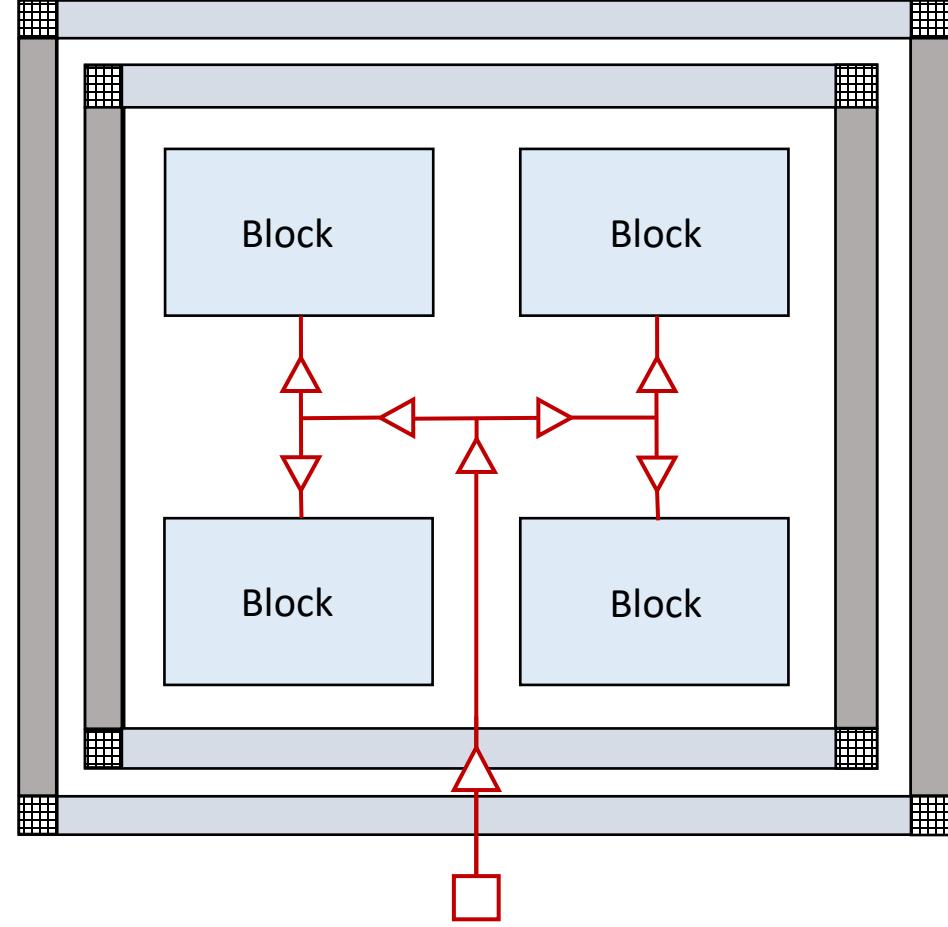
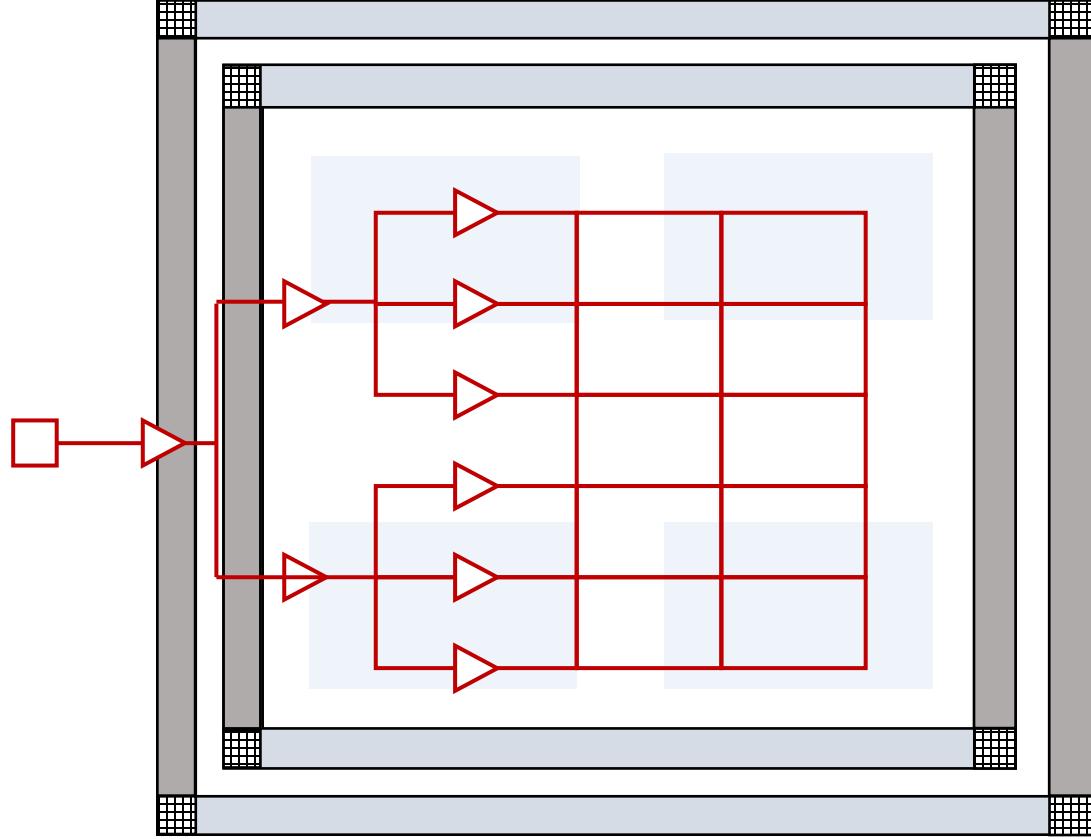


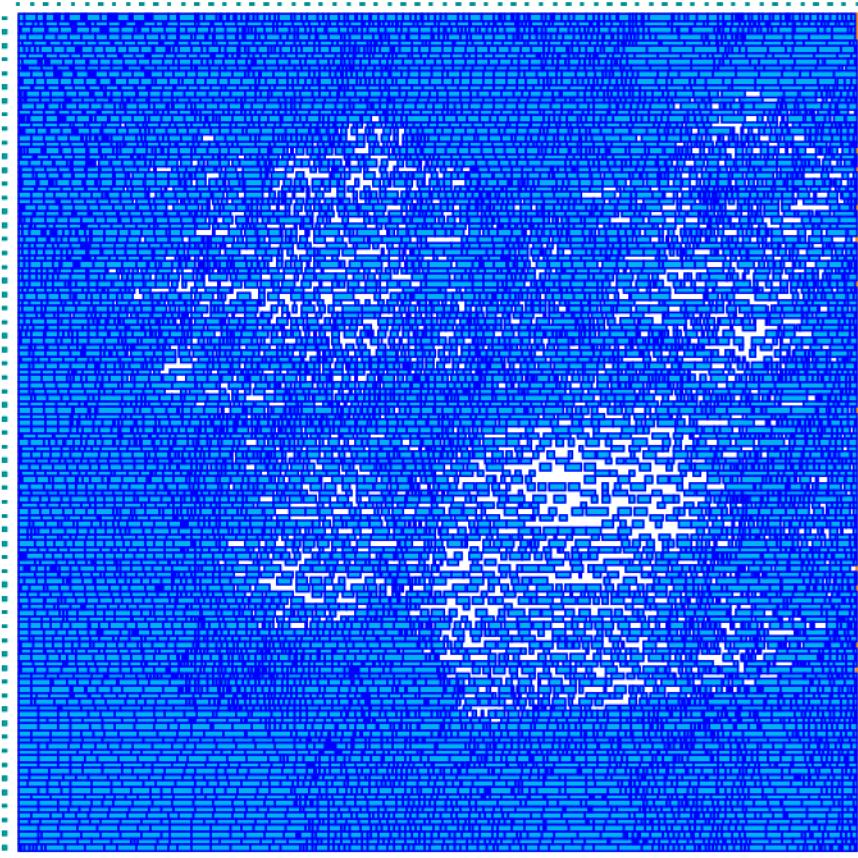
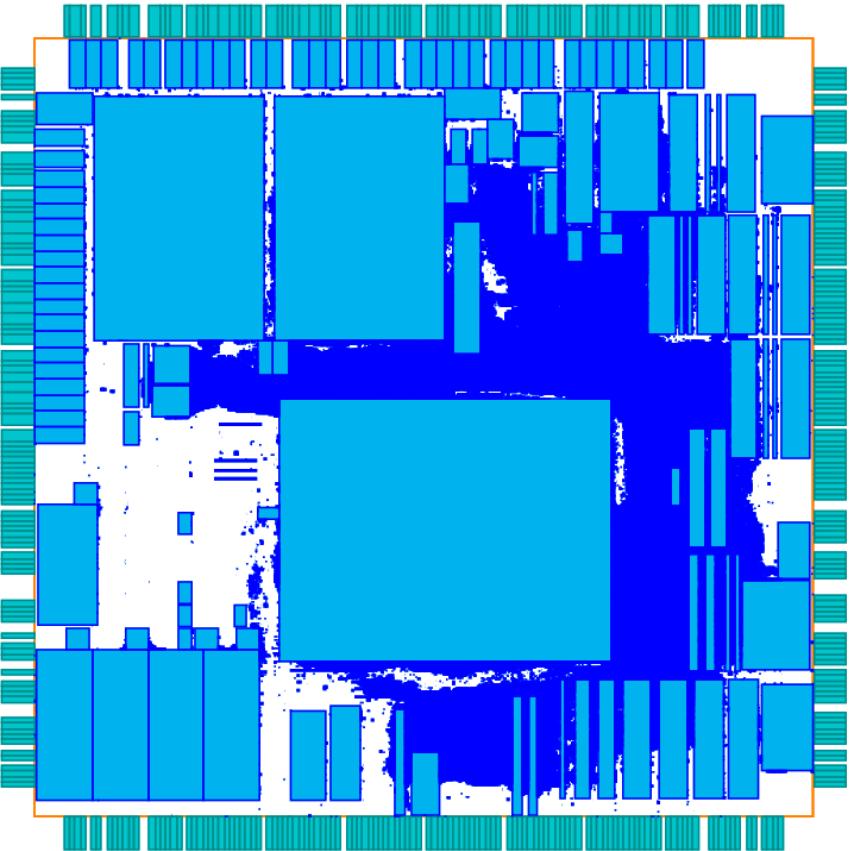


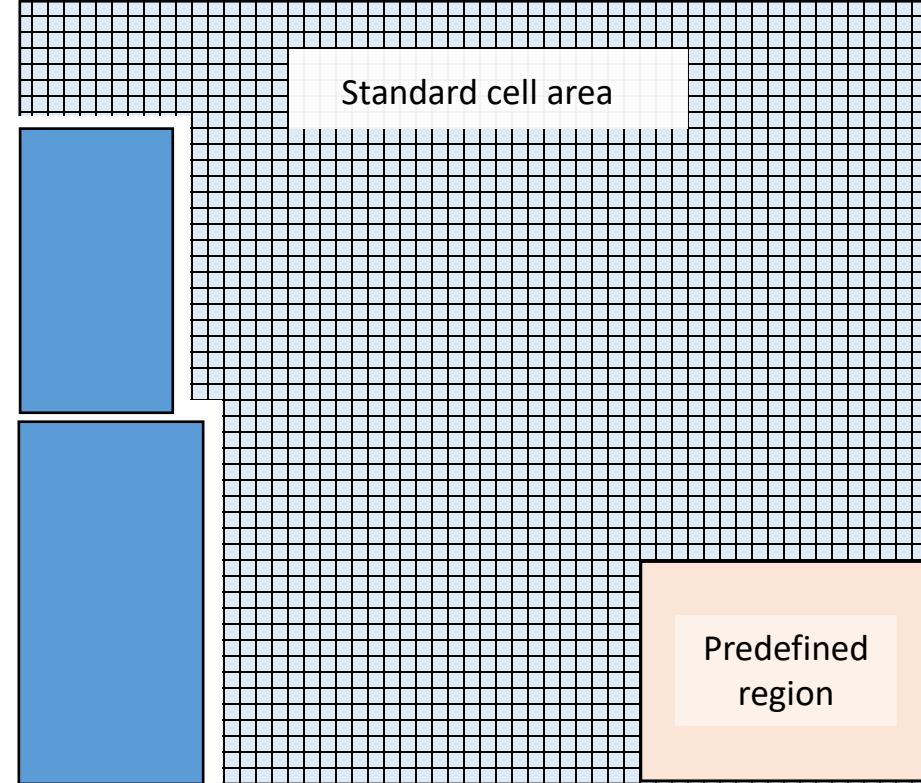
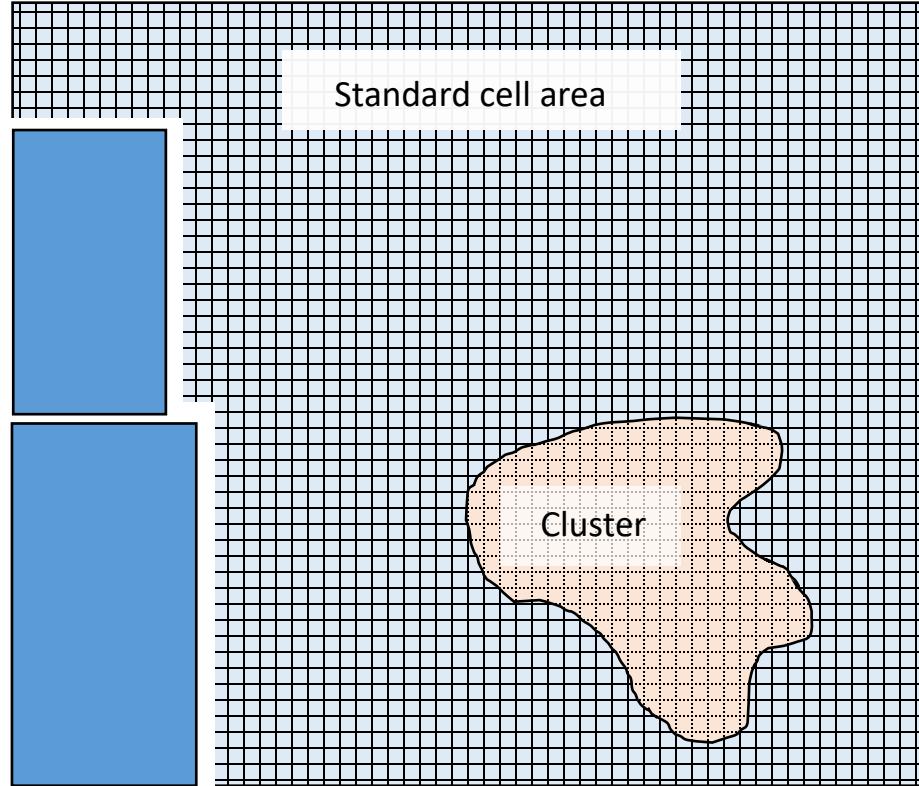


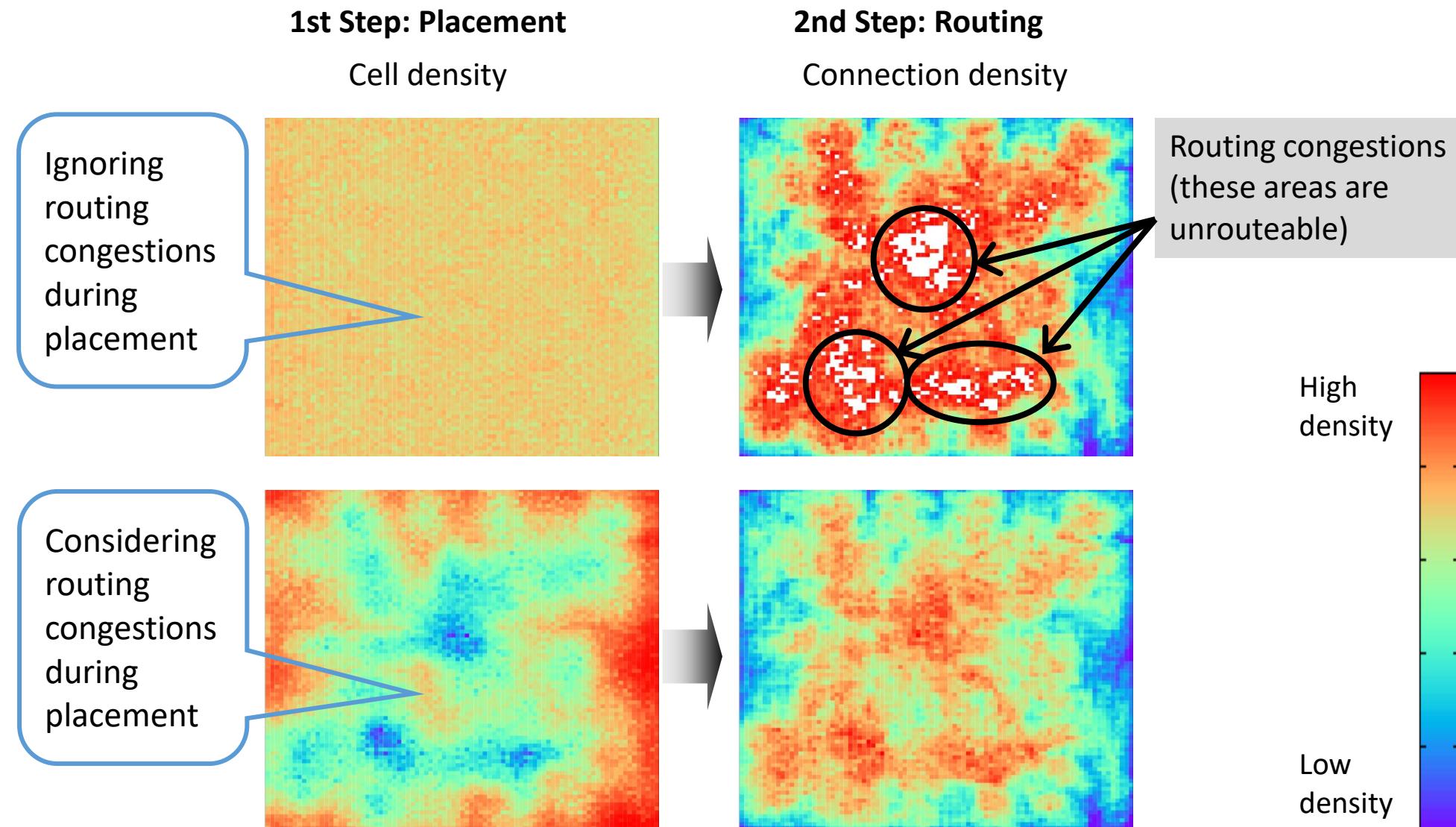


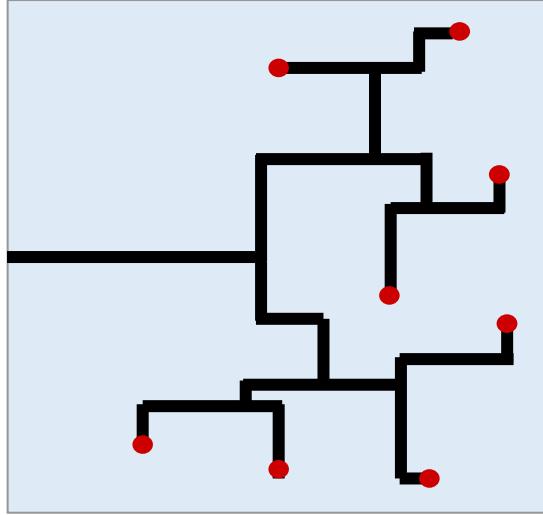




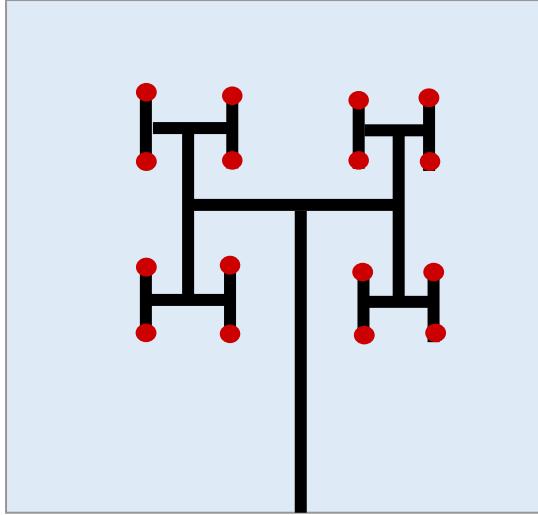




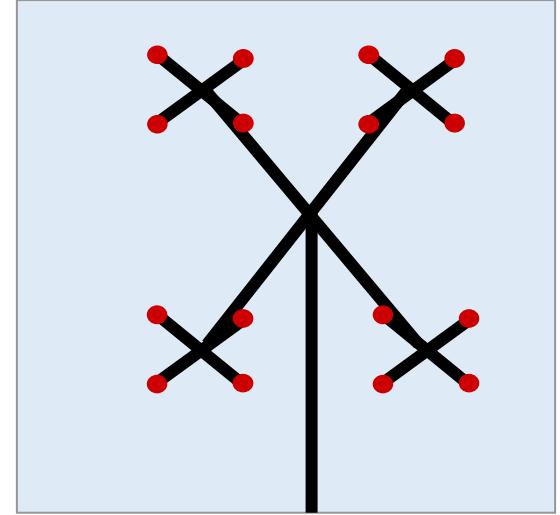




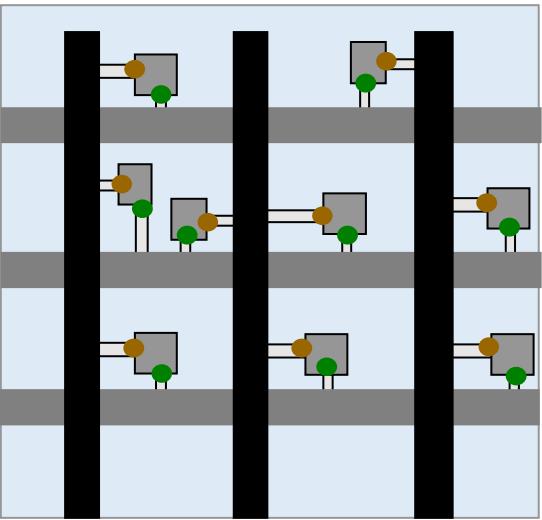
Balanced tree



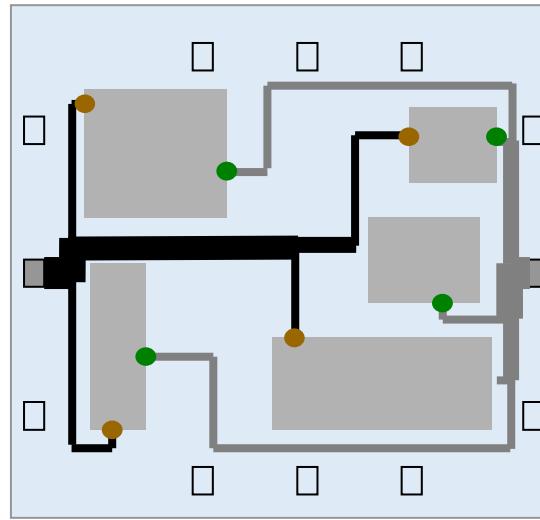
H tree



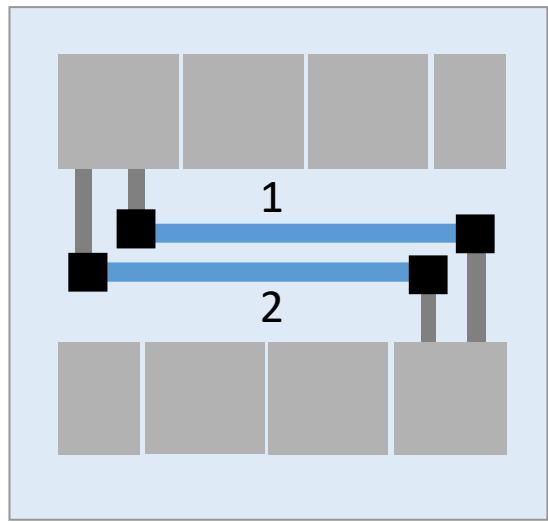
X tree



Power mesh

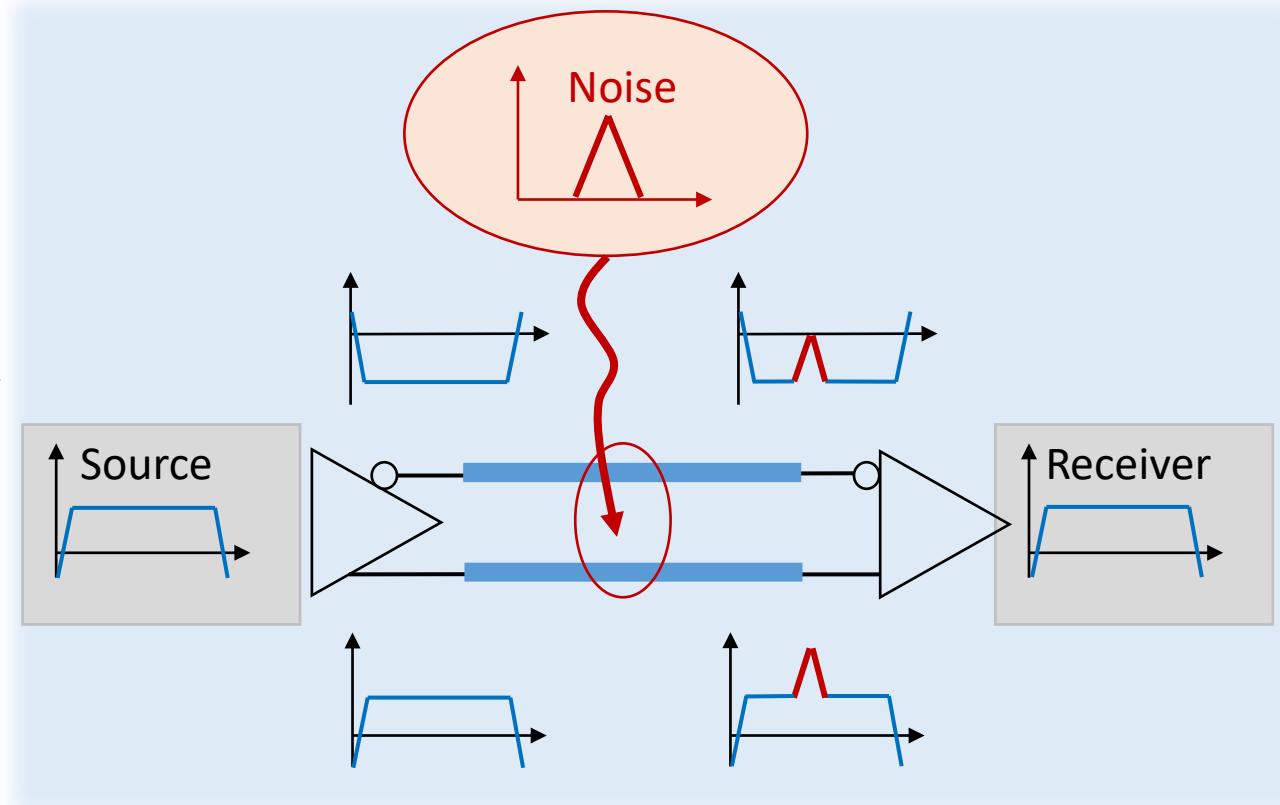


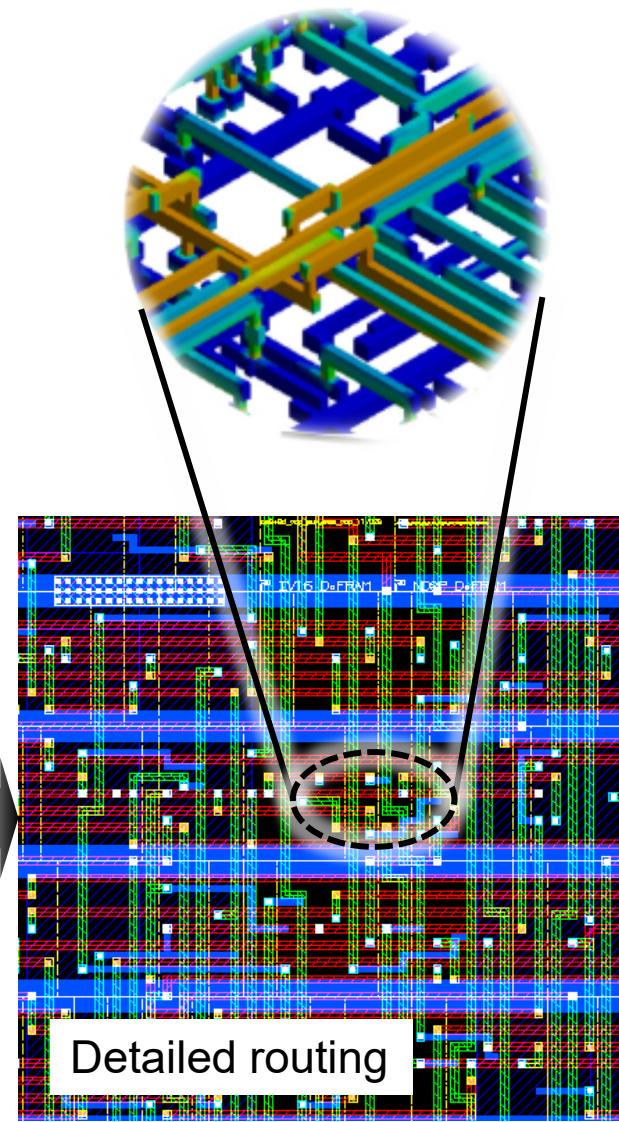
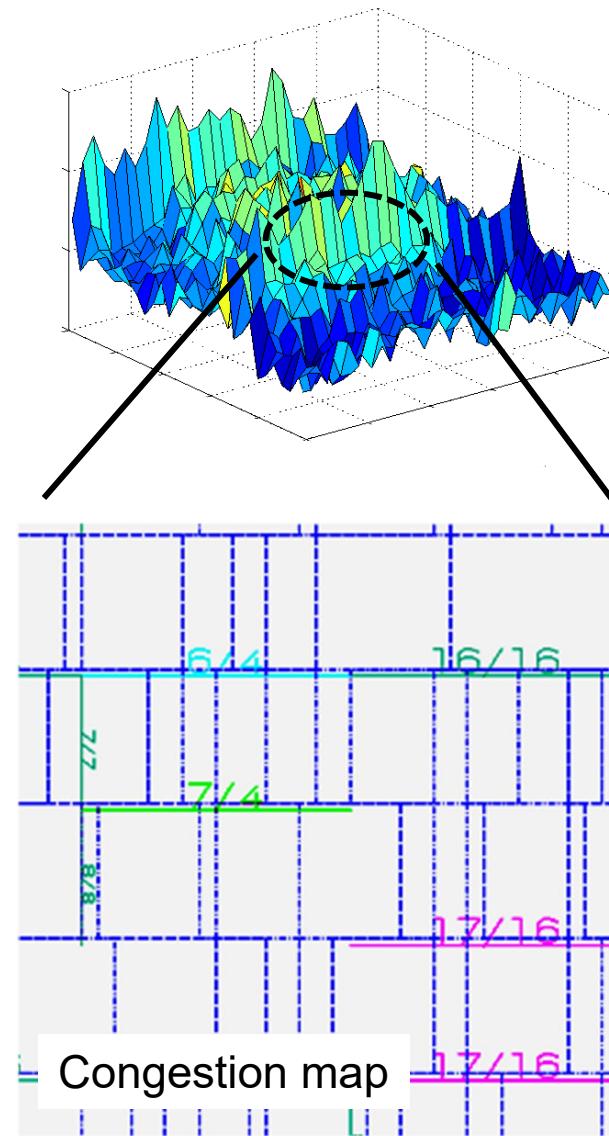
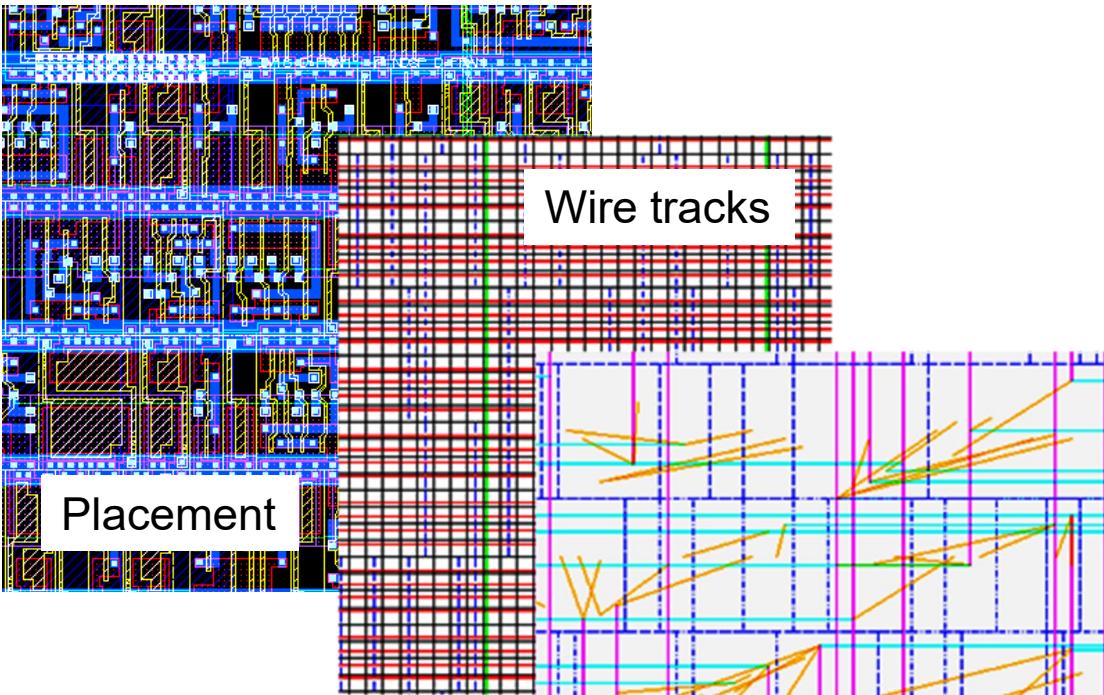
Power tree

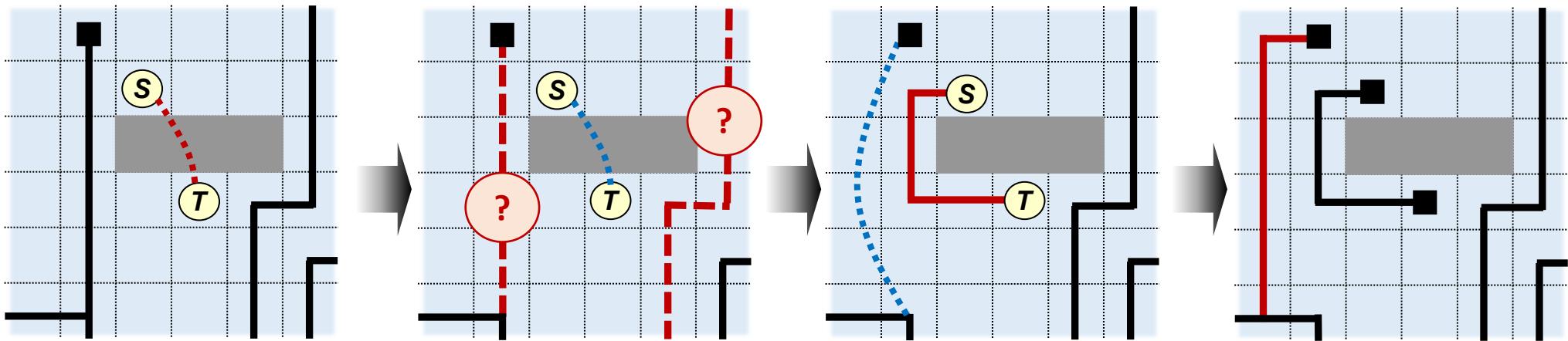


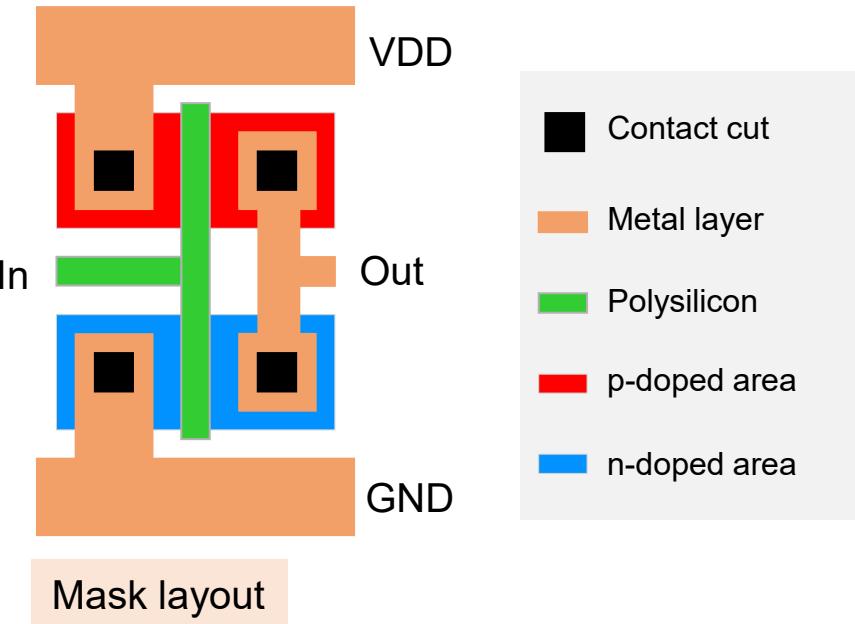
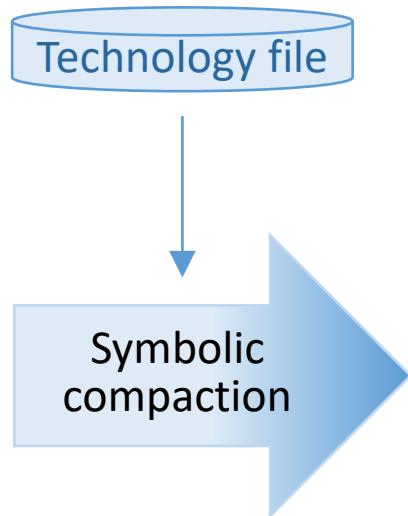
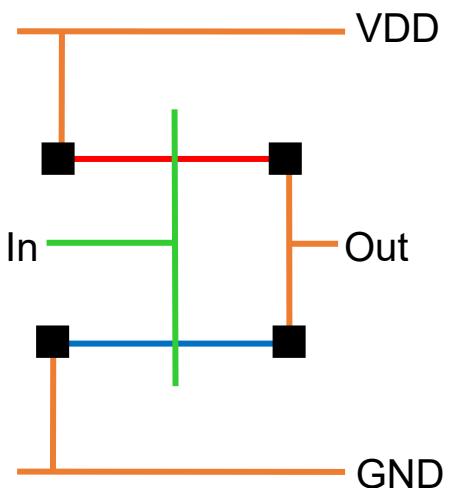
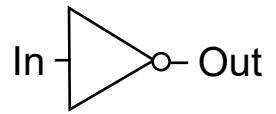
$$(R_1, C_1) = (R_2, C_2)$$

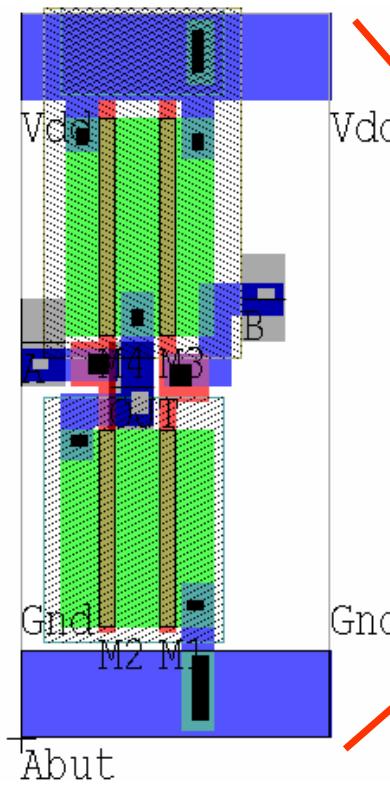
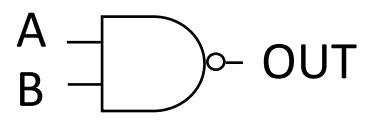
Differential  
signaling







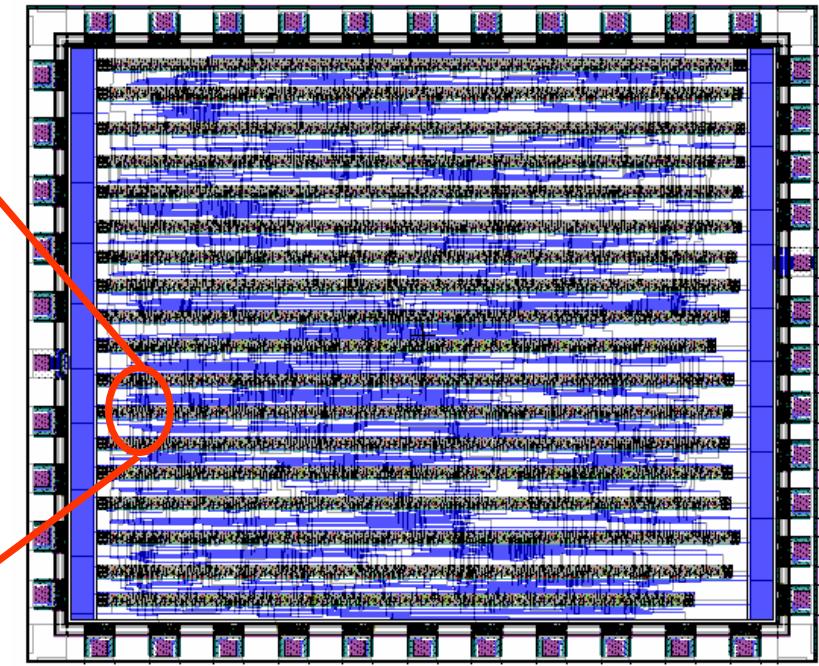
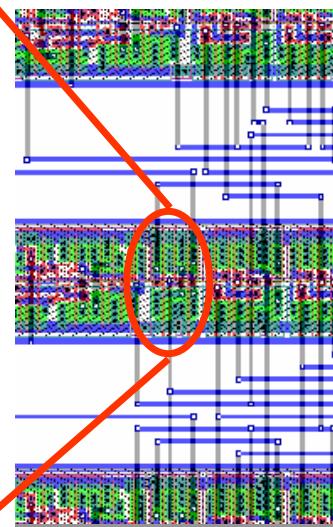


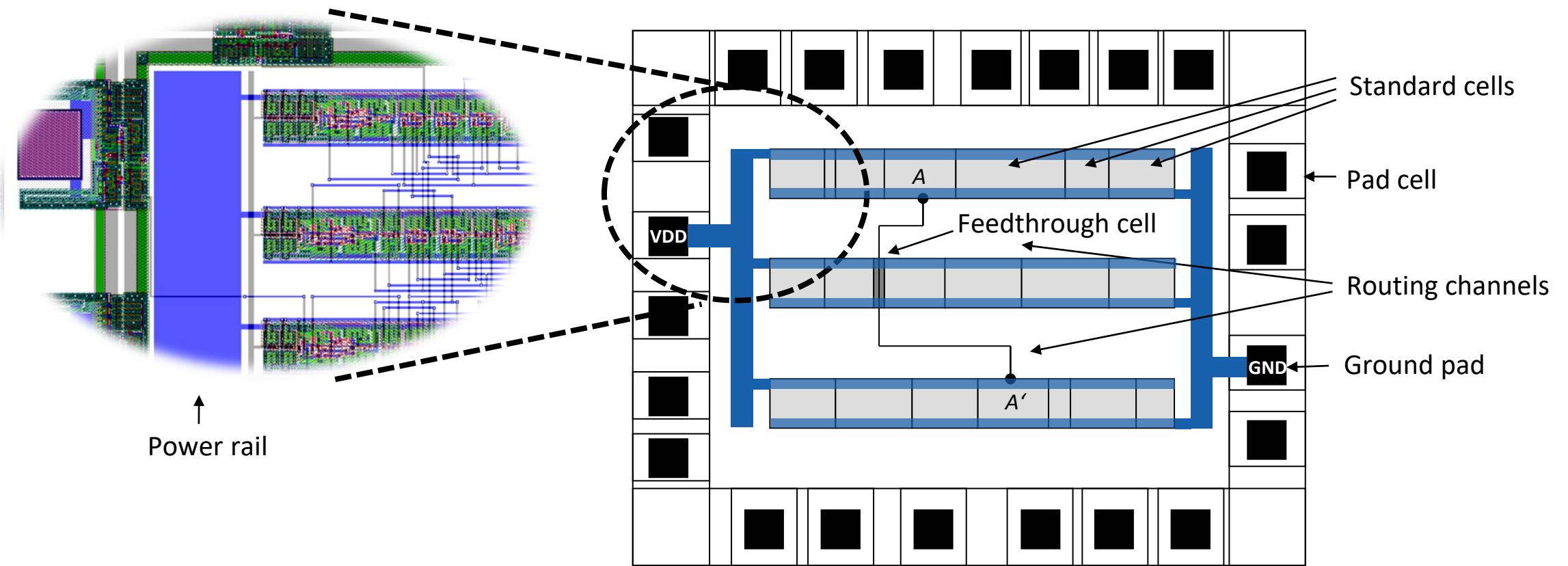


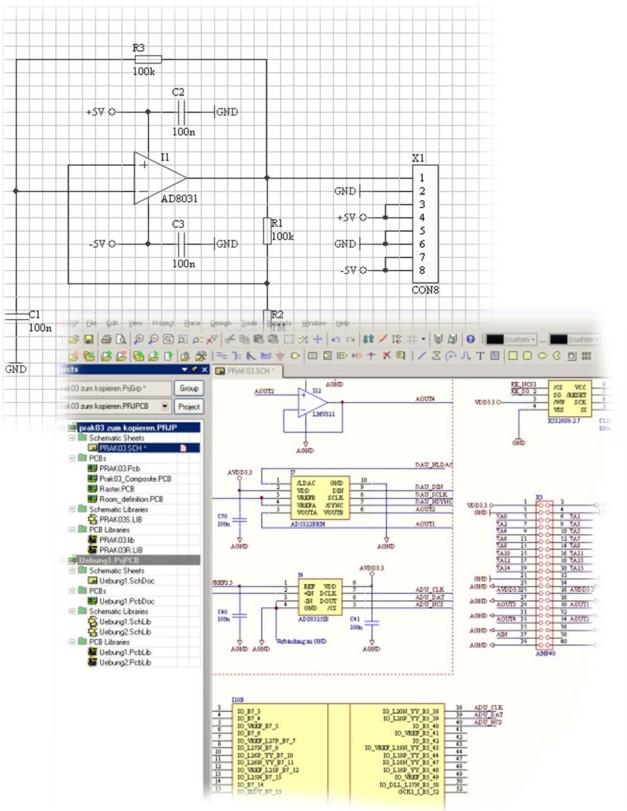
Vdd

Gnd

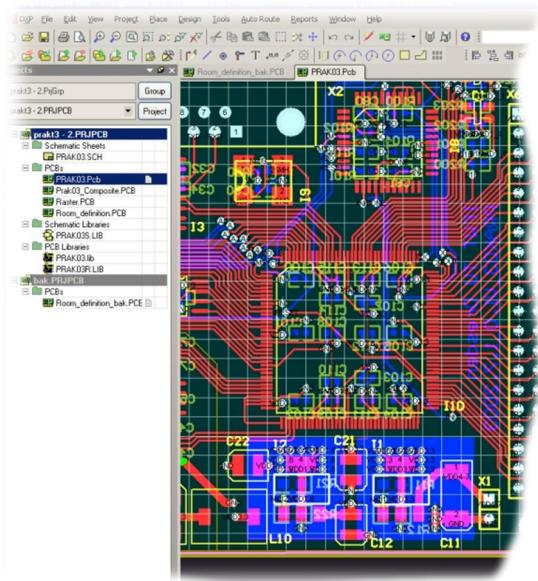
Abut



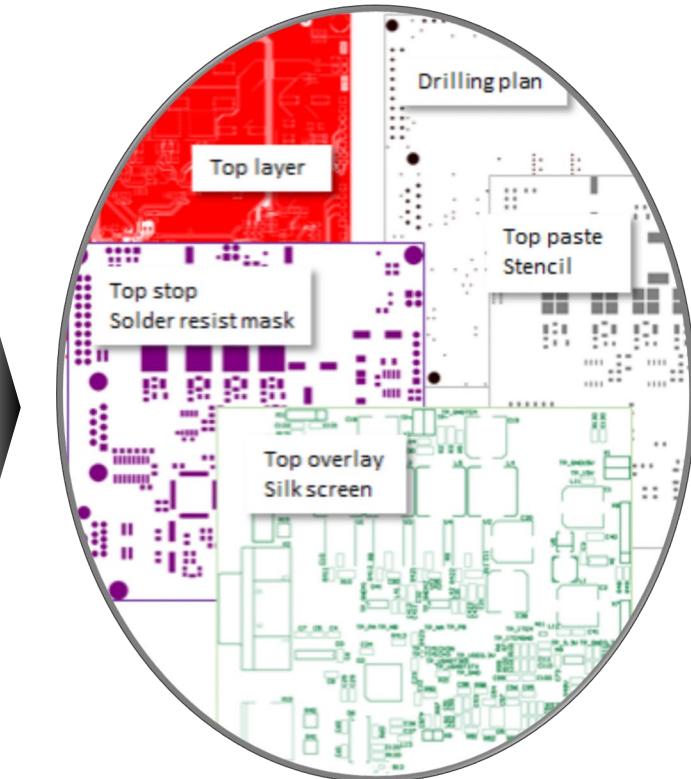




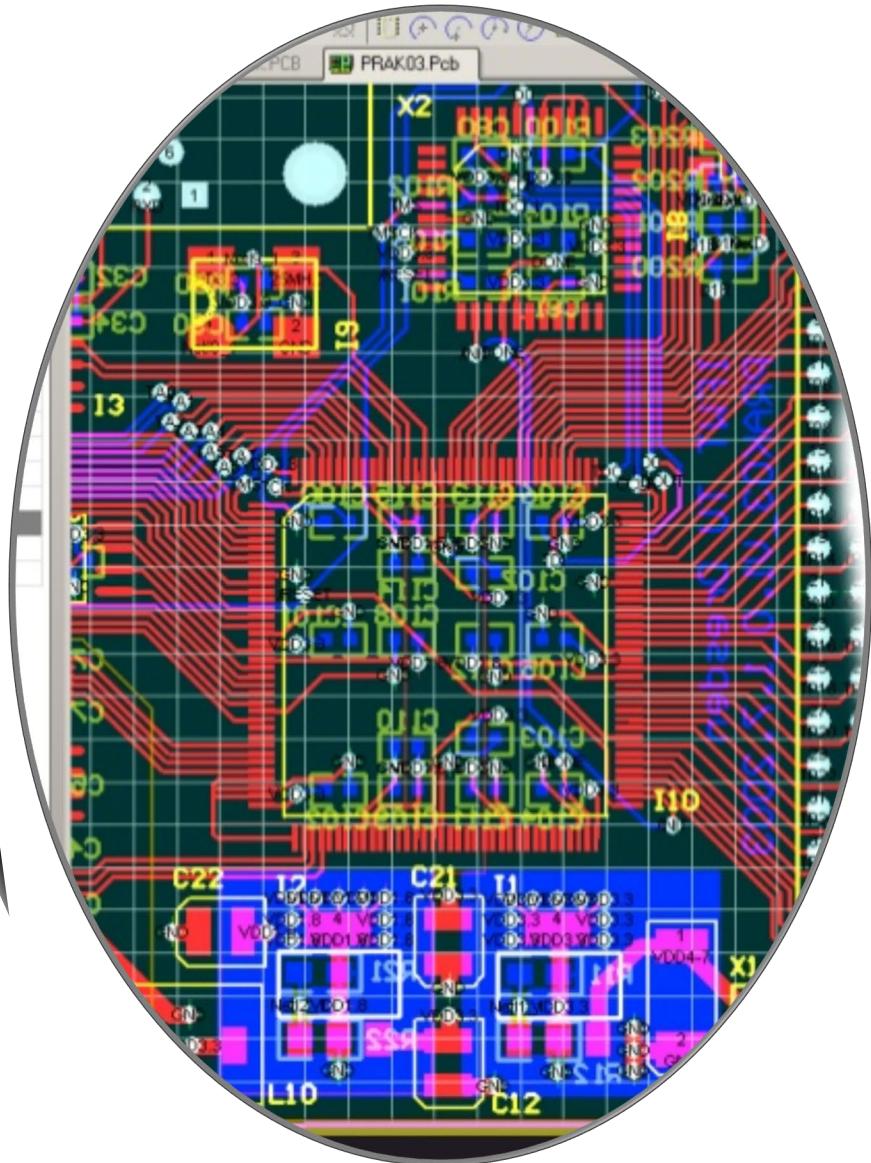
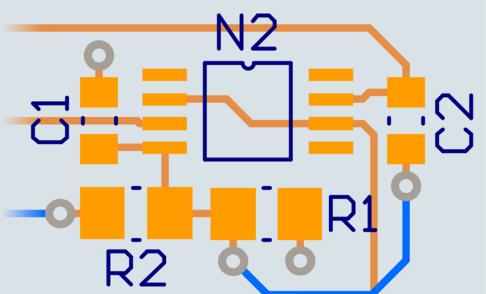
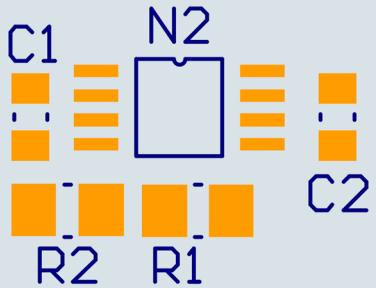
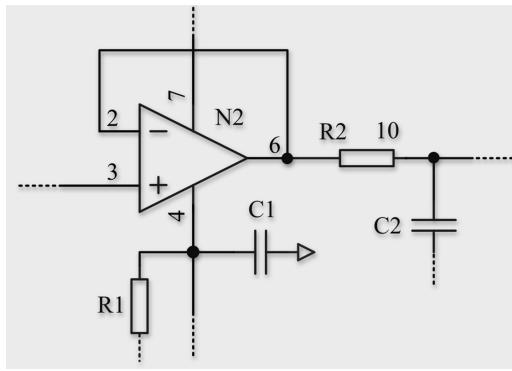
Schematic entry



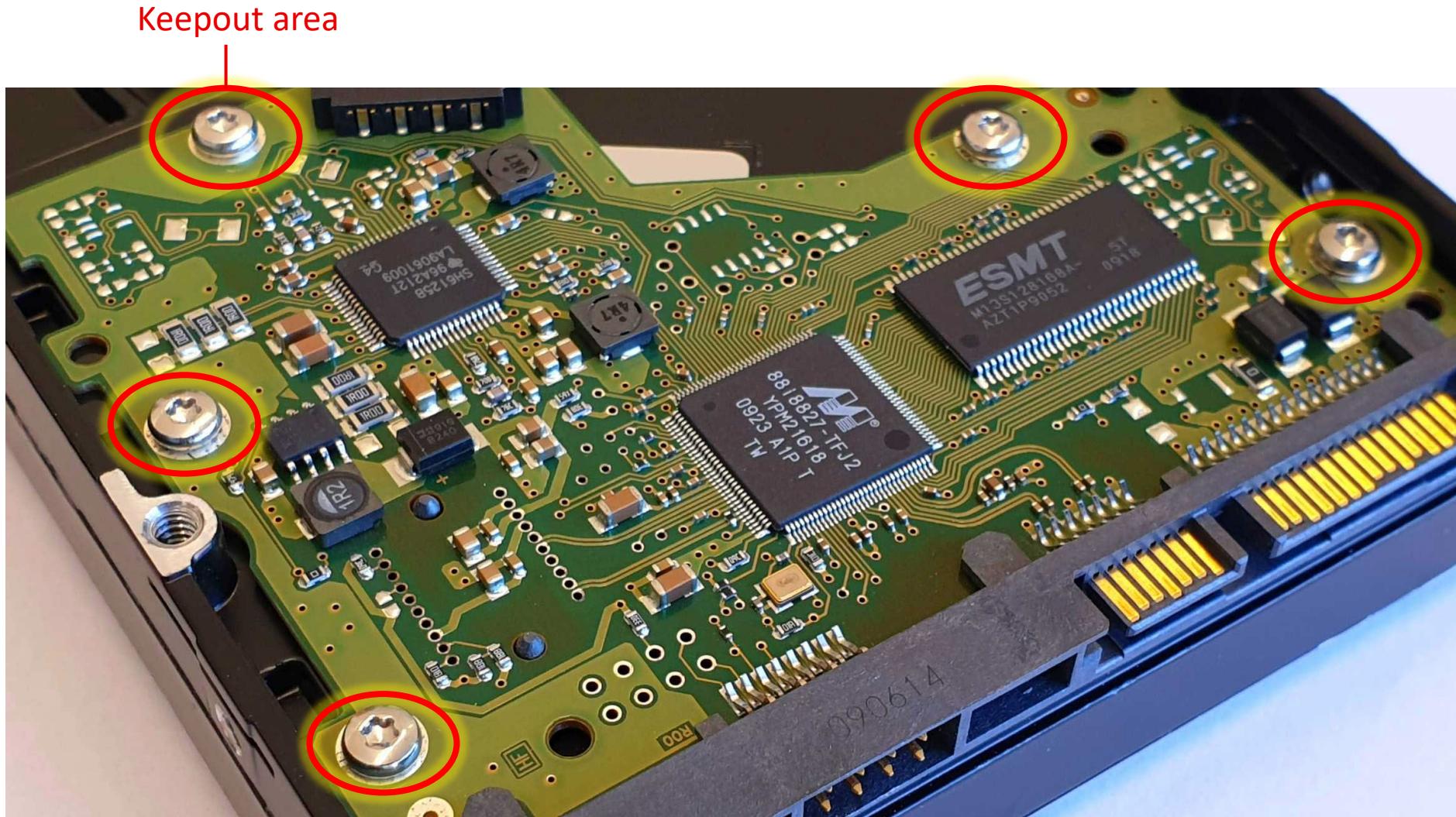
PCB layout generation

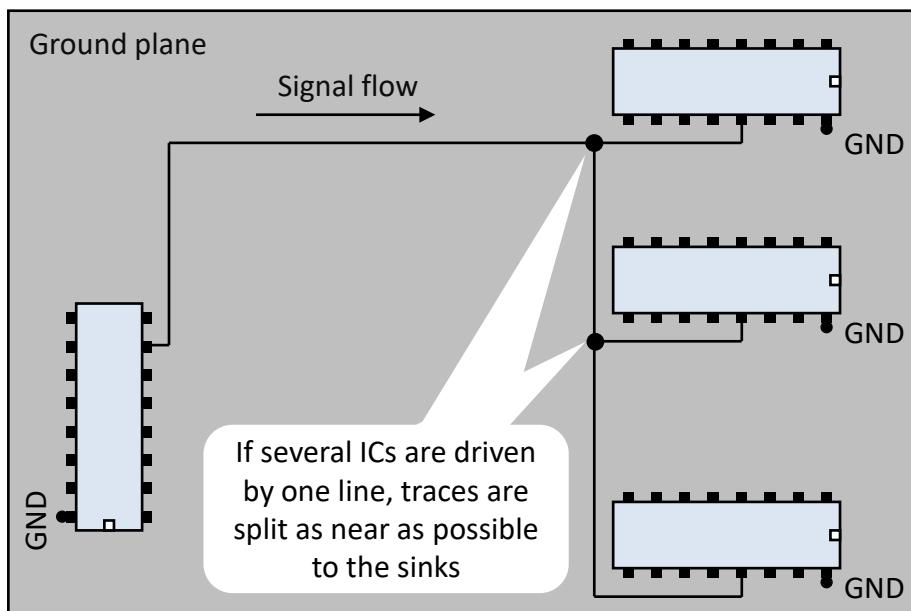
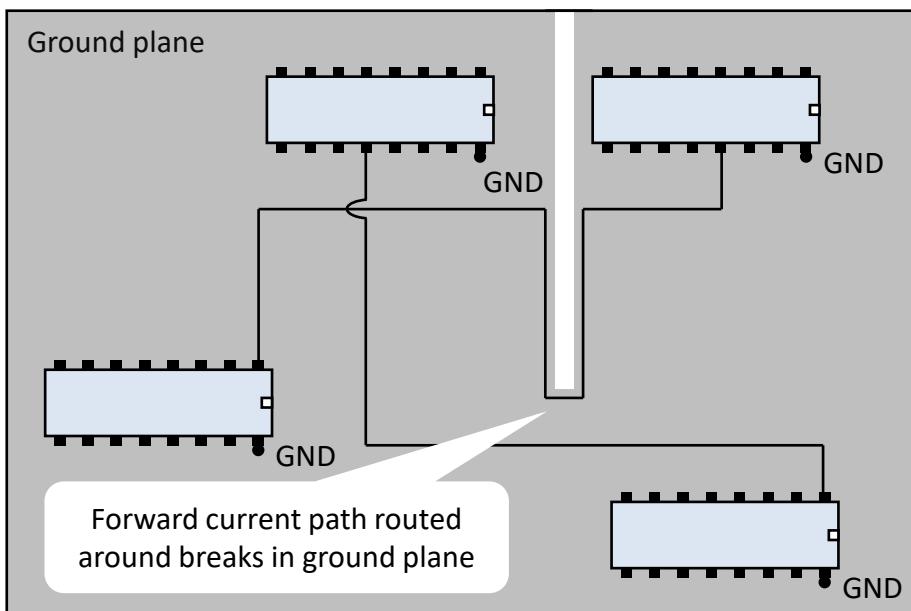
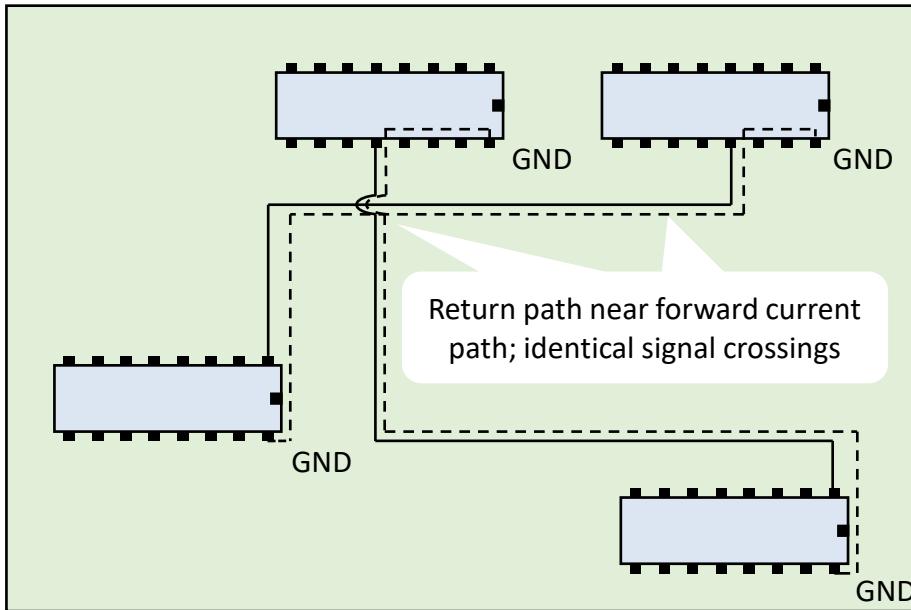
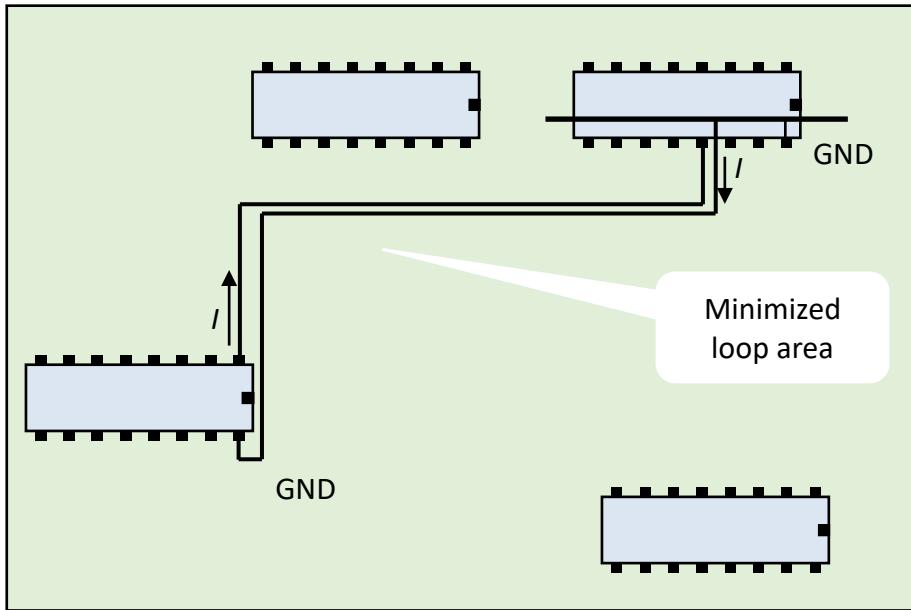


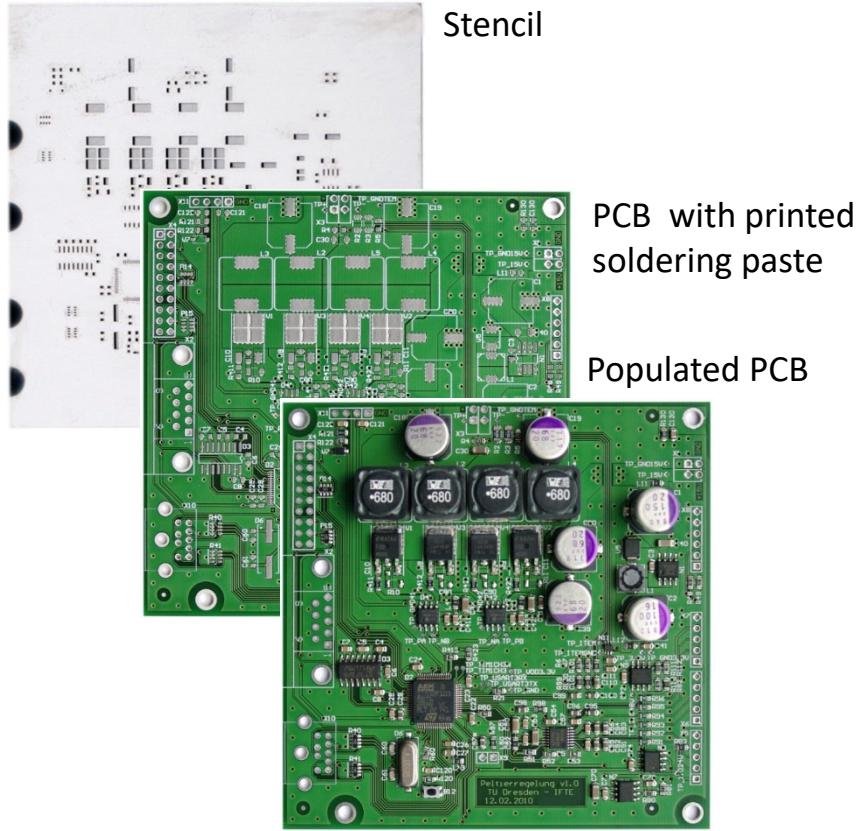
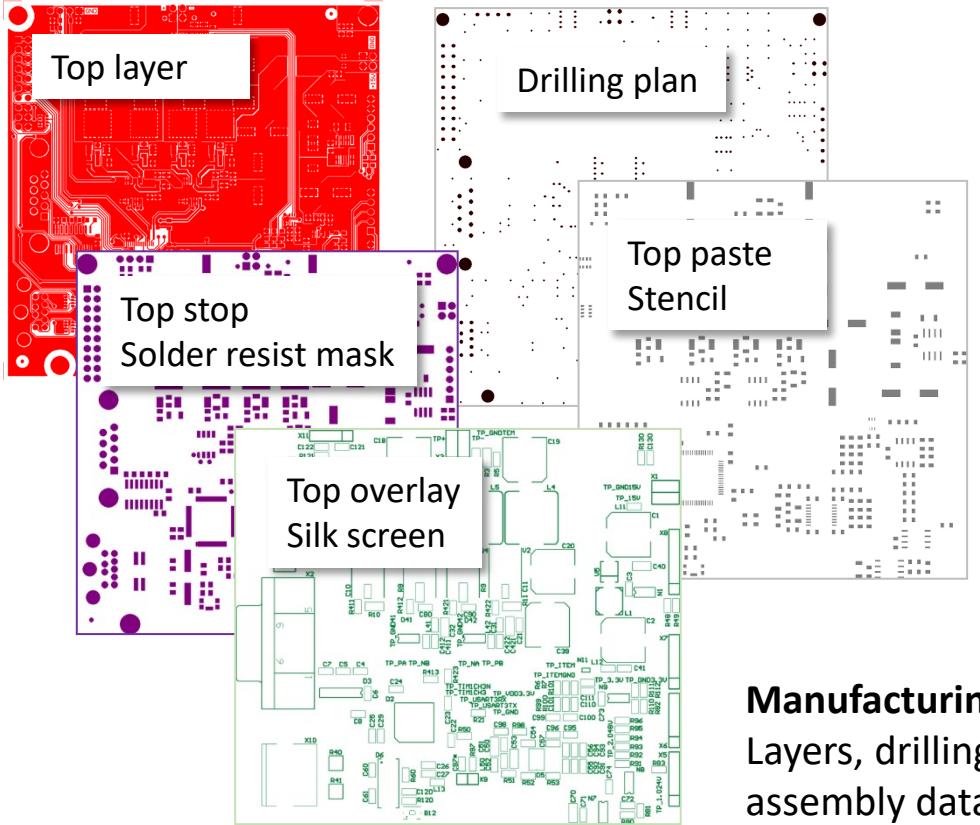
Manufacturing documentation

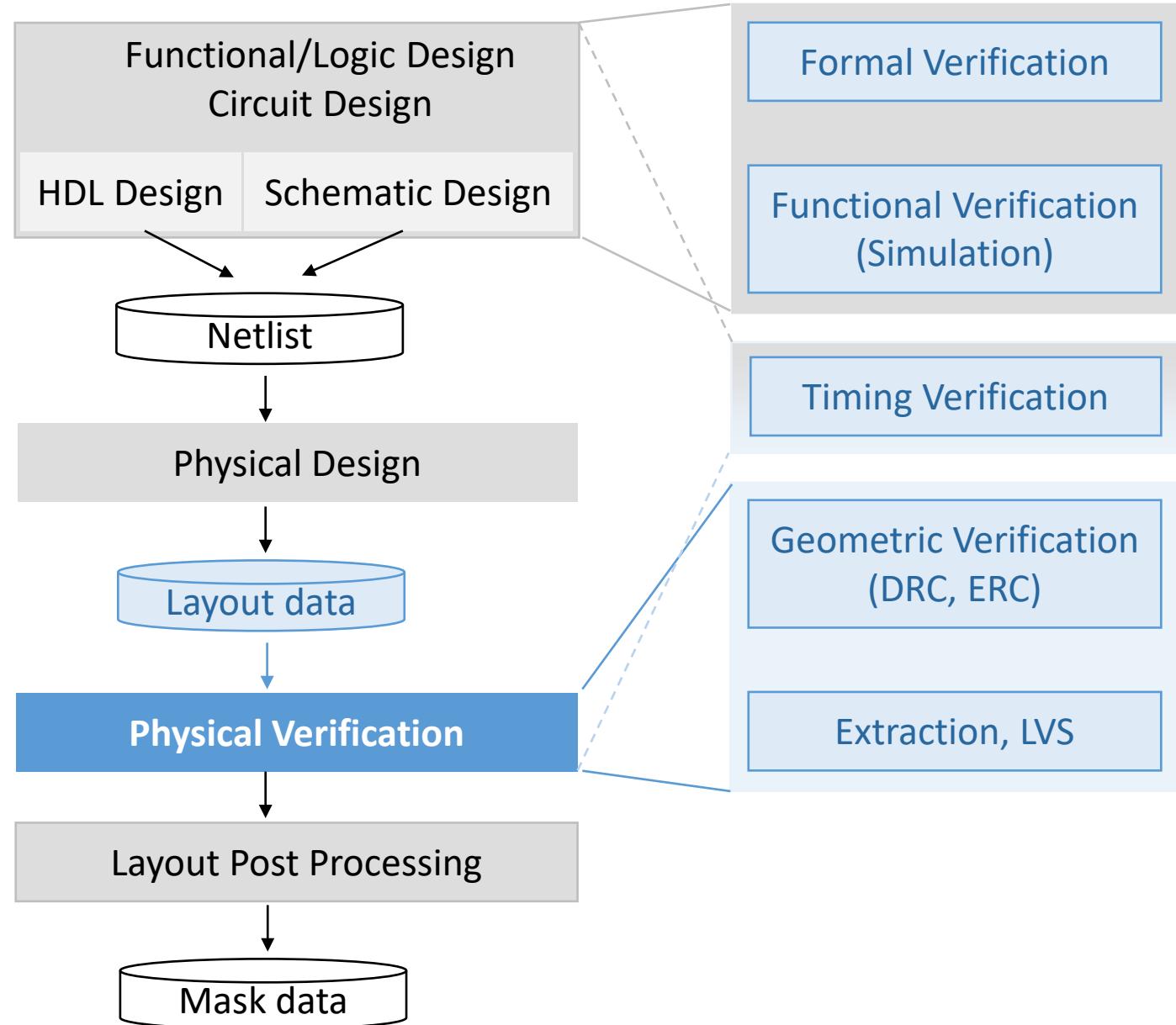


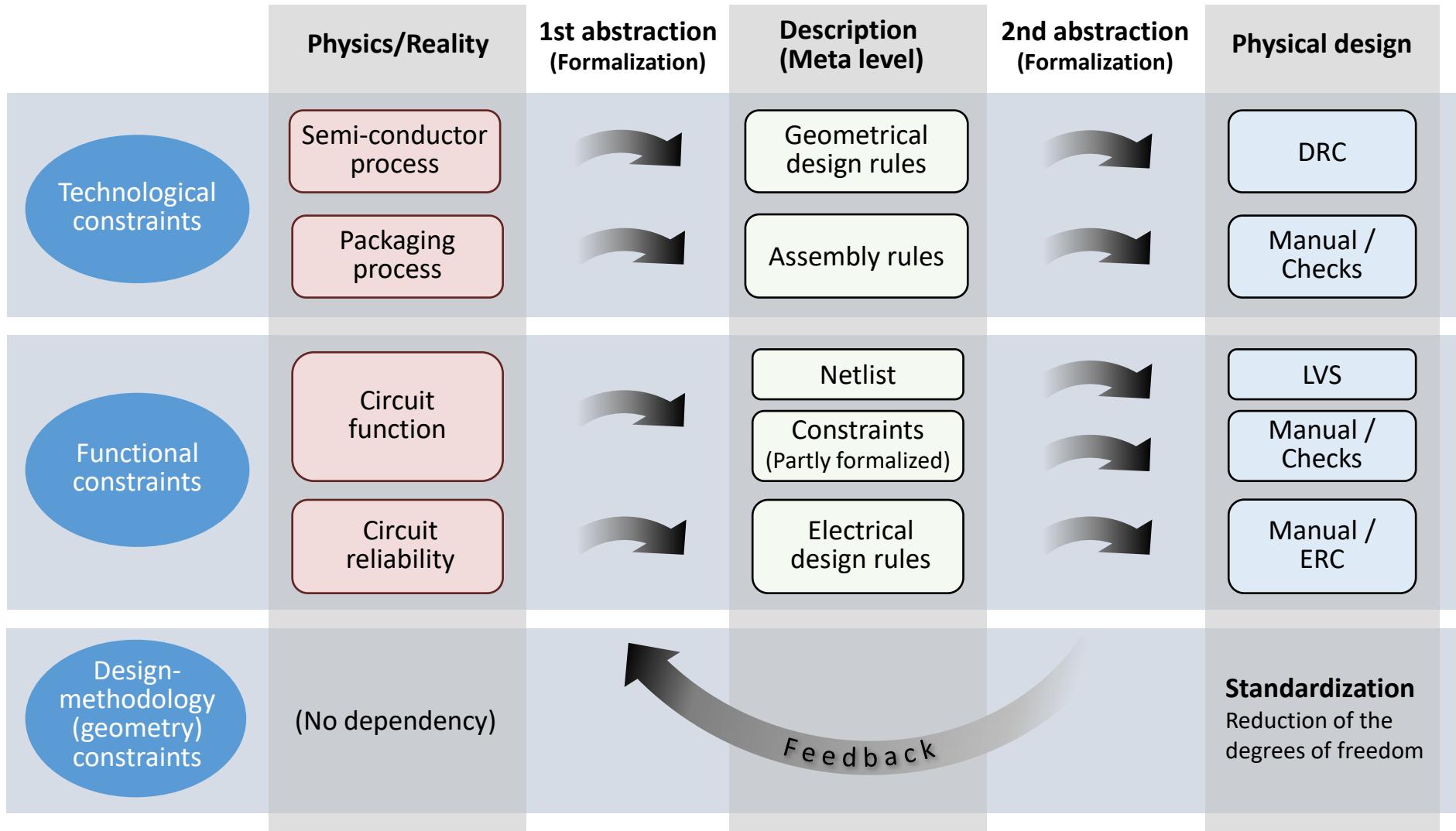
PCB layout



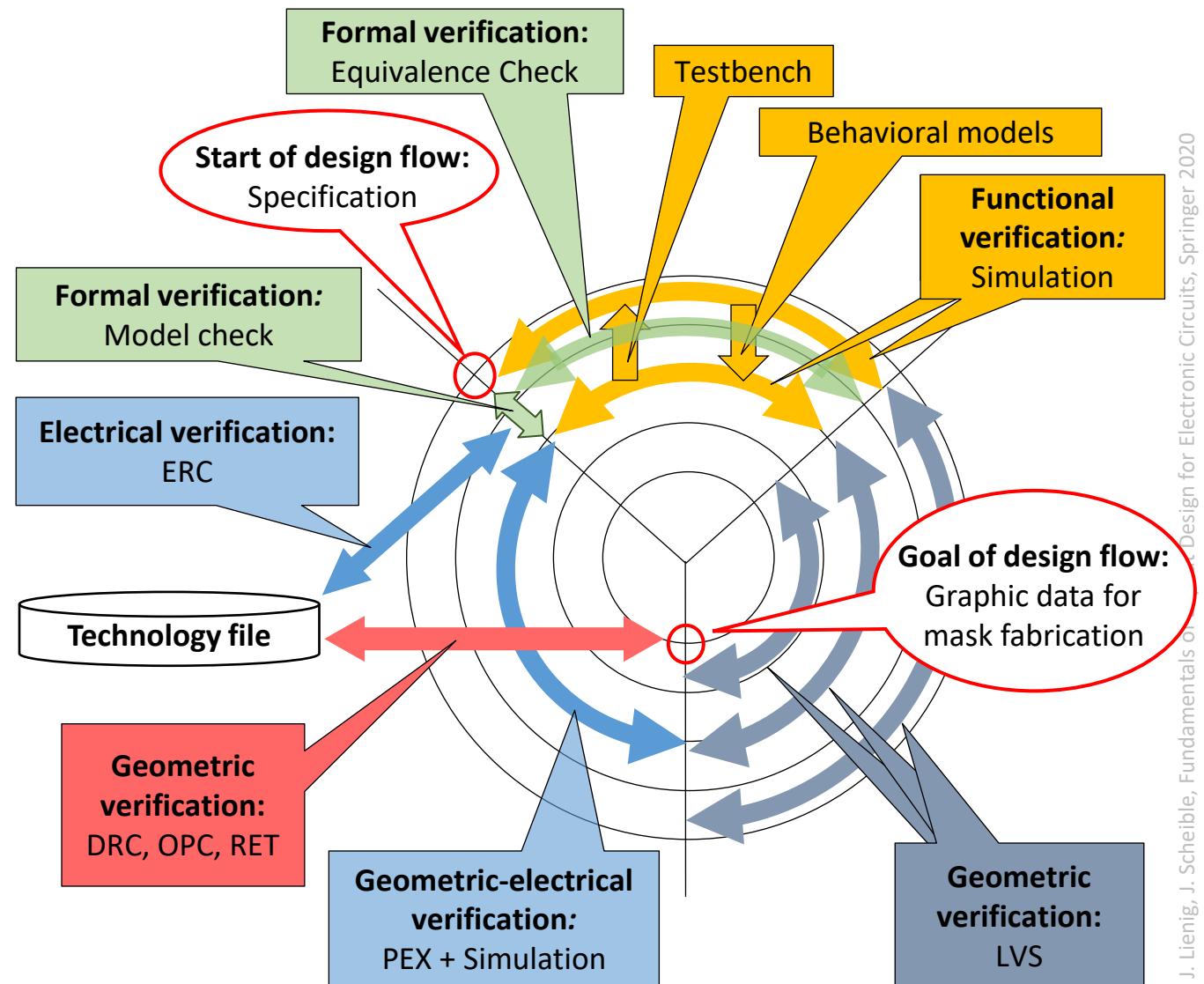
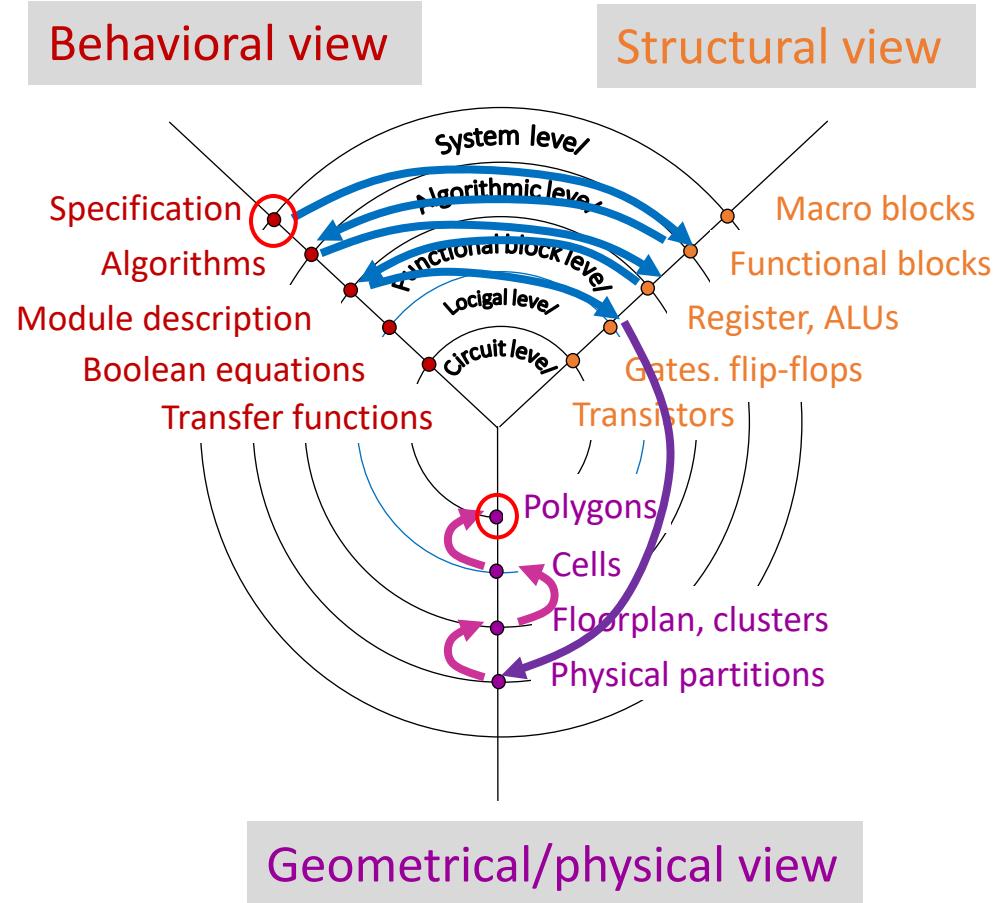


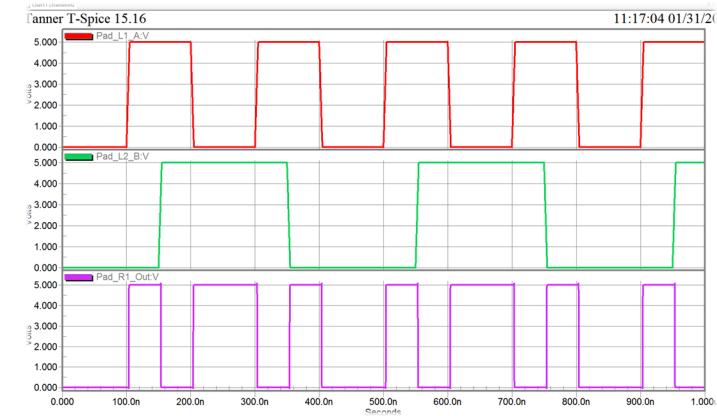
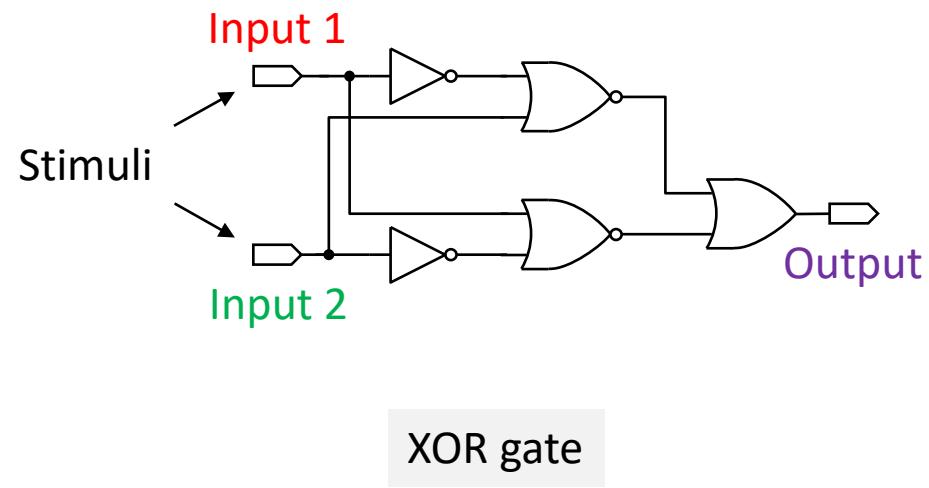




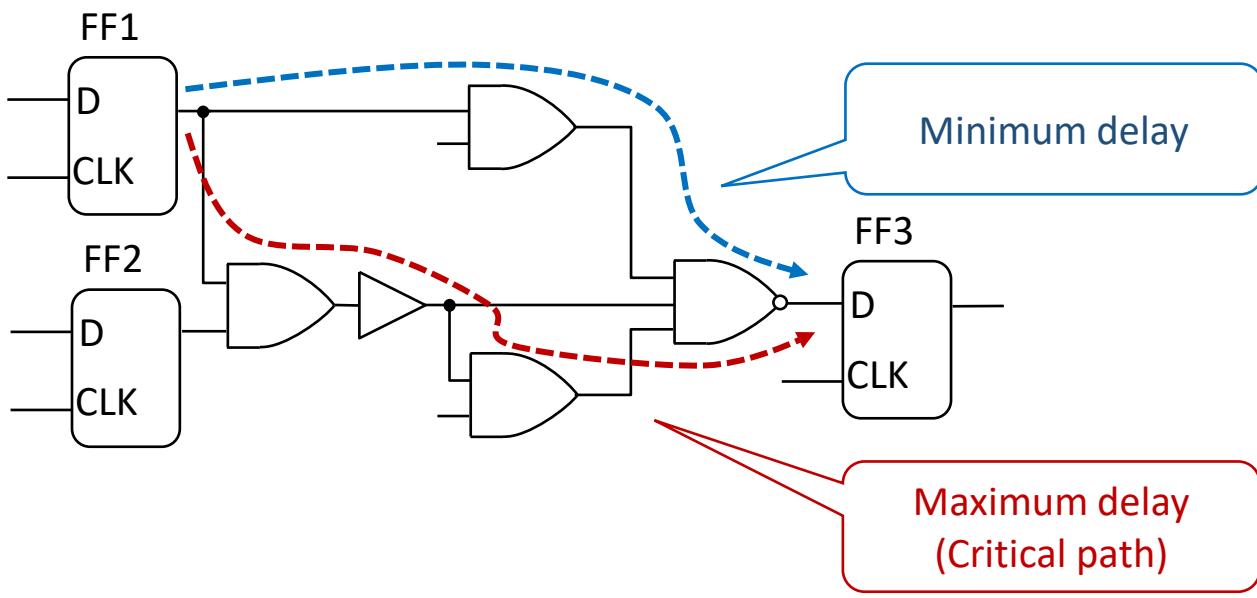


Check	What is checked?	How is it checked?	Method
Model check	Logical characteristic (Assumption is true?)	Mathematical models	Formal verification
Equivalence check	Logical equivalence of two descriptions	Mathematical models	Formal verification
Simulation	Circuit behavior vs. specification	Virtual experiment (stimuli and output)	Functional verification
DRC (OPC, RET)	Layout vs. technological constraints (manufacturability)	Geometrical design rules	Geometric verification
LVS	Layout vs. schematic	Netlist extraction from layout, rule based	Geometric verification
PEX (plus simulation)	Impact of parasitics on circuit behavior	Parameter extraction from layout, rule based; followed by simulation	Geometric and functional verification
ERC	Layout vs. electric process boundaries (reliability)	Connectivity extraction from layout, rule based	Geometric verification
Testing	Compliance for practical usage	Real experiment, customer checking	Validation

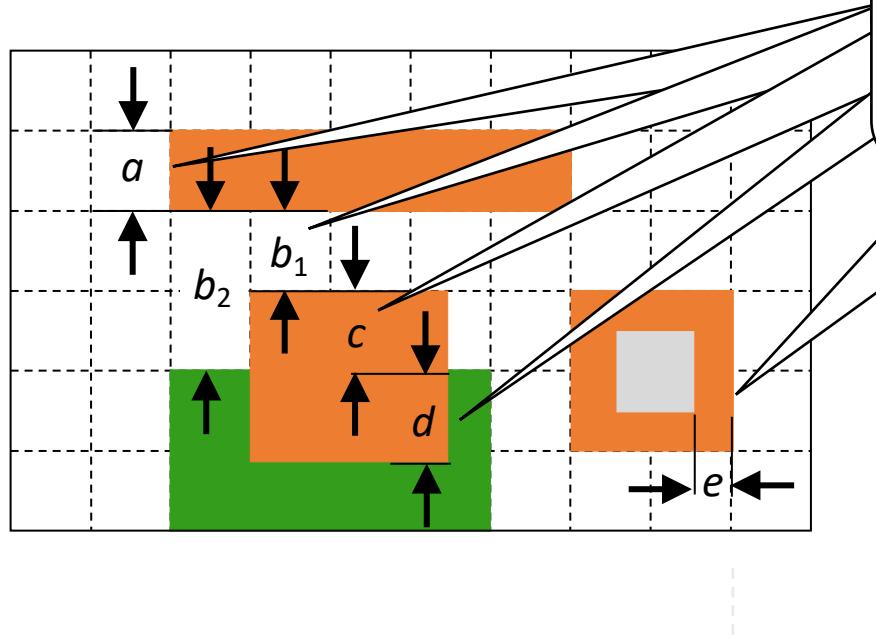




Input 1  
Input 2  
Output

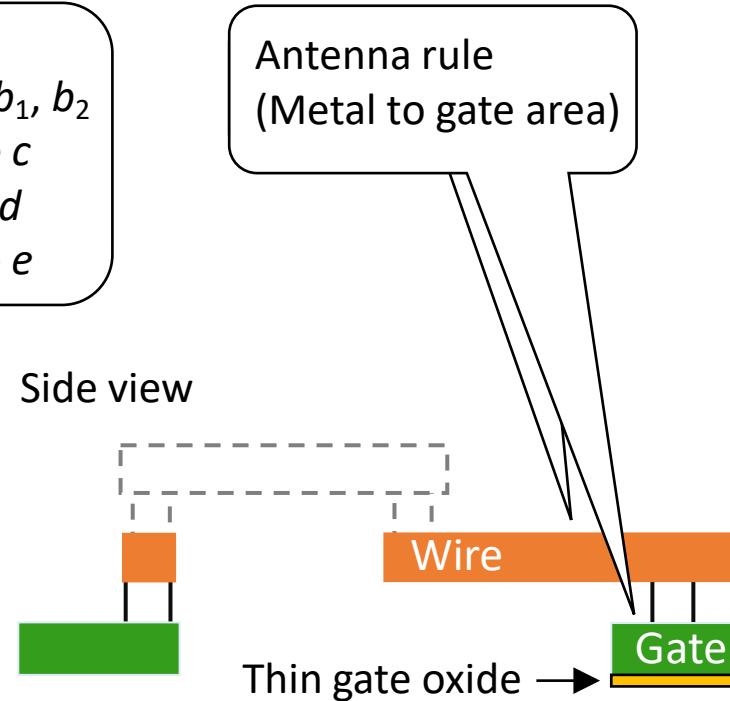


Top view

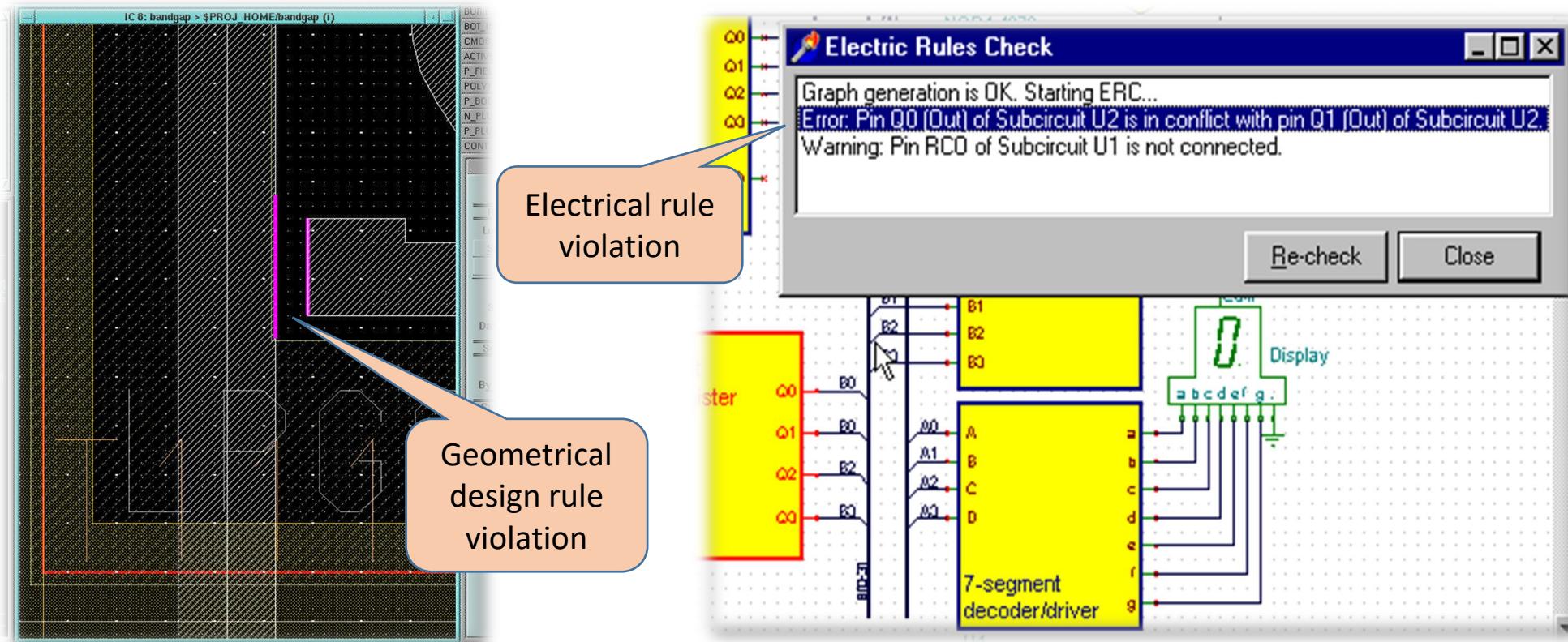


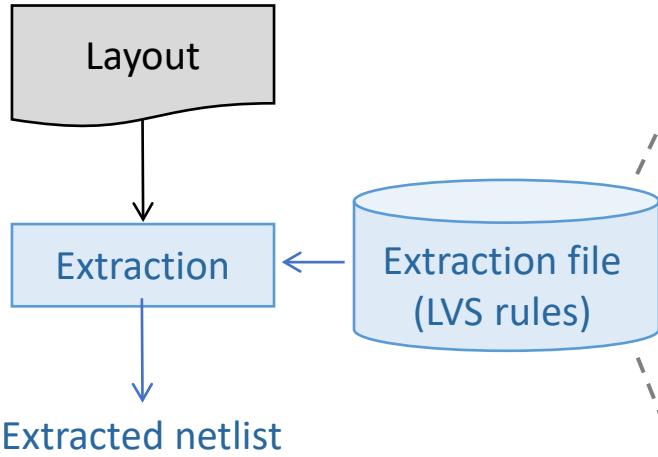
Width rule  $a$   
Spacing rules  $b_1, b_2$   
Extension rule  $c$   
Intrusion rule  $d$   
Enclosure rule  $e$

Side view



Metal 2  
Metal 1  
Poly





### # rev: 990222 GD – Extract Rules File

# \*\*\*\*\*

```

connect(N Well, ndiff, ndiff)
connect(subs, pdiff, pdiff)
connect(allsubs, subs, subs)
connect(ndiff, Metal1, Active Contact)
connect(pdiff, Metal1, Active Contact)
connect(Poly, Metal1, Poly Contact)
connect(Metal1, Metal2, Via)
  
```

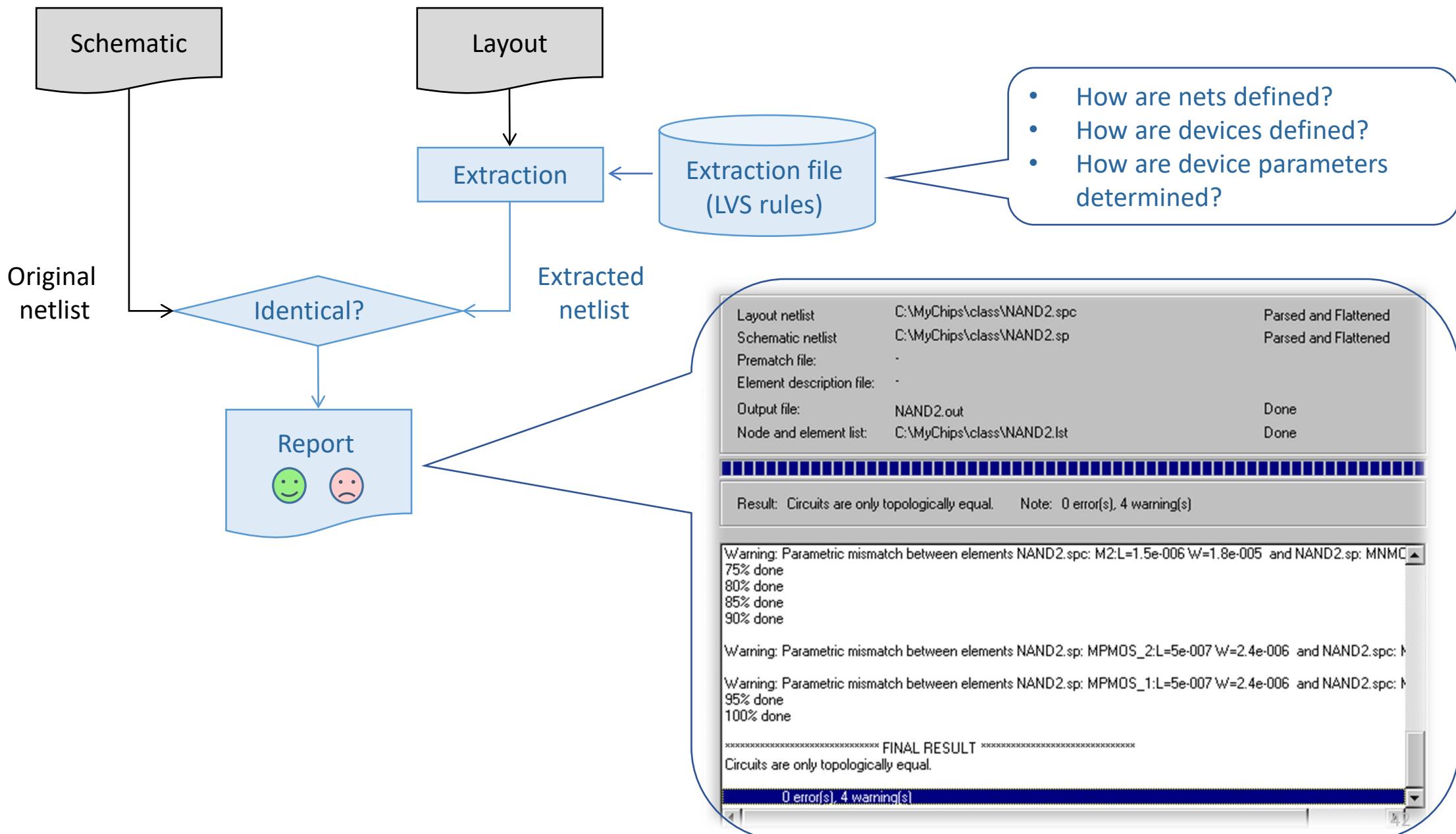
How are layers connected  
and thus nets defined?

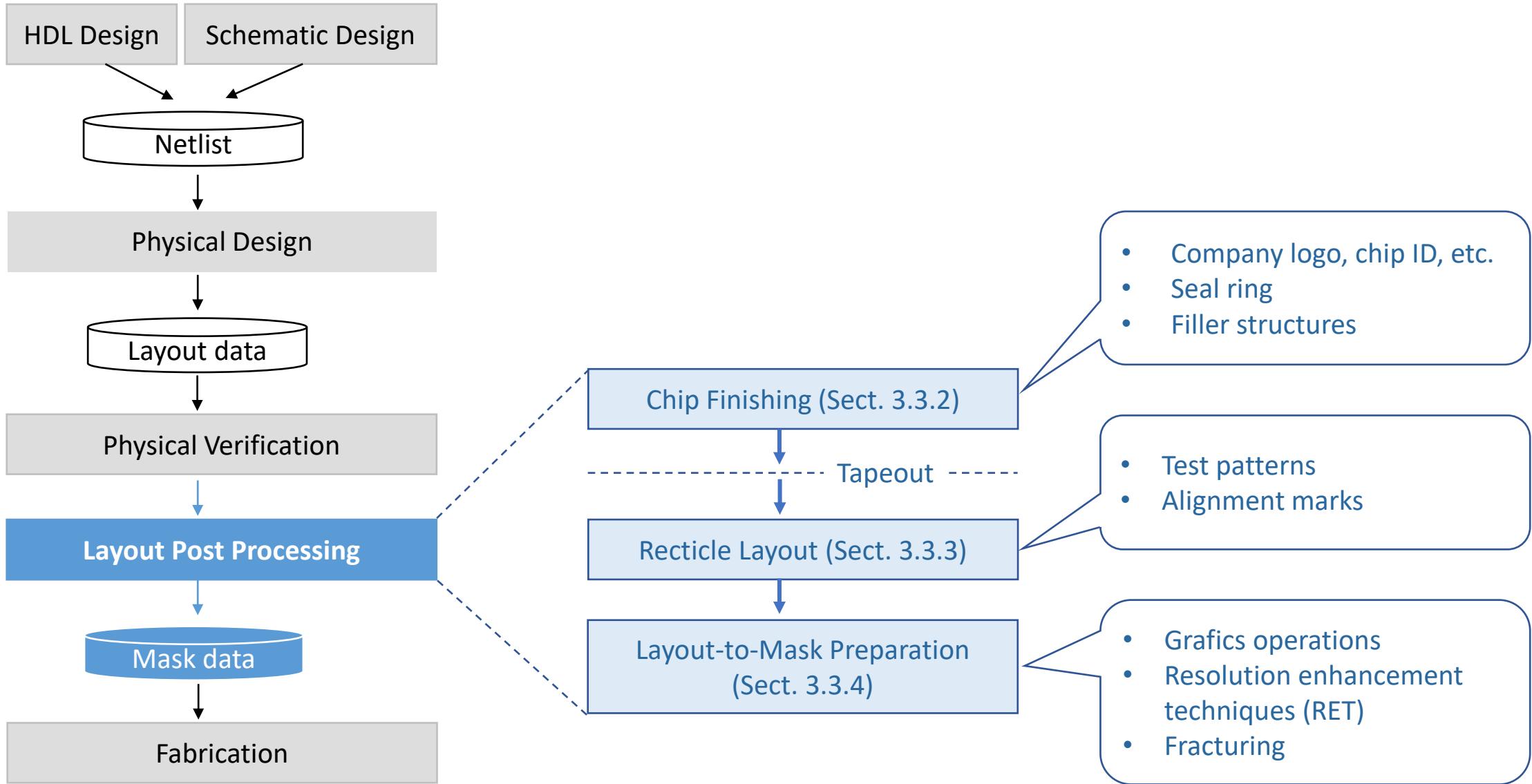
### # NMOS transistor with poly1 gate

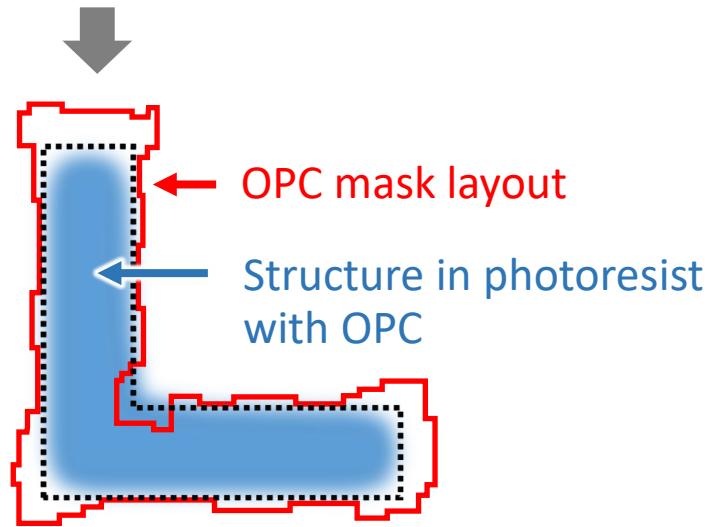
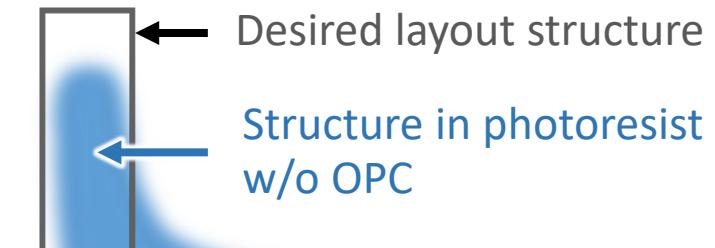
```

device = MOSFET(
    RLAYER=ntran;
    Drain=ndiff, WIDTH;
    Gate=Poly;
    Source=ndiff, WIDTH;
    Bulk=subs;
    MODEL=NMOS;
)
  
```

How are devices defined?  
How are device parameters  
determined?

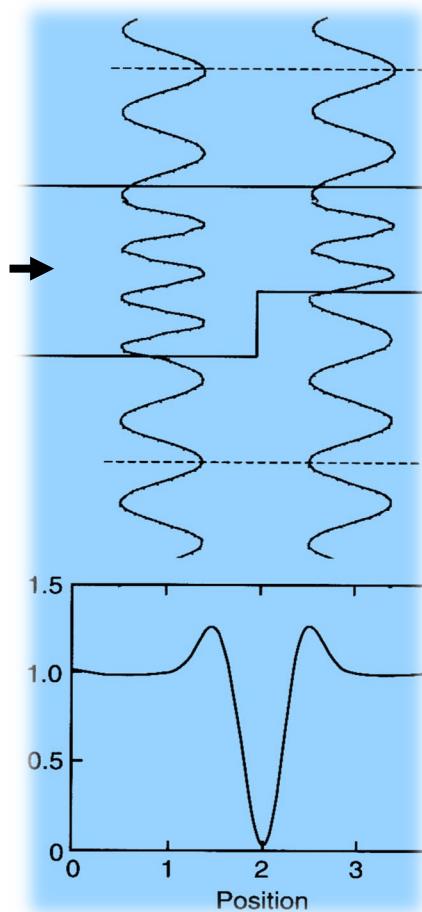






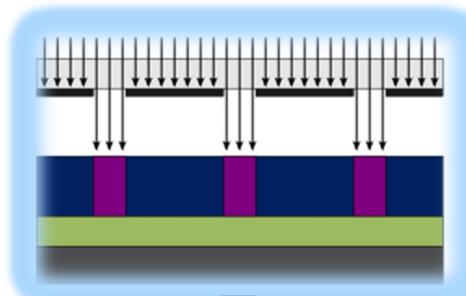
## Optical Proximity Correction (OPC)

Mask with phase shift

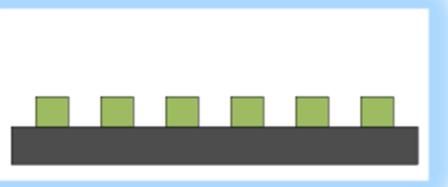
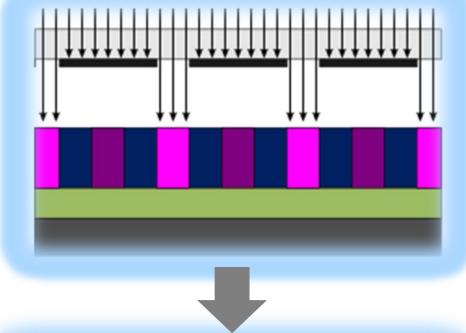


## Phase Shift Mask

Mask 1



Mask 2



## Double Patterning