Chapter 5: Steps in Physical Design: From Netlist Generation to Layout Post Processing

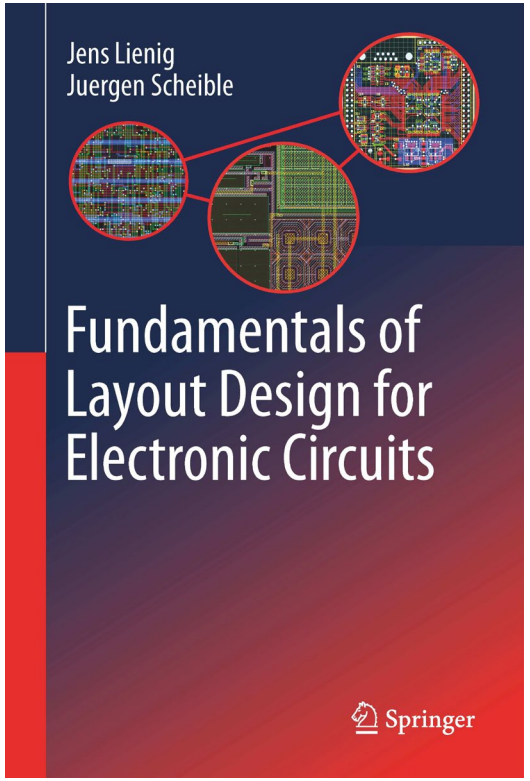
5.1 Generating a Netlist Using Hardware Description Language

5.2 Generating a Netlist Using Symbolic Design Entry

5.3 Primary Steps in Physical Design

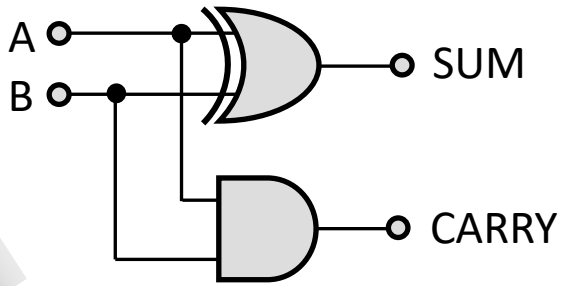
5.4 Verification

5.5 Layout Post Processing

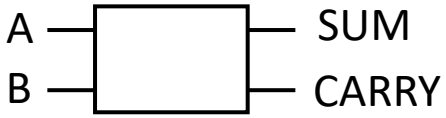


Chapter 5: Steps in Physical Design: From Netlist Generation to Layout Post Processing

Half adder

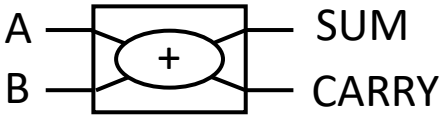


Entitiy with
interface description

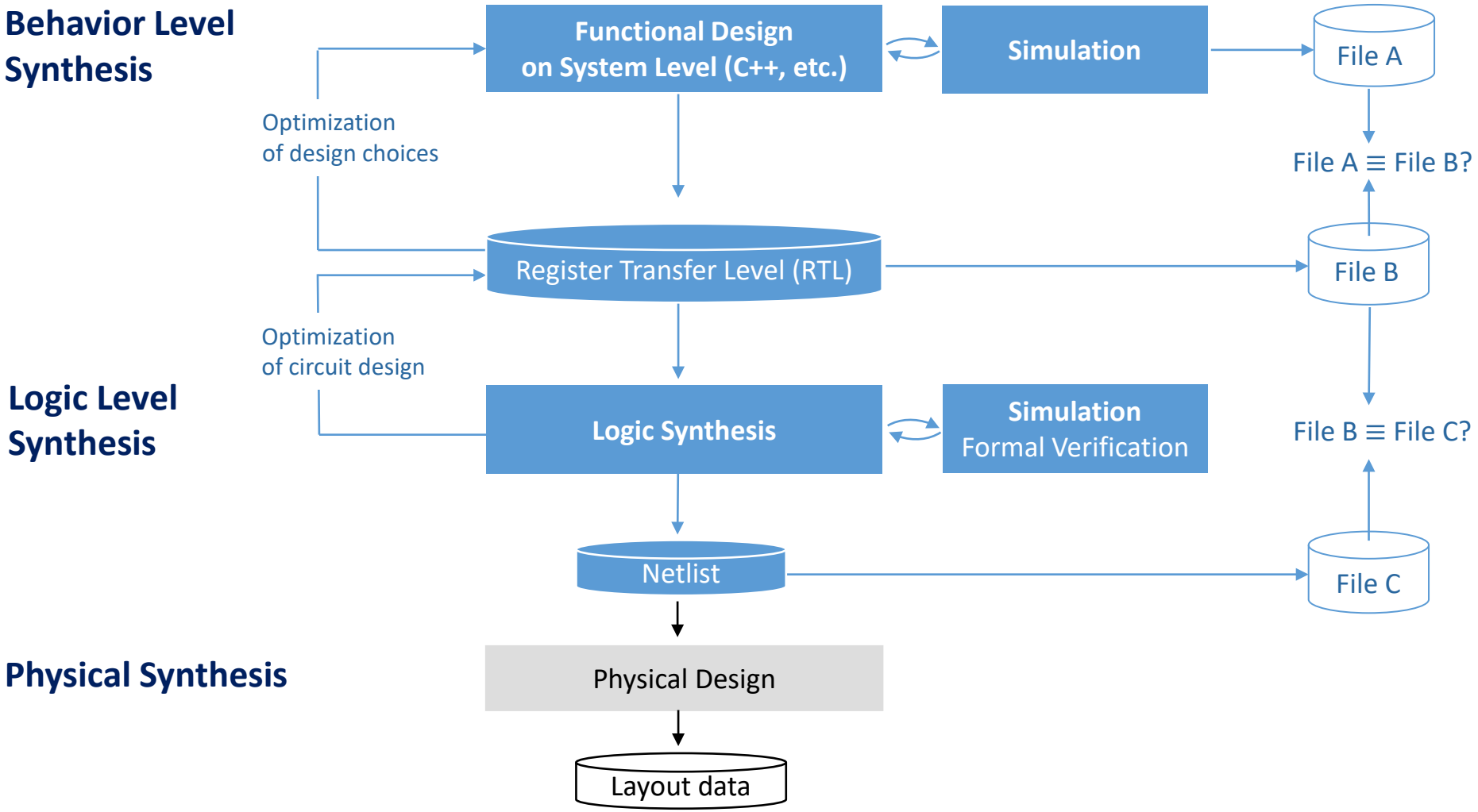



```
entity HALFADDER is
  port(A, B       : in bit;
       SUM, CARRY: out bit);
end entity HALFADDER;
```

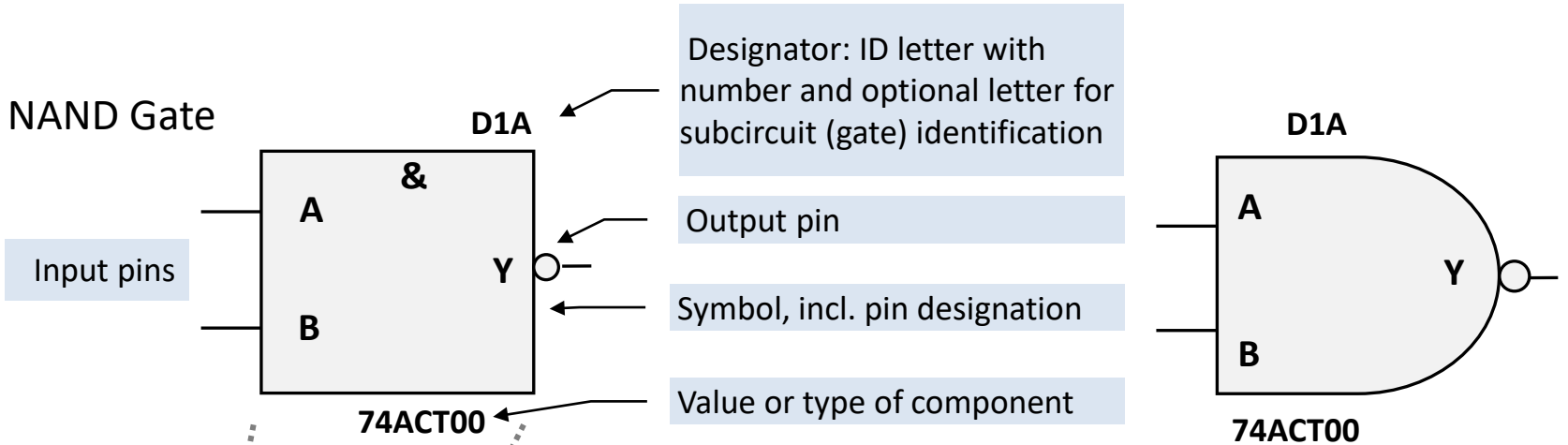
Architecture with
implementation

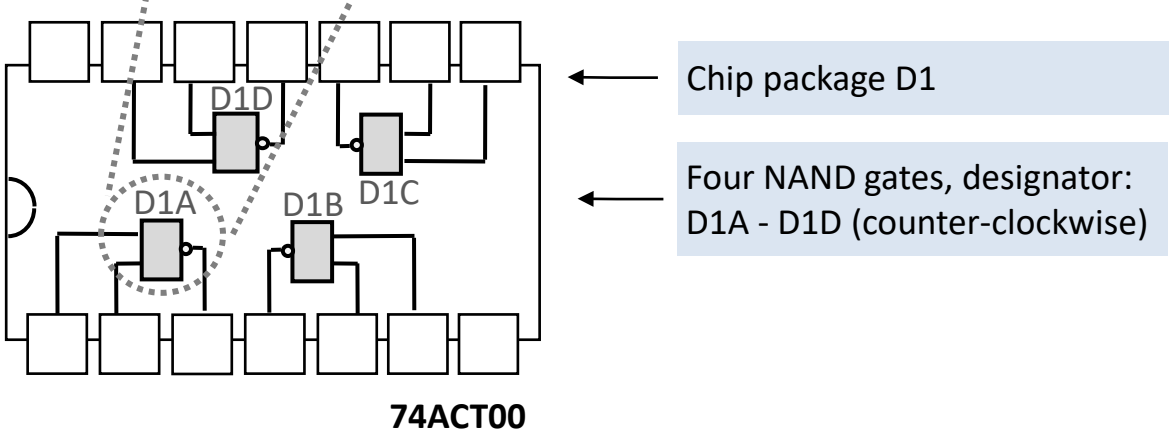


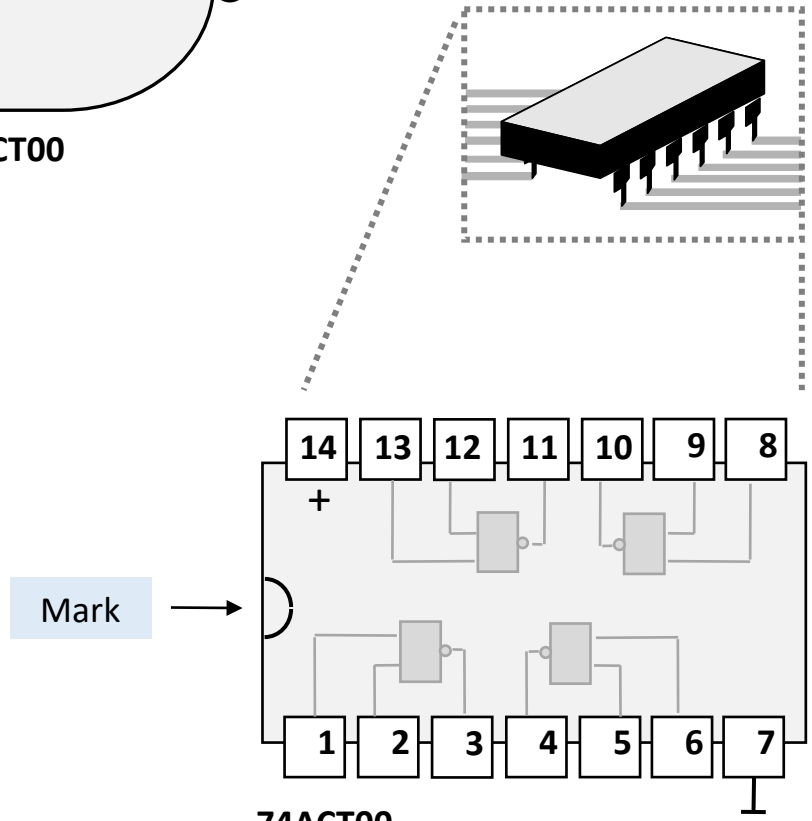

```
architecture RTL of HALFADDER is
begin
      SUM   <= A xor B;
      CARRY <= A and B;
end architecture RTL;
```

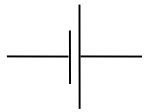
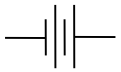
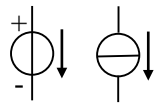
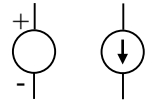
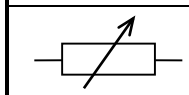
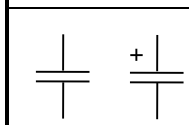
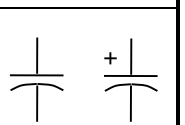
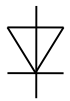


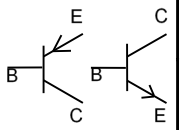
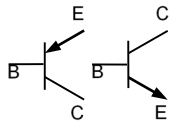
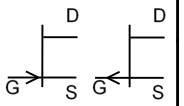
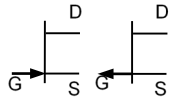
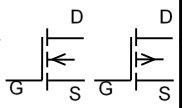
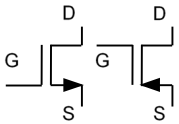
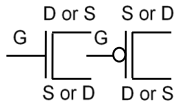
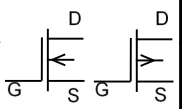
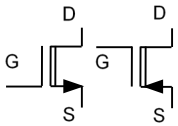
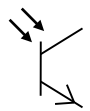
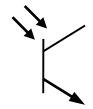
NAND Gate

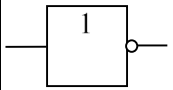
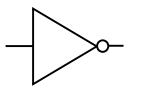
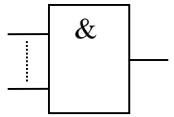
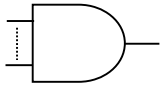
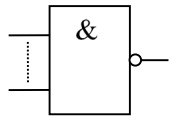
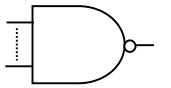
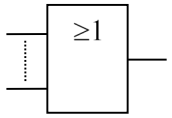
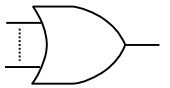
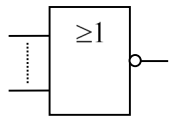
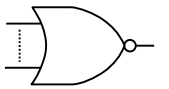
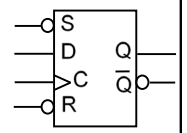


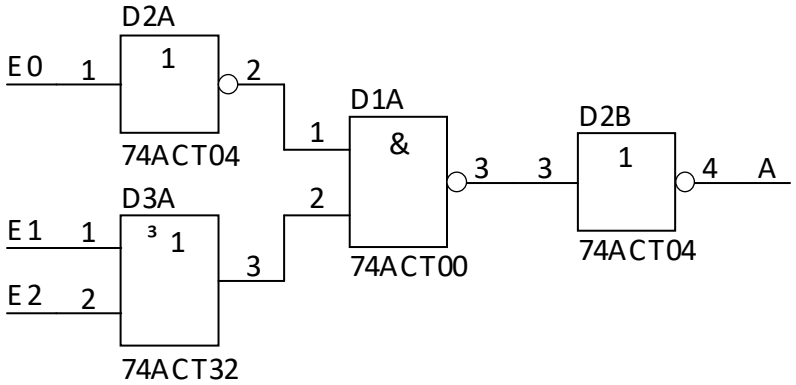


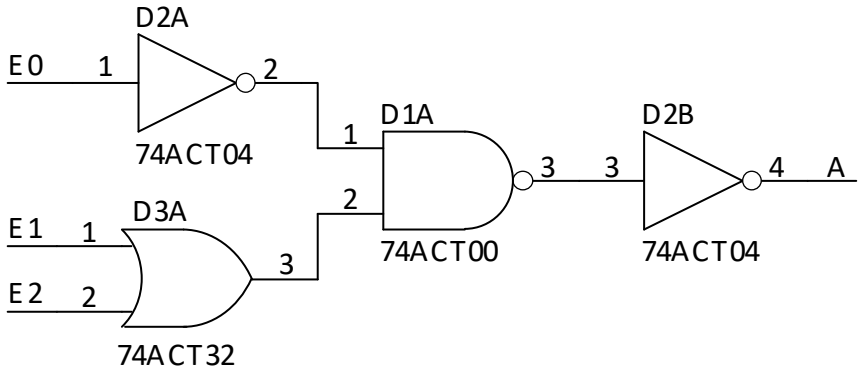


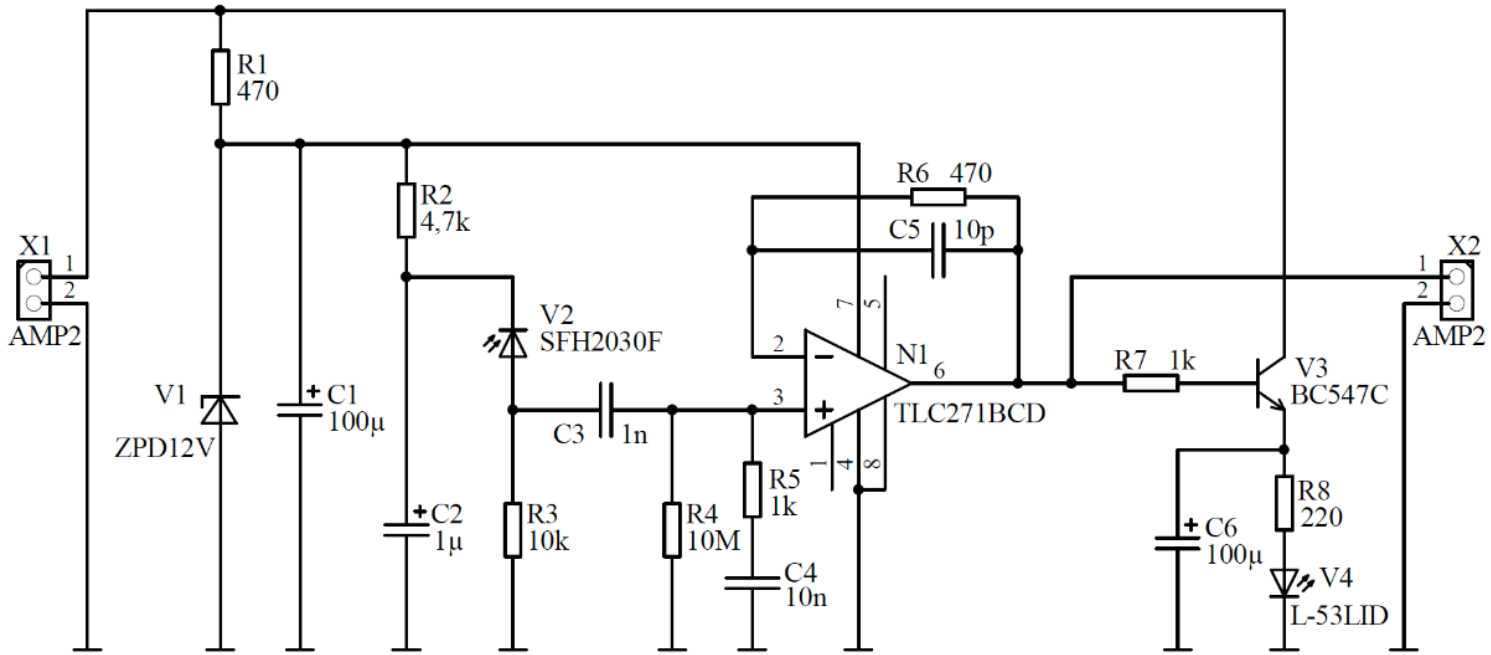
IEEE/IEC symbol	Description	Alternative/ distinctive shape
	Primary cell, secondary cell, storage battery The longer line represents the positive pole, the shorter one the negative pole.	
	Ground symbols	
	DC voltage source DC current source	
	Resistor	
	Resistor, adjustable	
	Capacitor Polarized capacitor	
	Inductor, coil, winding, choke (without core)	
	Semiconductor diode; (triangle = anode, bar = cathode)	
	Light emitting diode (LED) Photo-diode	

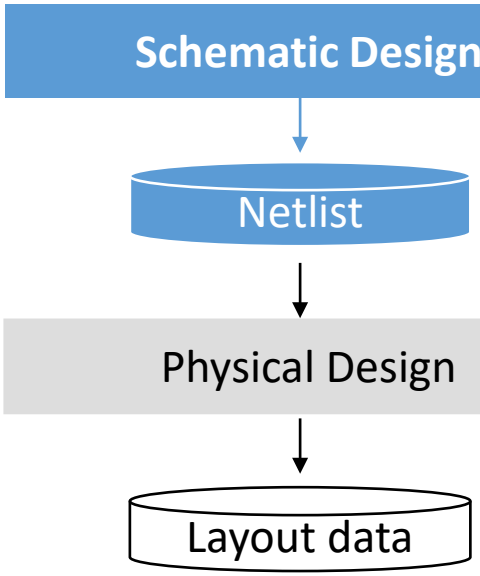
IEEE/IEC symbol	Description	Alternative/ distinctive shape
	pnp- npn- transistor	
	n-channel p-channel Junction FET	
	n-channel p-channel Enhancement MOSFET	
	n-channel p-channel (n-MOS) (p-MOS) Enhancement MOSFET (digital representation)	
	n-channel p-channel Depletion MOSFET	
	Photo transistor (npn model)	

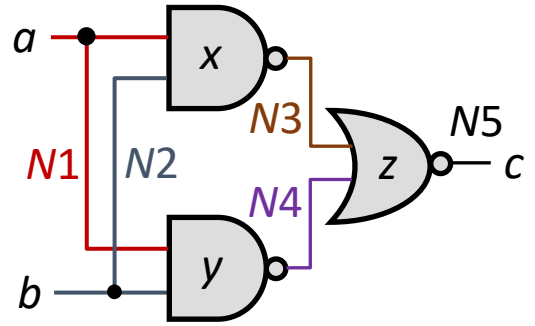
IEEE/IEC symbol	Description	Alternative/ distinctive shape
	Inverter	
	AND gate	
	NAND (AND with negated output)	
	OR gate	
	NOR (OR with negated output)	
	D-Flipflop	
	Operational amplifier	









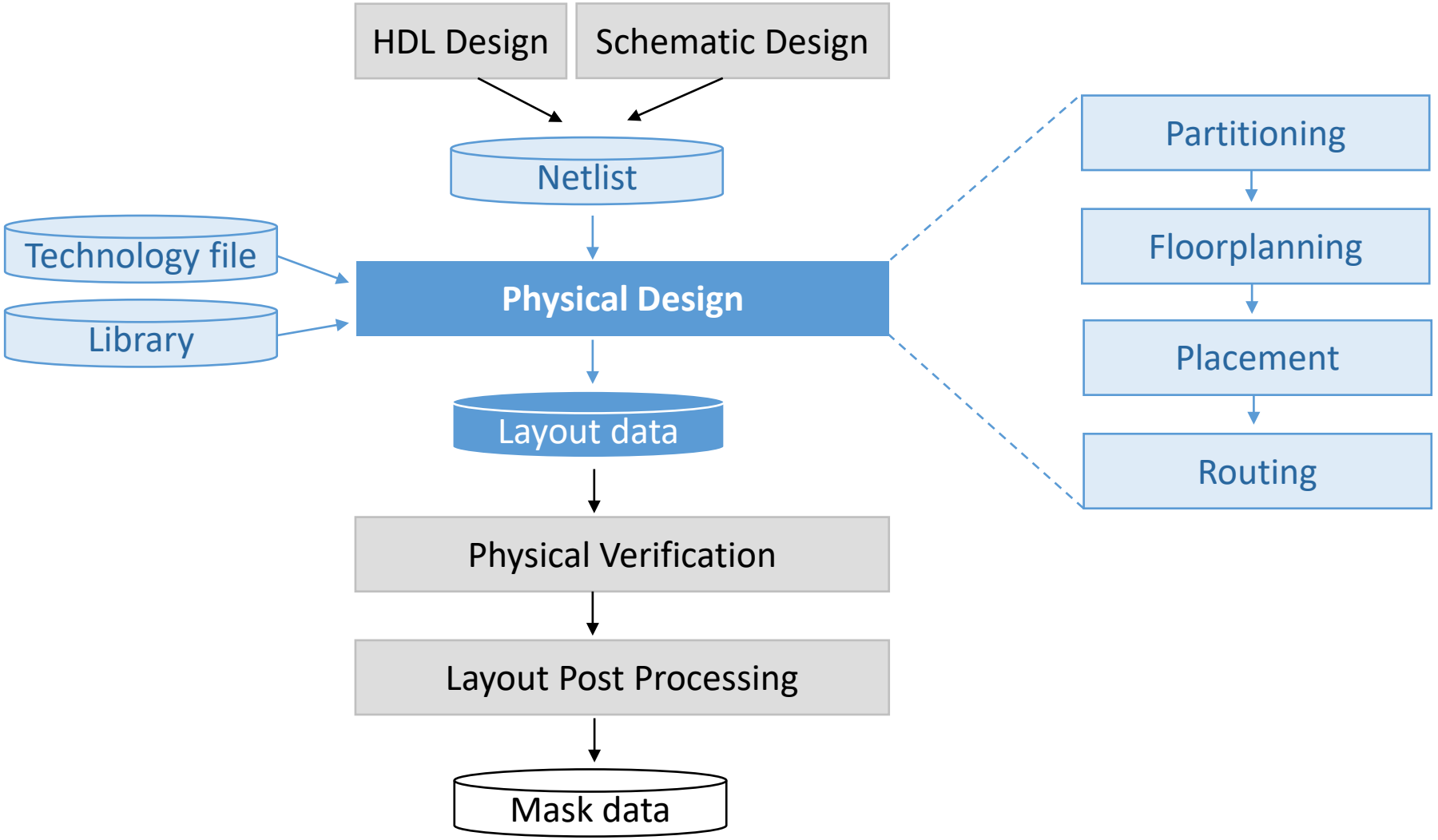


Net-oriented netlist

(*N*1: *a*, *x*.IN1, *y*.IN1)
(*N*2: *b*, *x*.IN2, *y*.IN2)
(*N*3: *x*.OUT, *z*.IN1)
(*N*4: *y*.OUT, *z*.IN2)
(*N*5: *z*.OUT, *c*)

Pin-oriented netlist

(*a*: *N*1)
(*b*: *N*2)
(*c*: *N*5)
(*x*: IN1 *N*1, IN2 *N*2, OUT *N*3)
(*y*: IN1 *N*1, IN2 *N*2, OUT *N*4)
(*z*: IN1 *N*3, IN2 *N*4, OUT *N*5)



System level

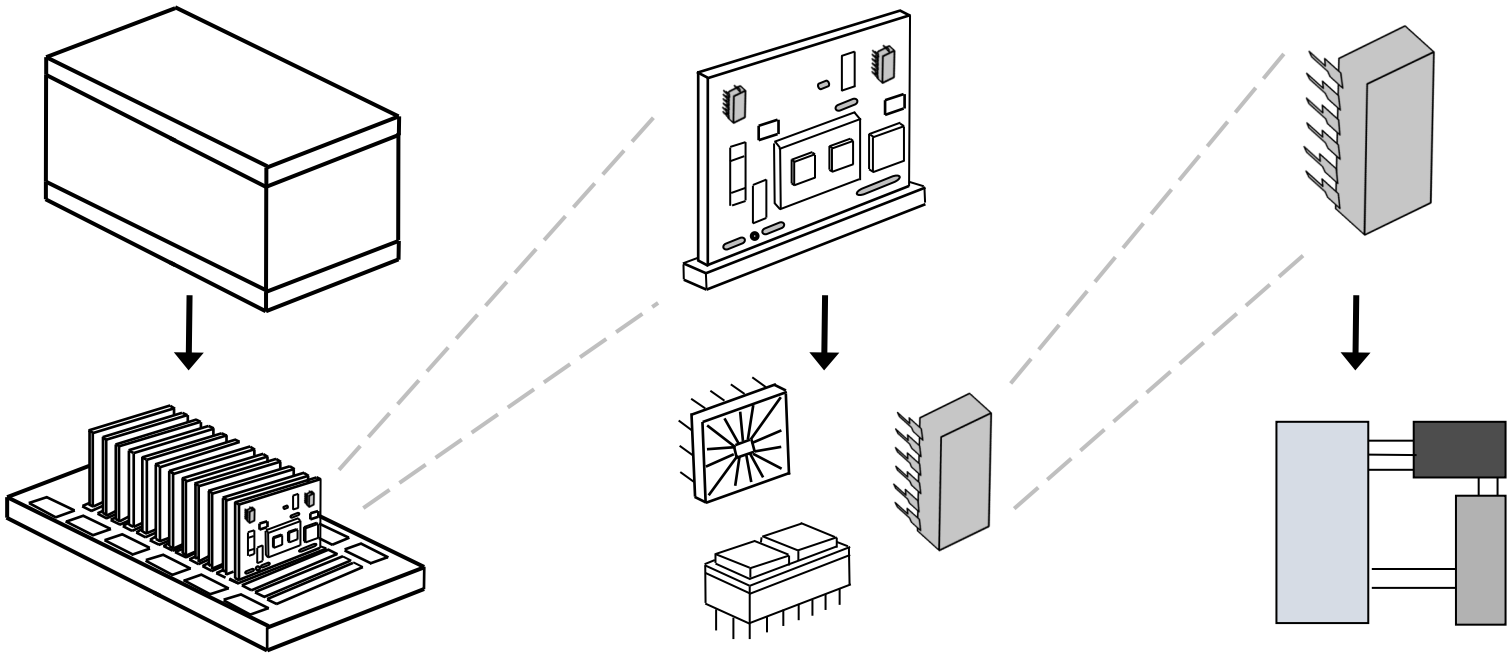
Each subsystem (PCB) can be designed and manufactured indepently

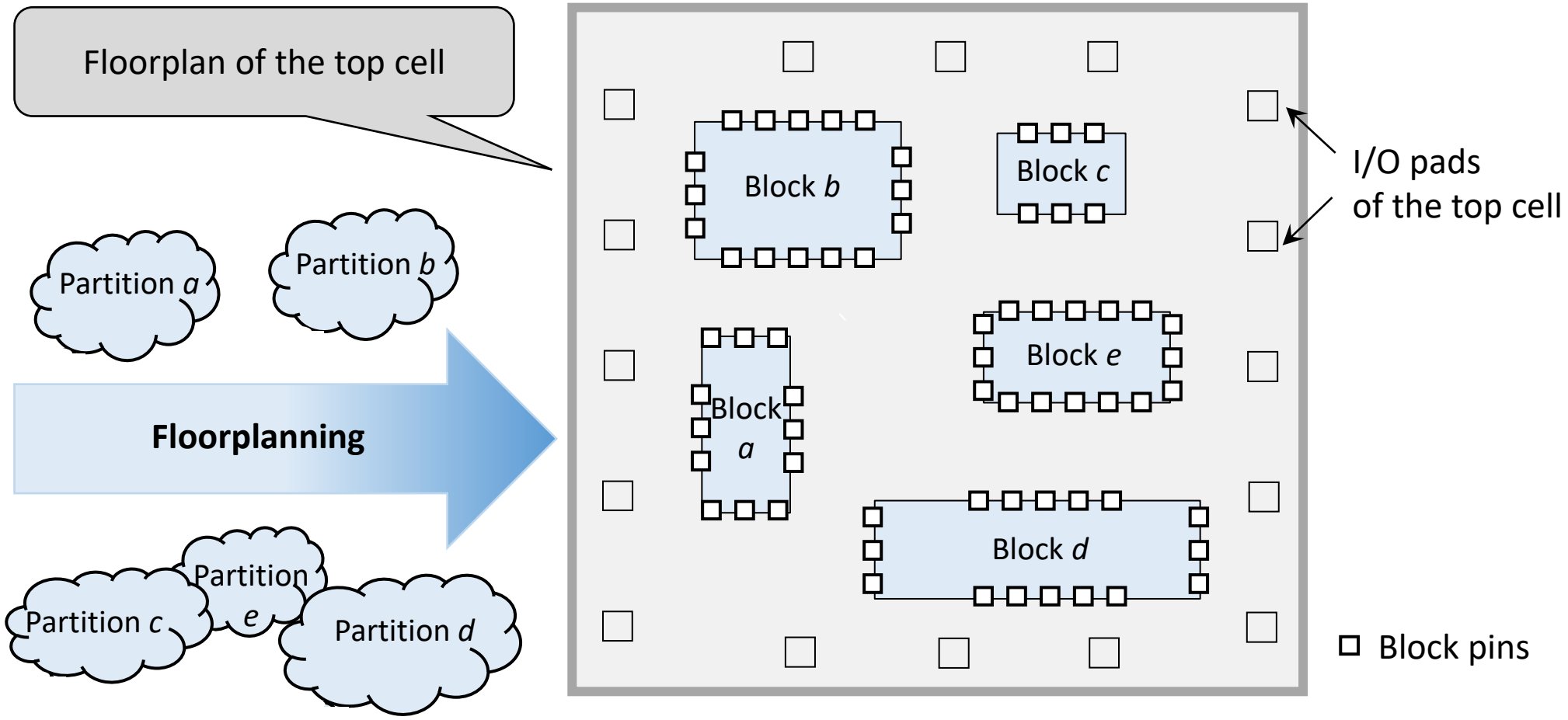
Board level

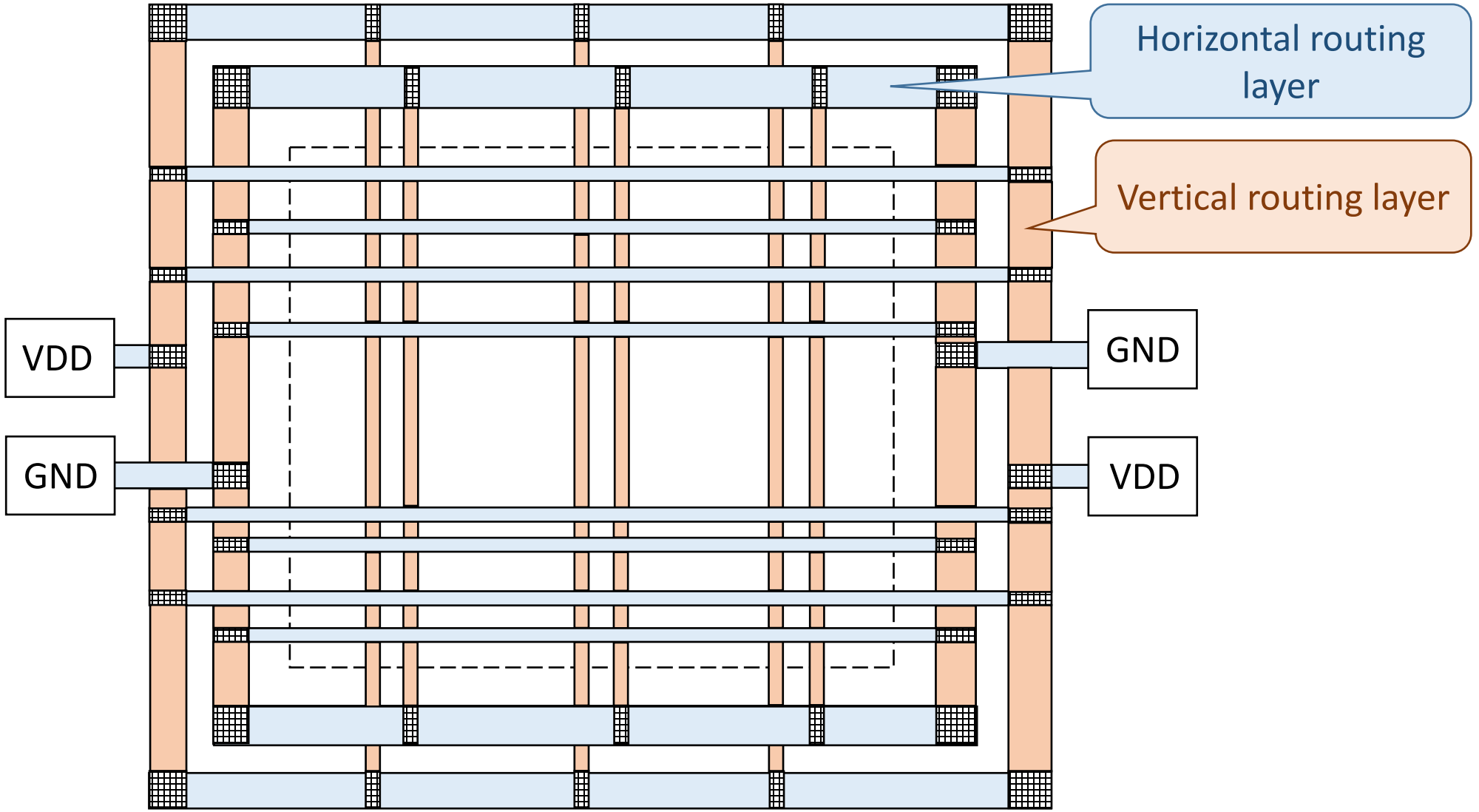
Determining subcircuits that can be realized as separate units (ICs, MCMs)

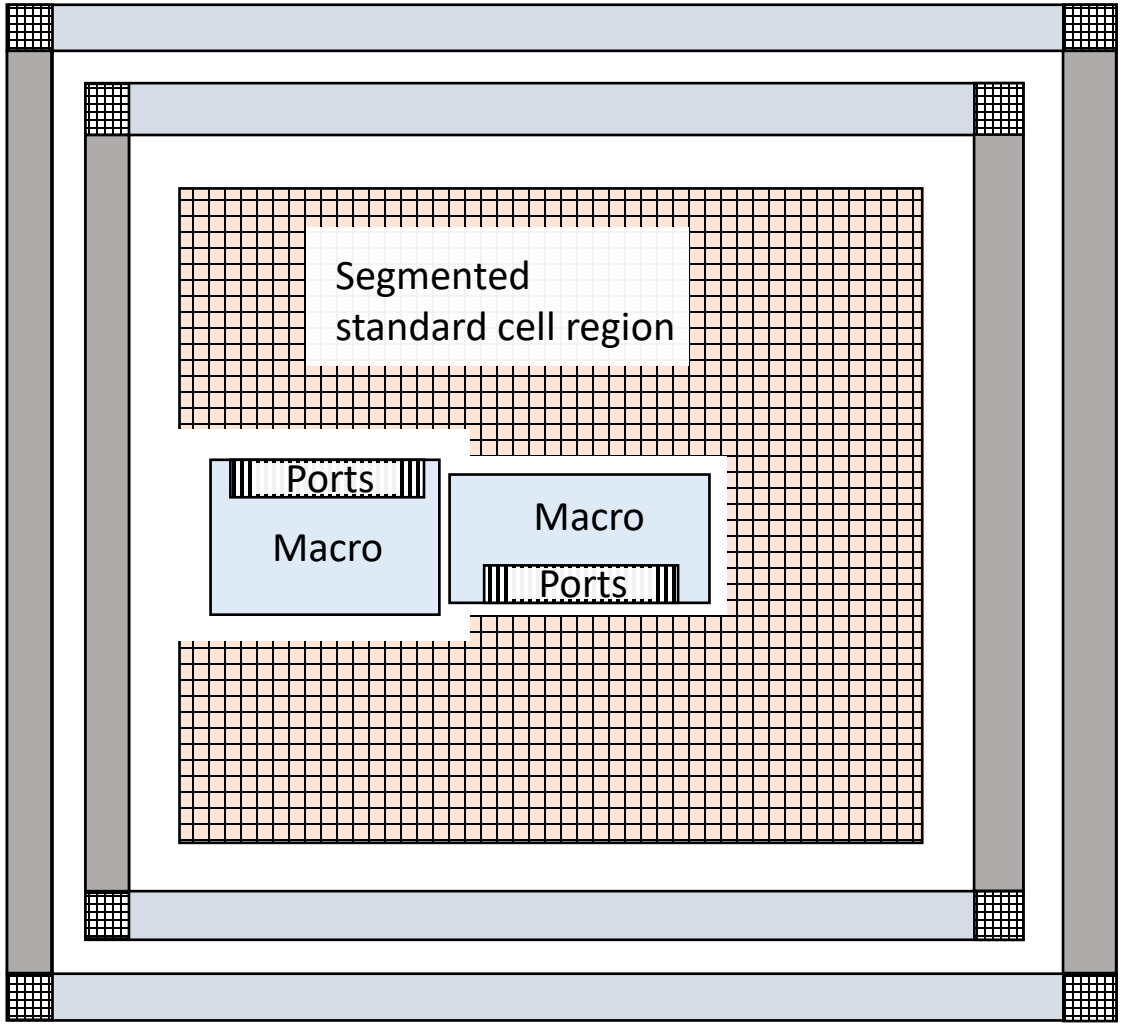
Chip level

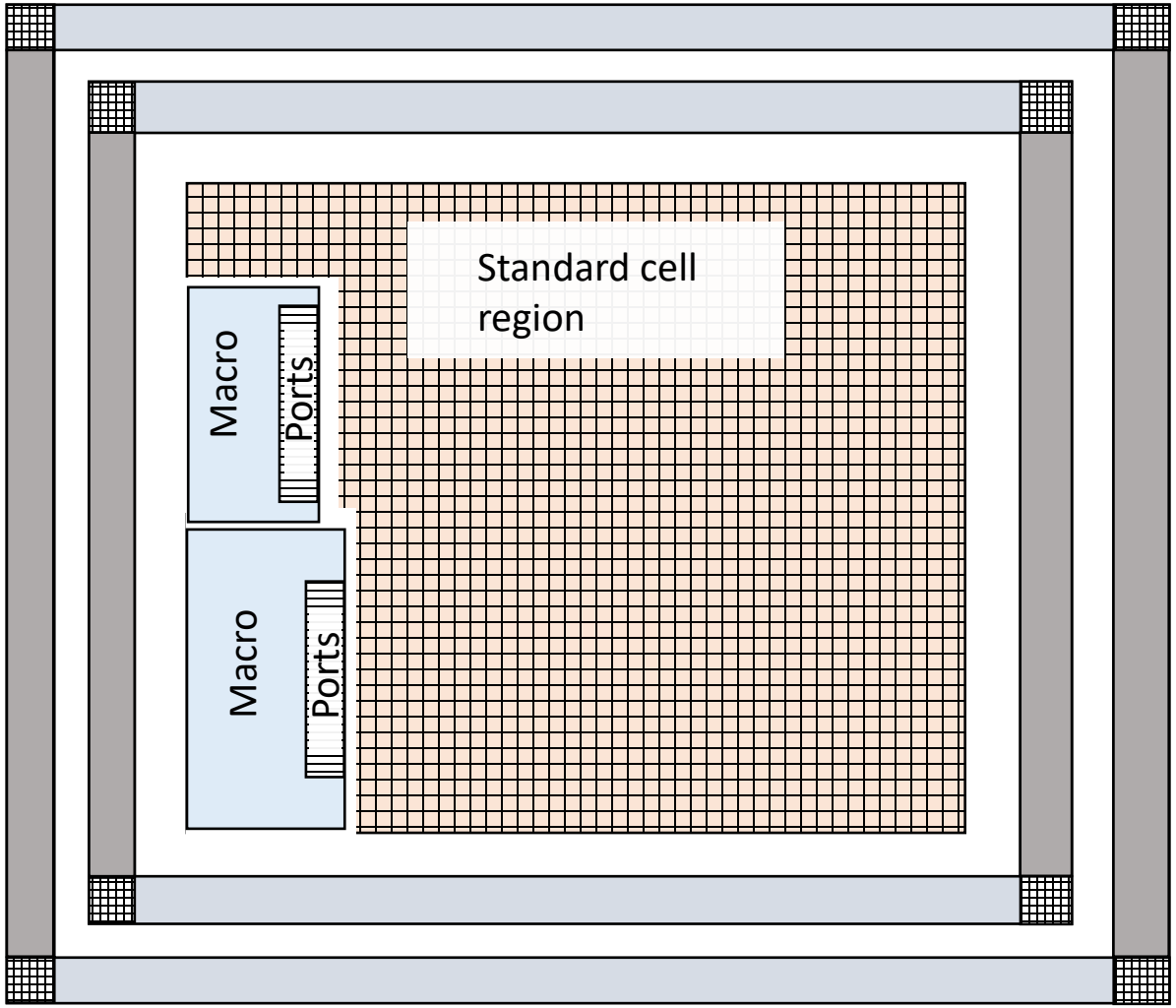
ICs are partitioned into smaller blocks that can be designed independently for the purpose of reducing complexity

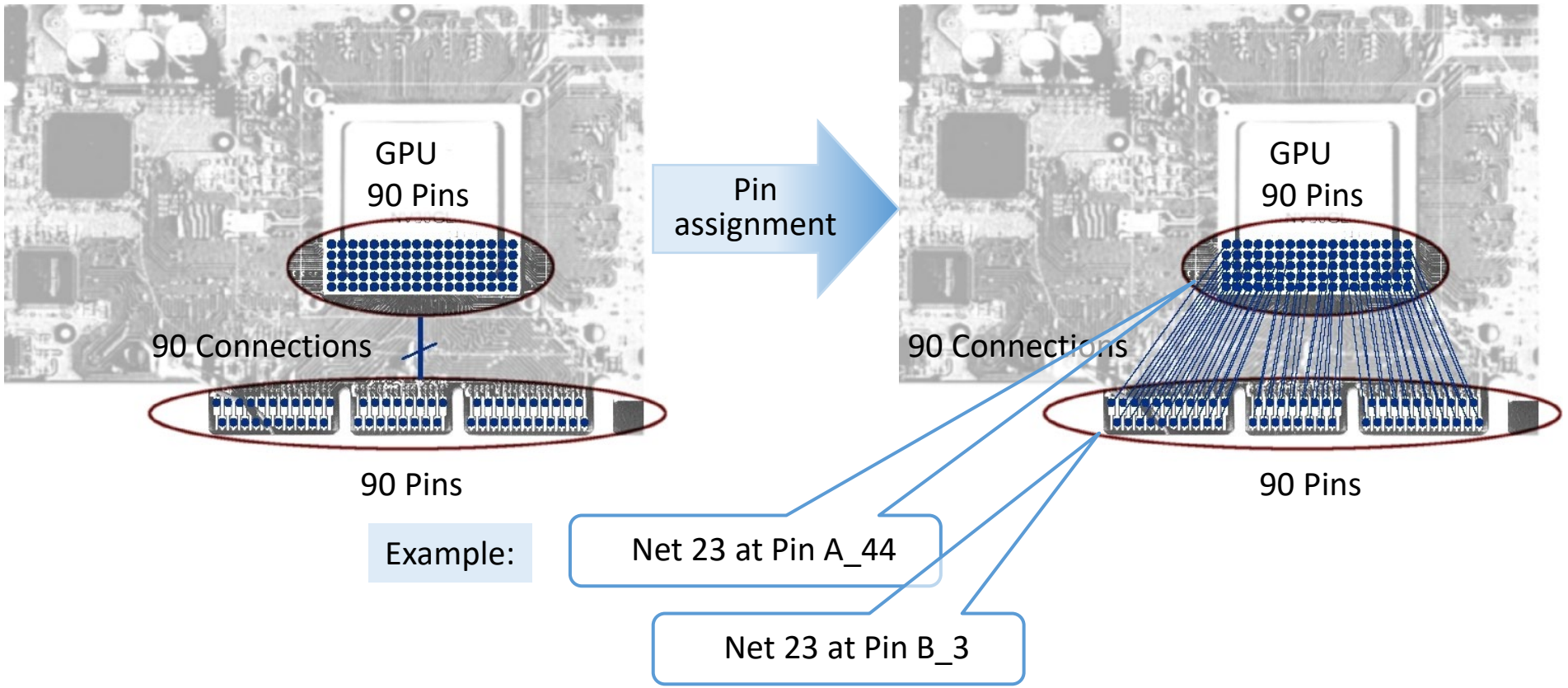


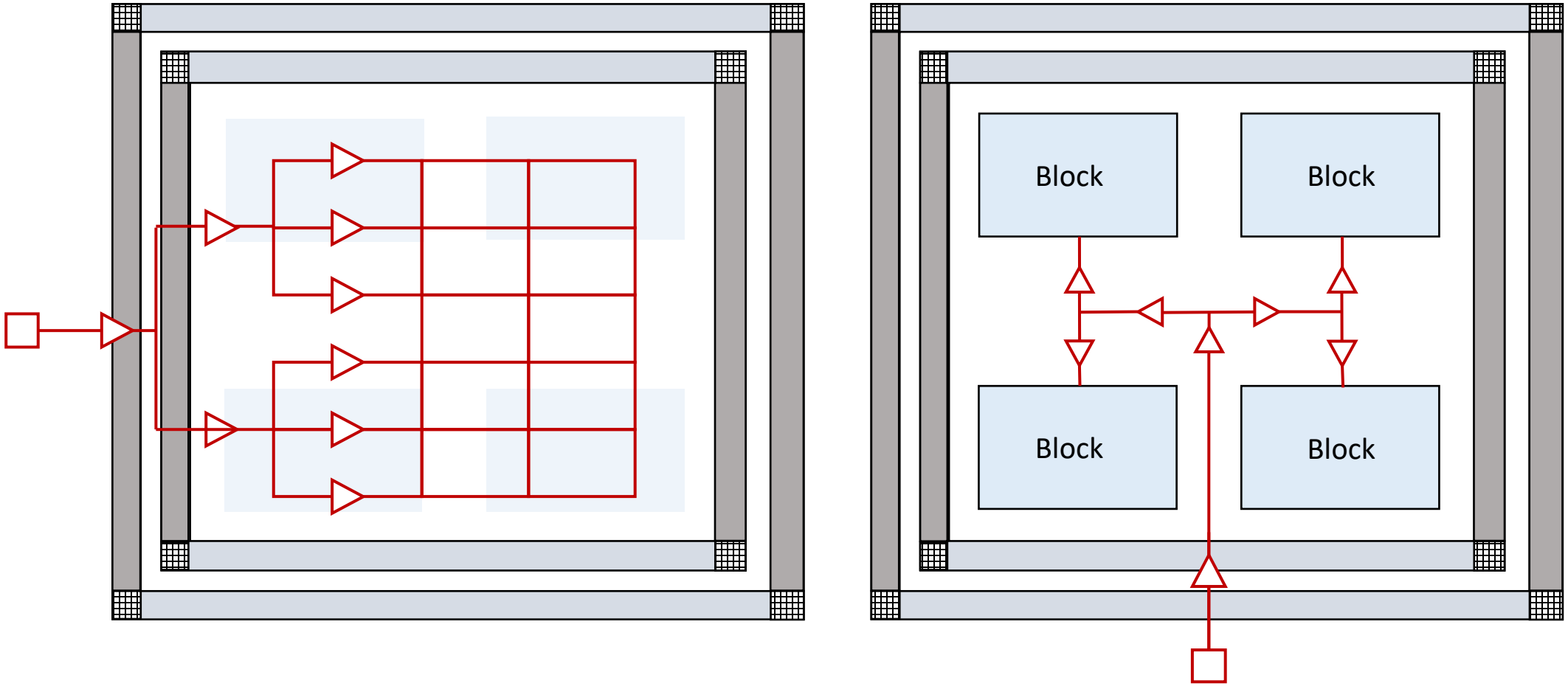


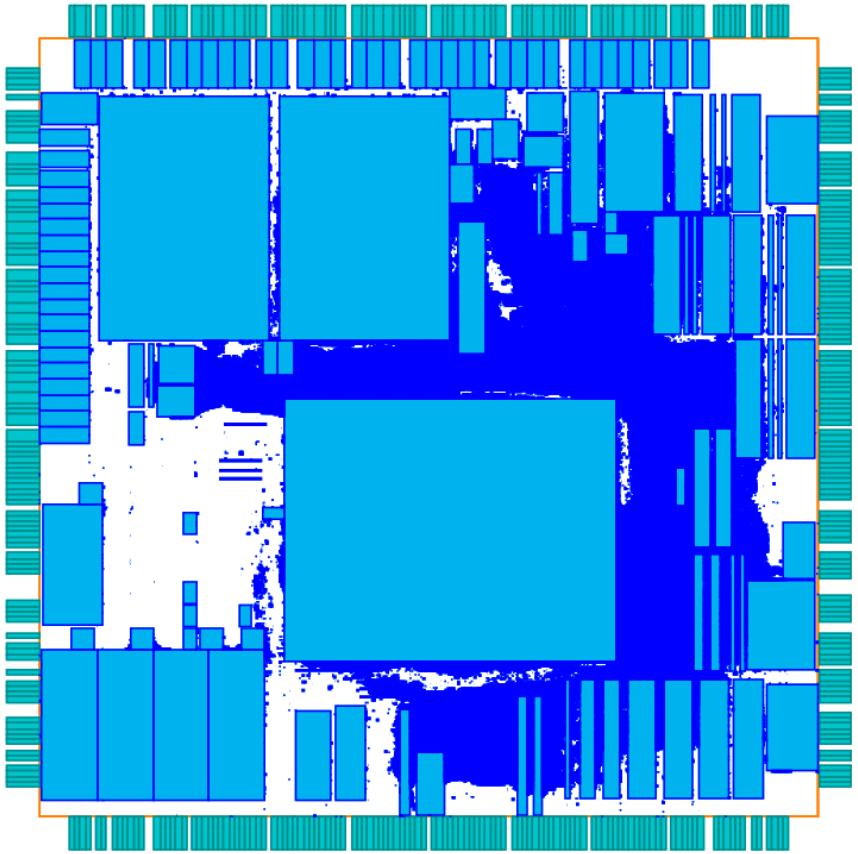


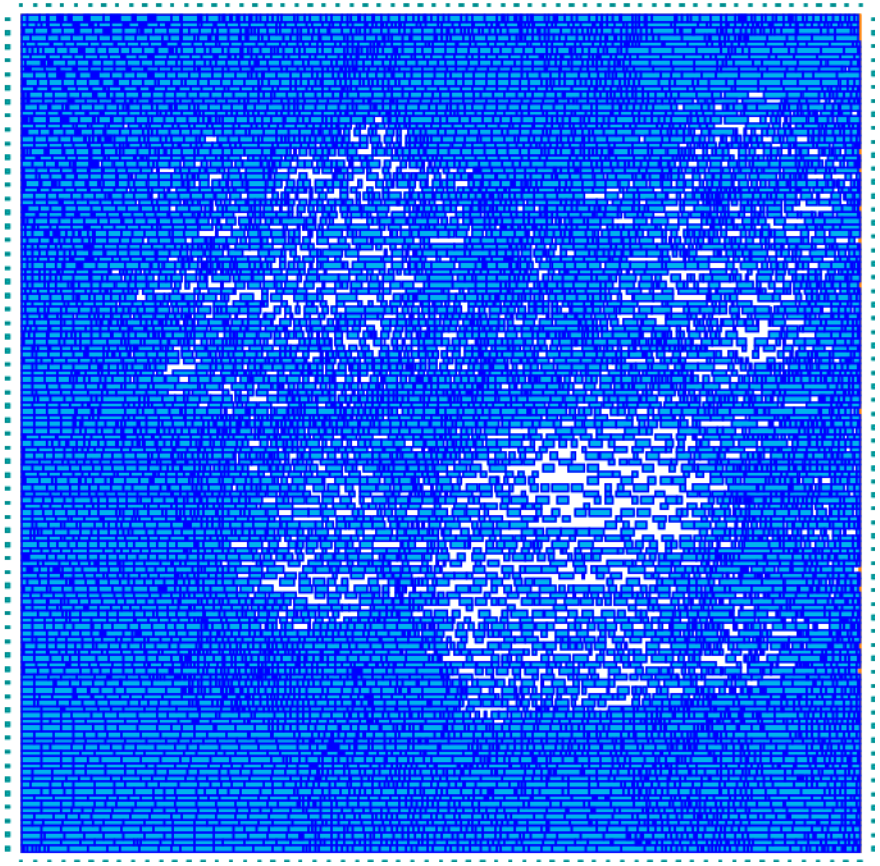


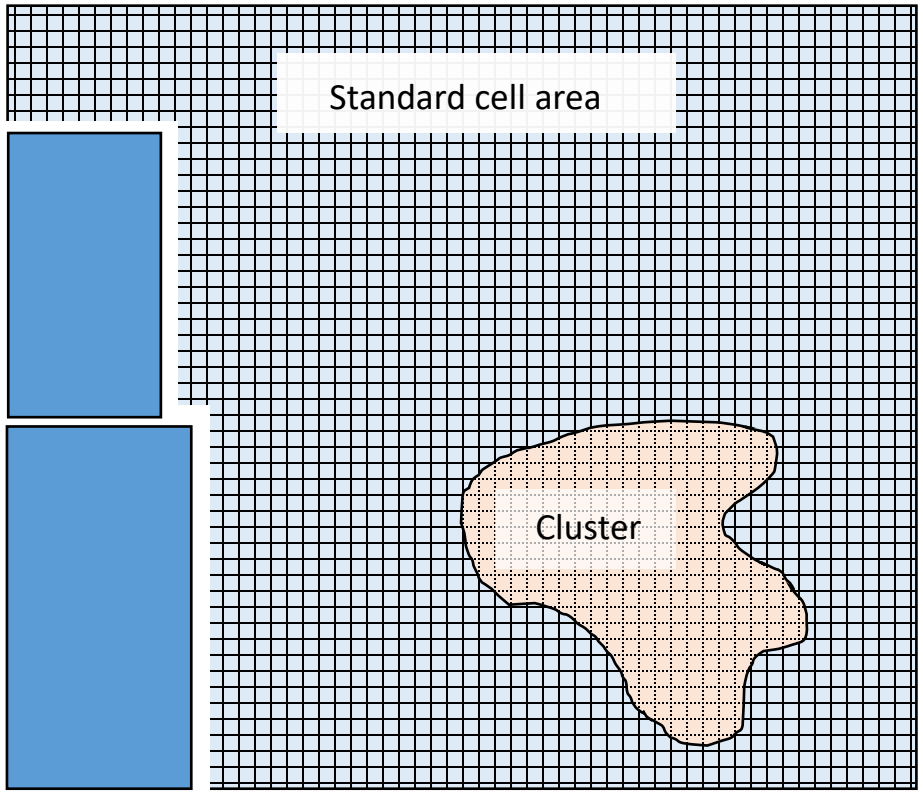


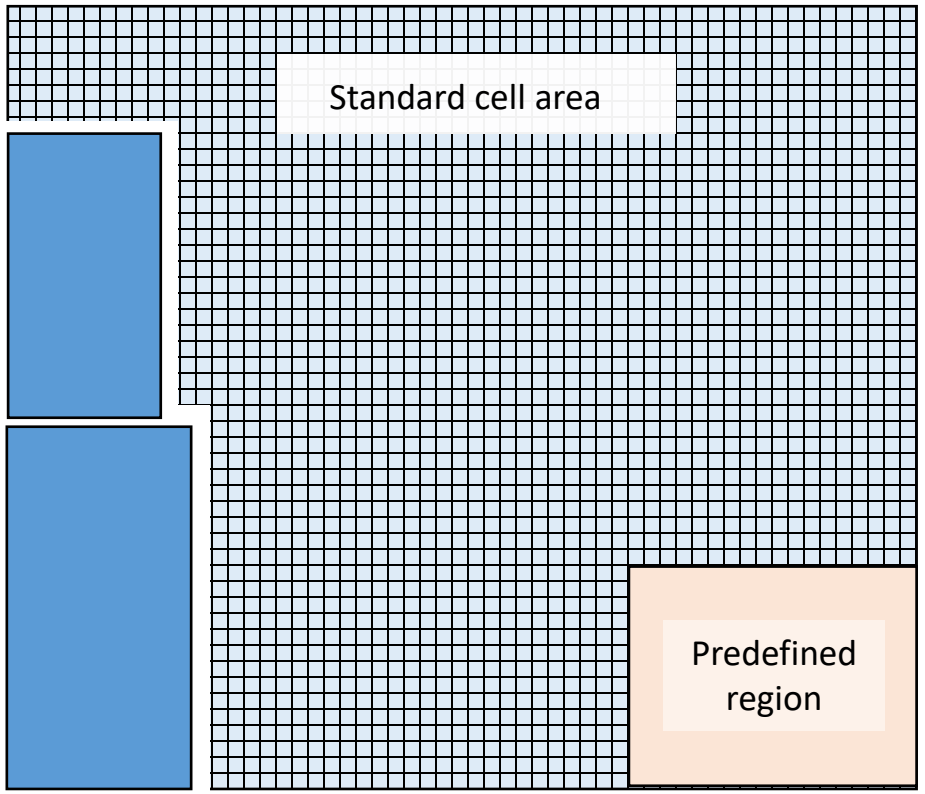


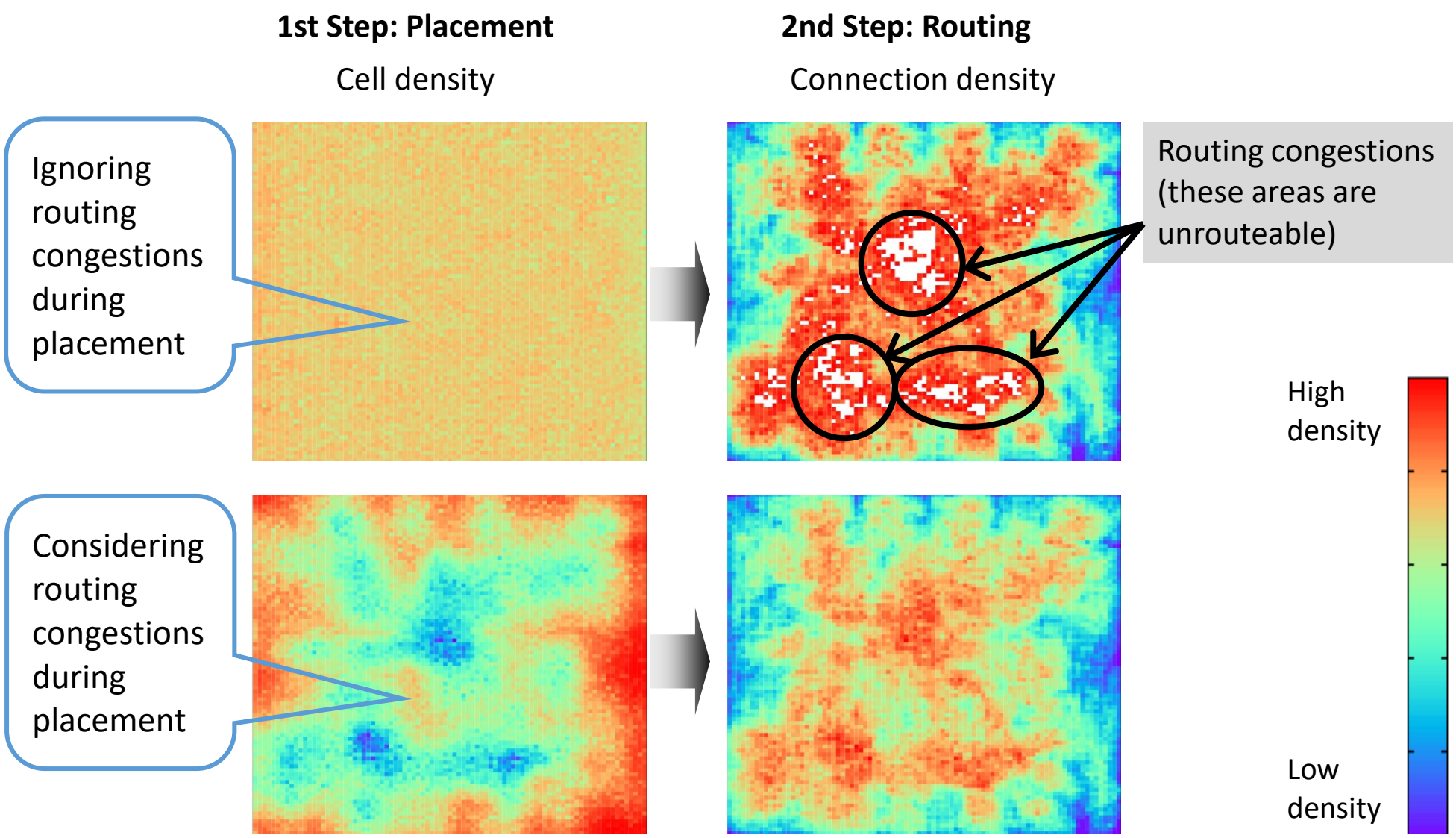


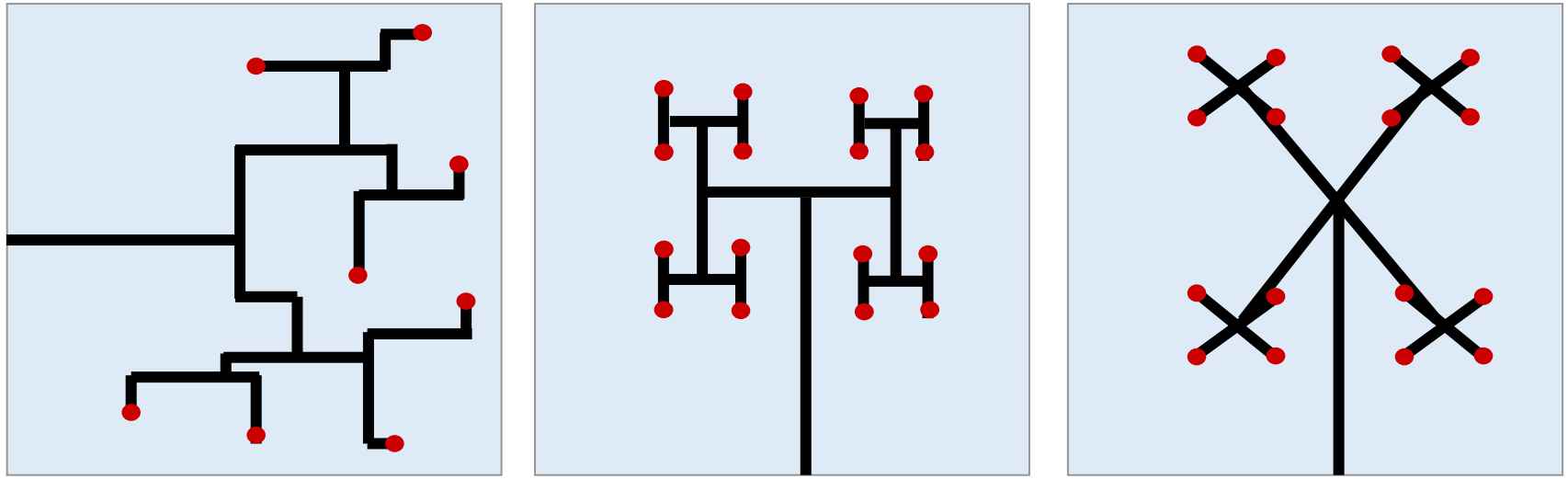




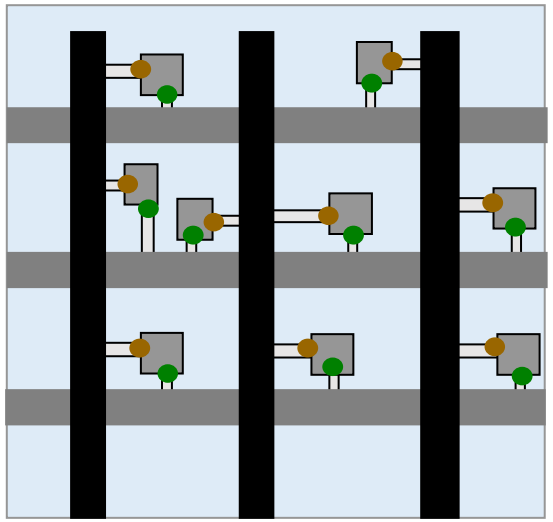




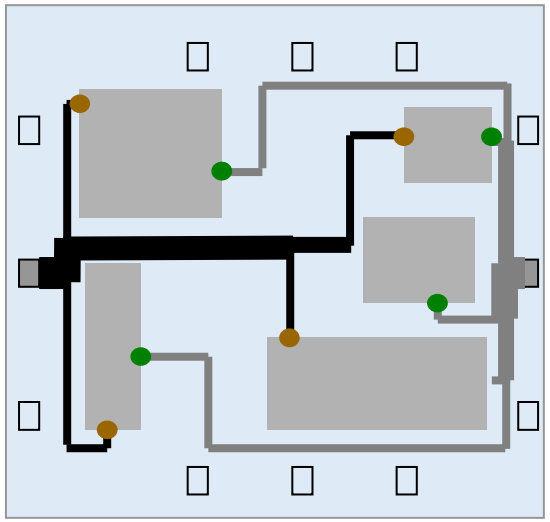




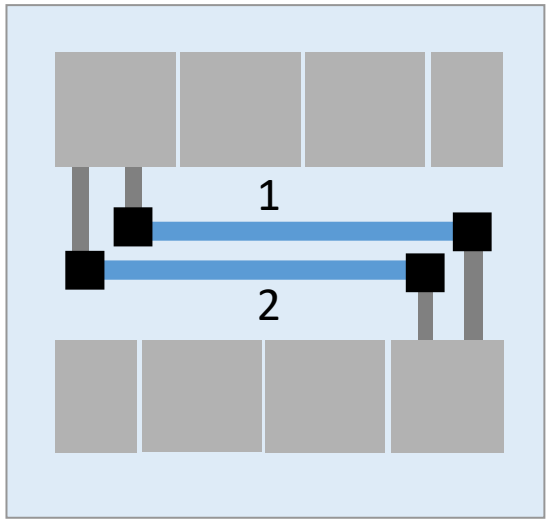
Balanced tree H tree X tree



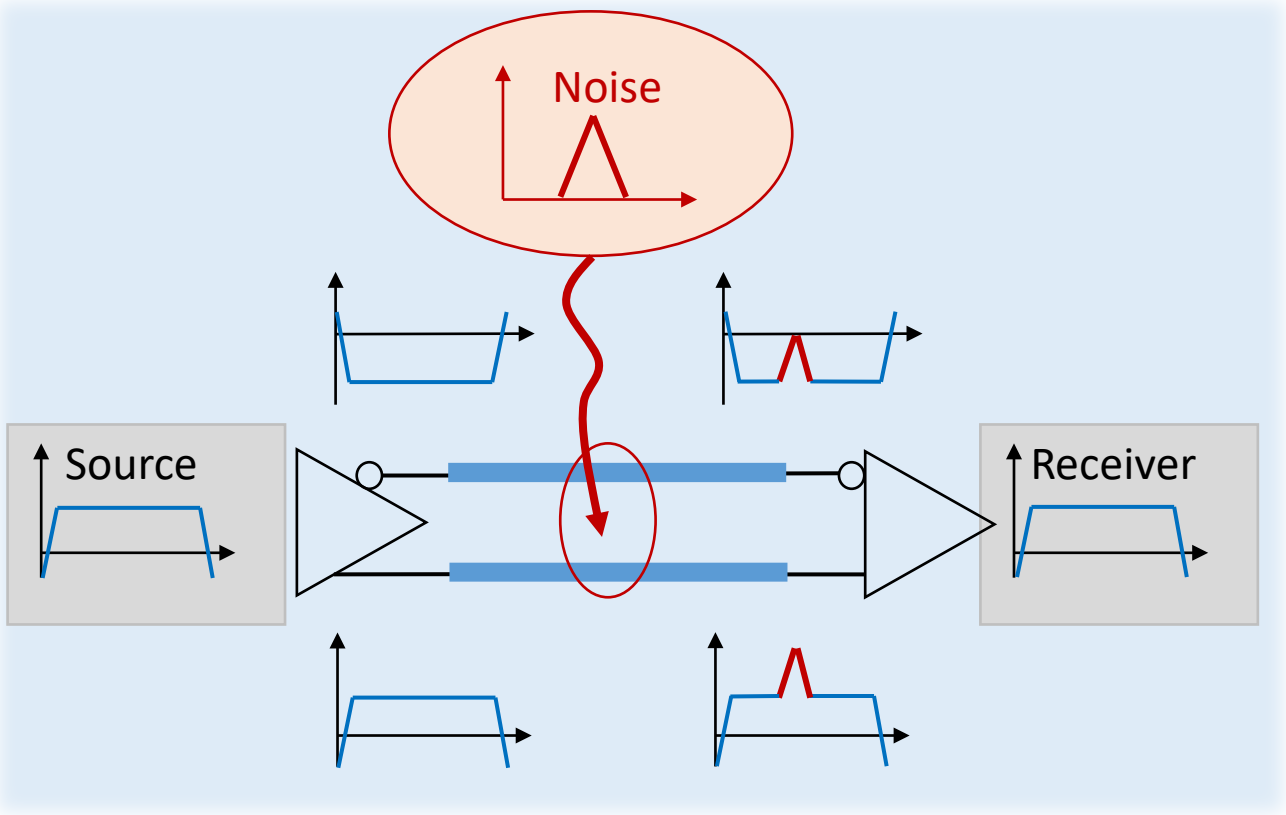
Power mesh



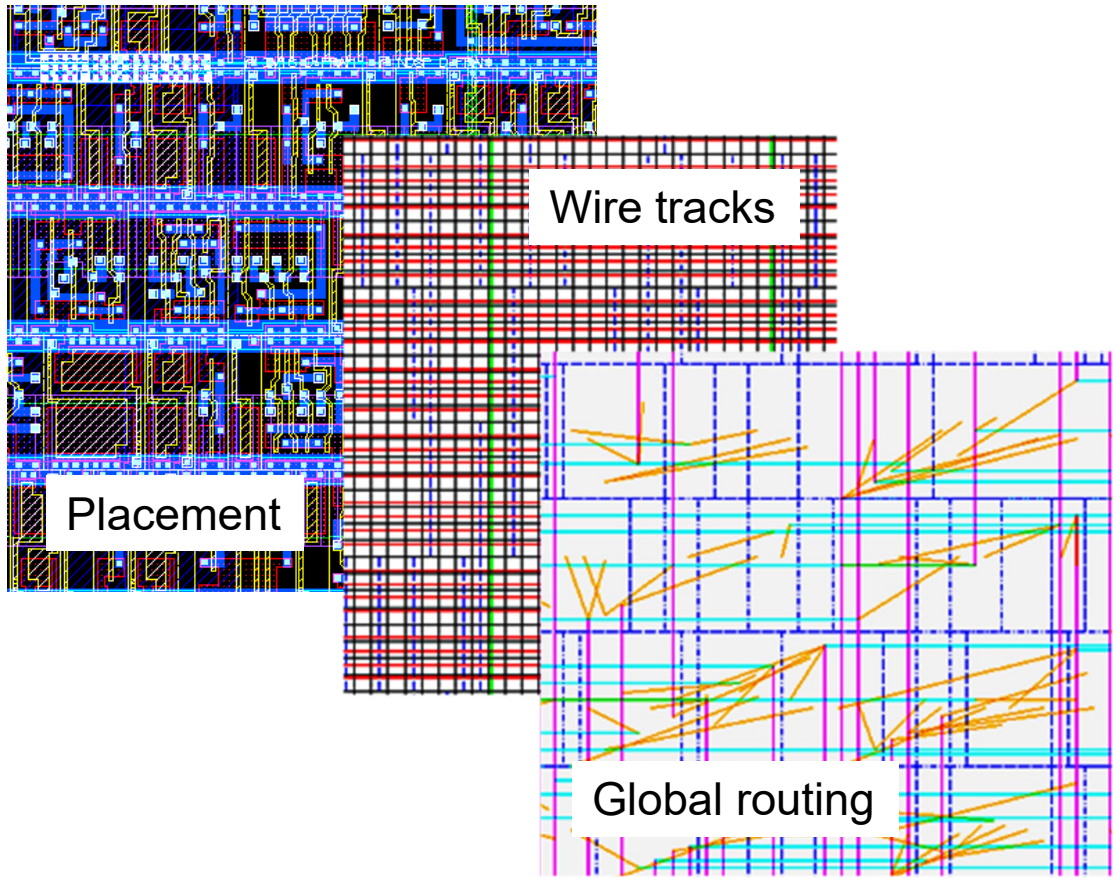
Power tree

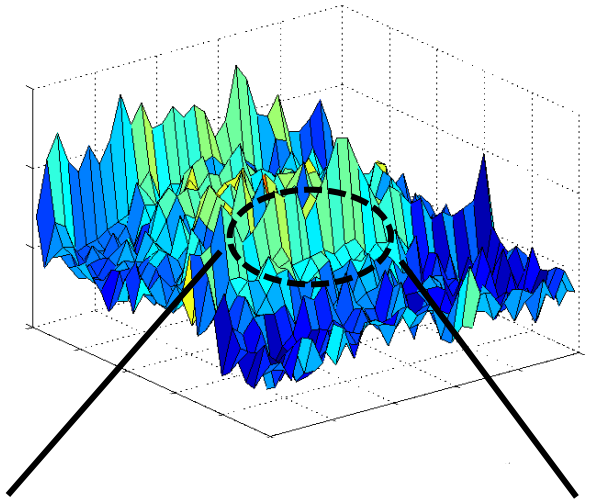


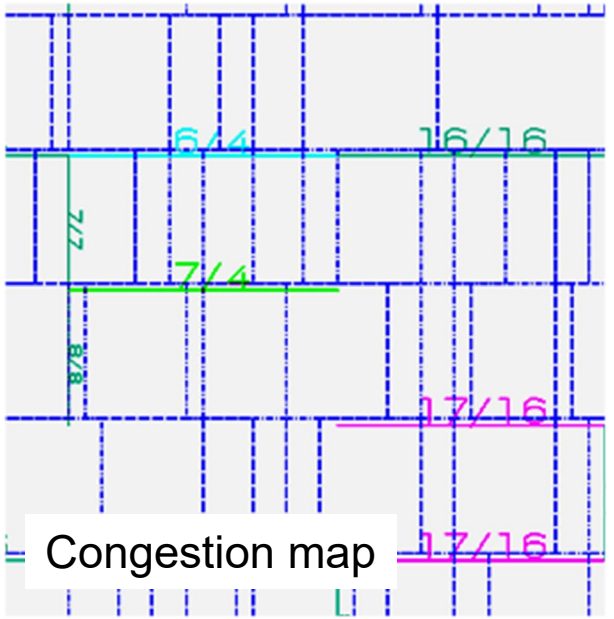
Differential signaling

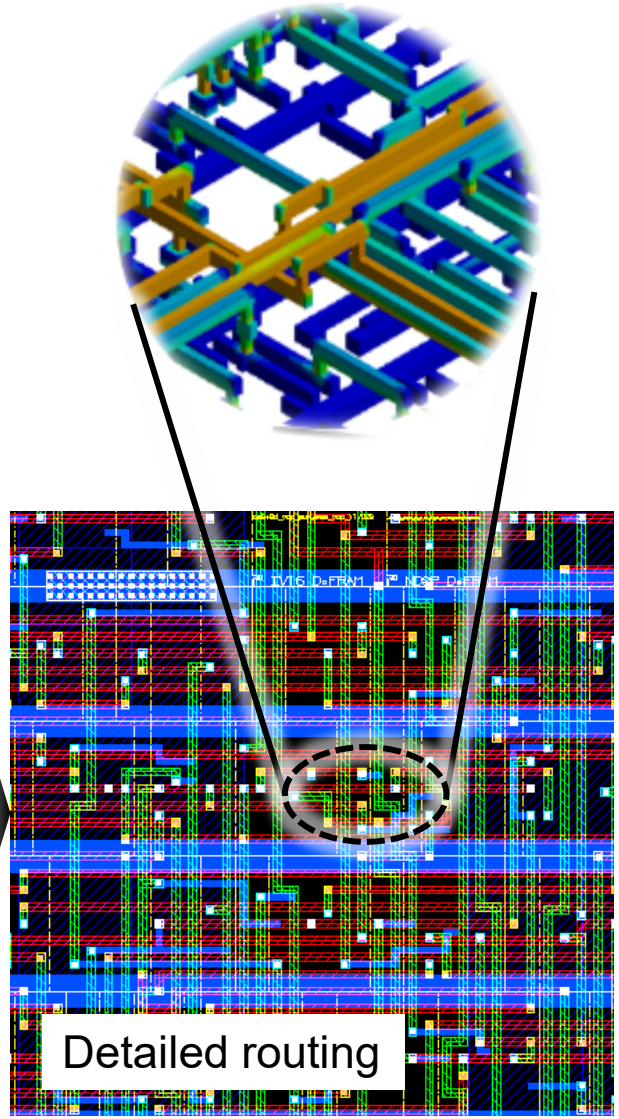


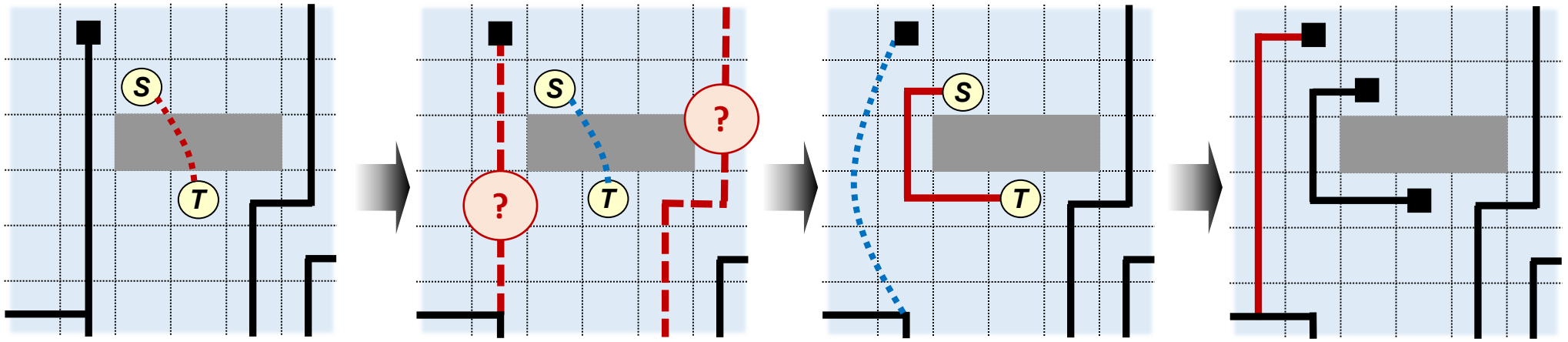
$(R_1, C_1) = (R_2, C_2)$

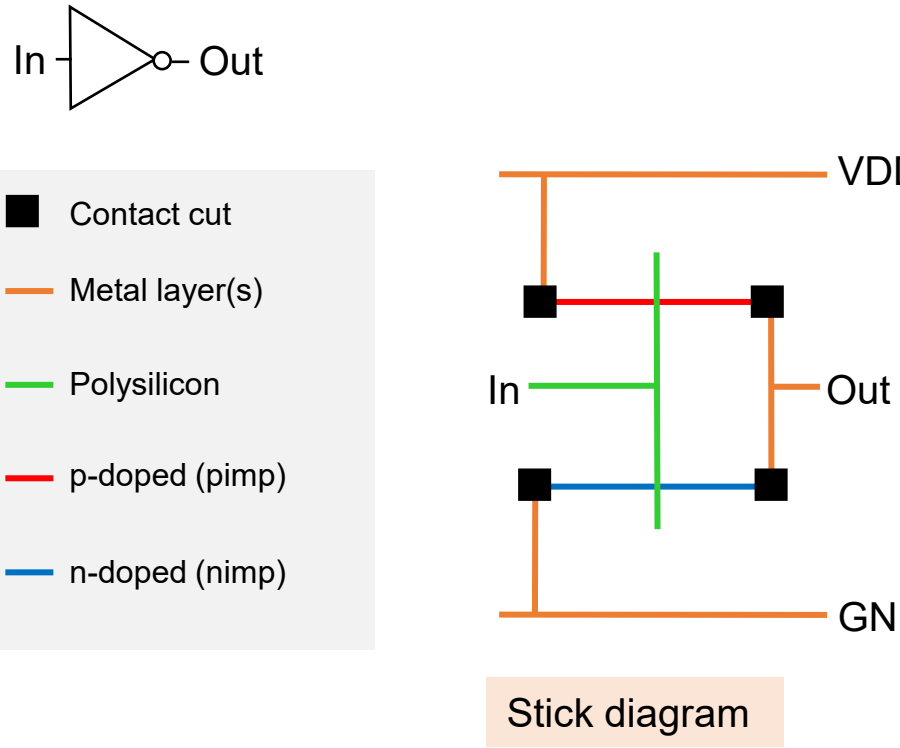


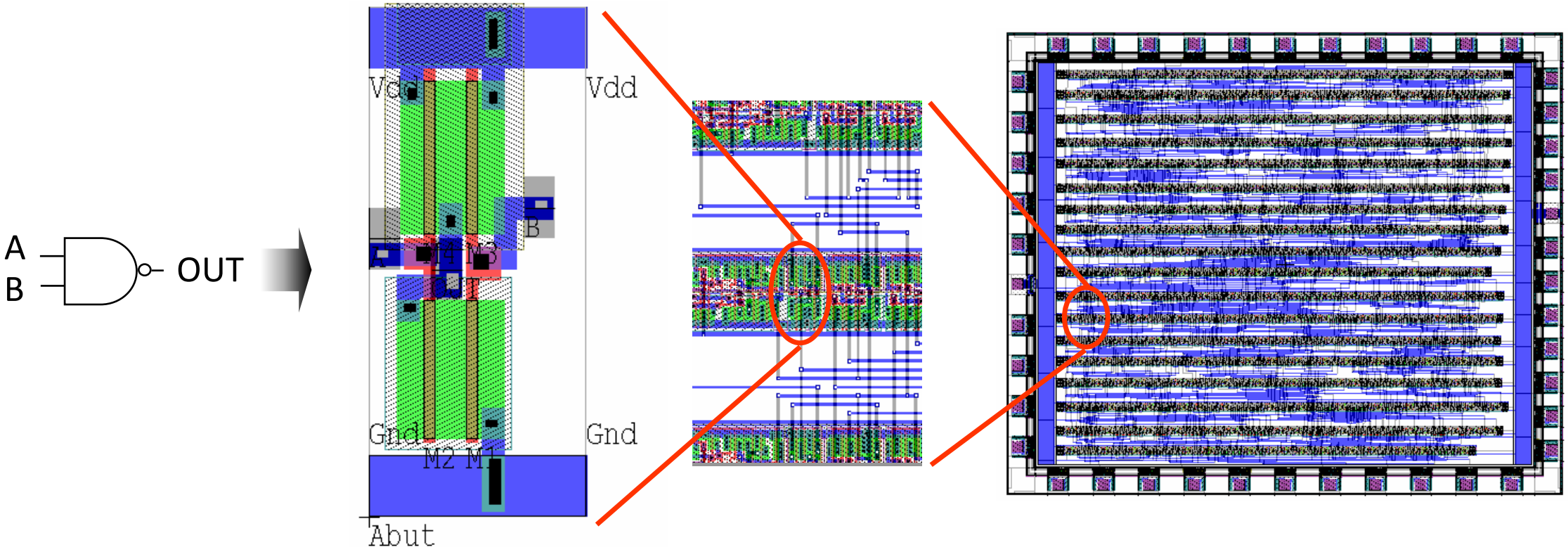


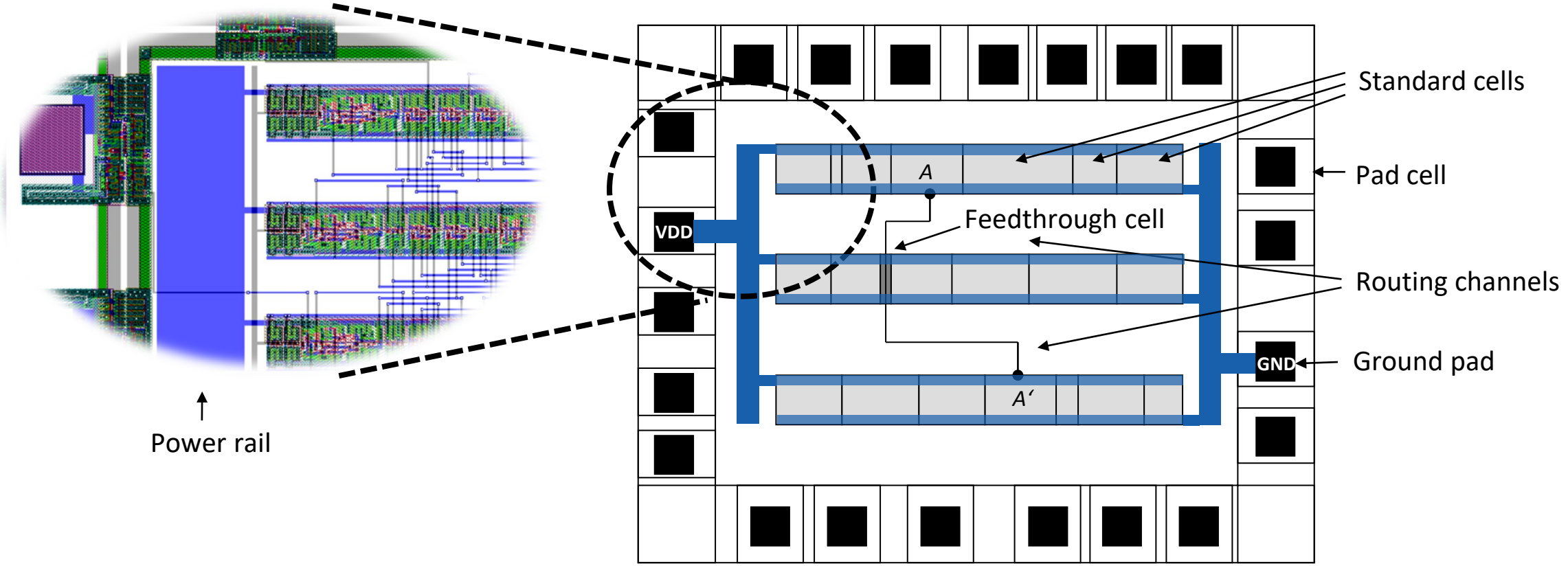


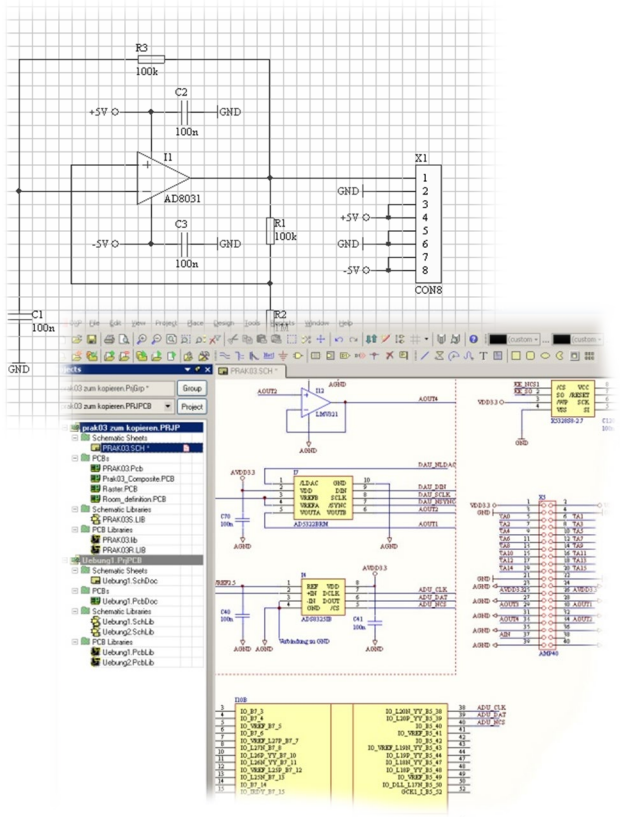




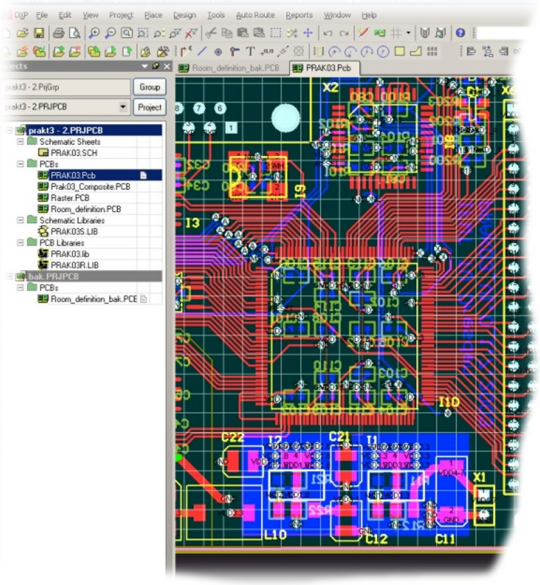




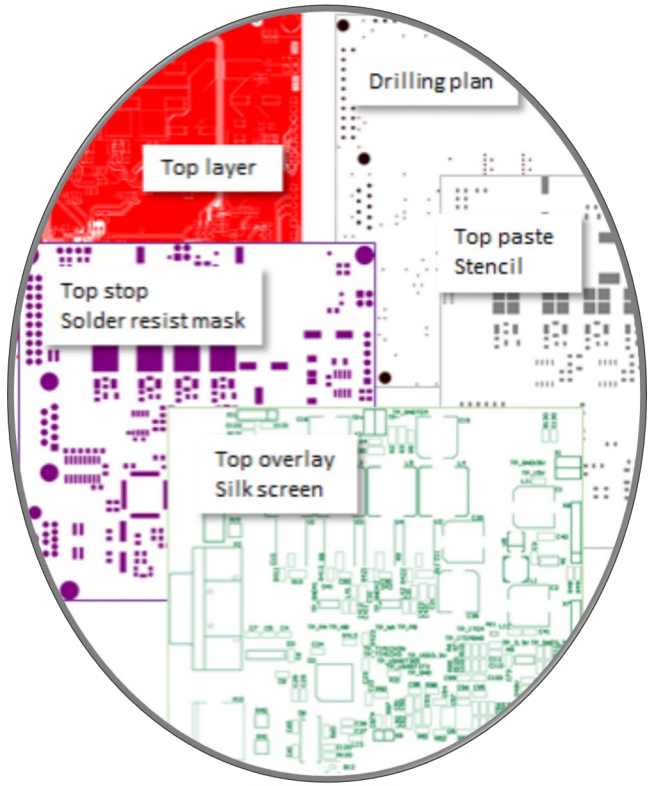




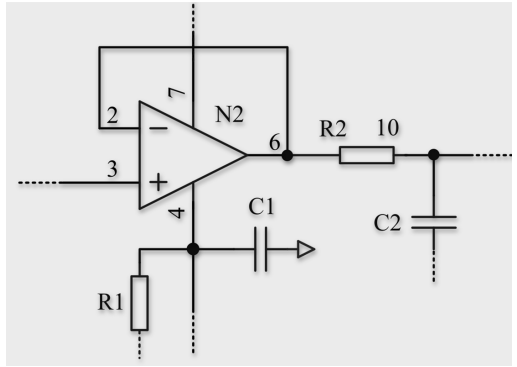
Schematic entry

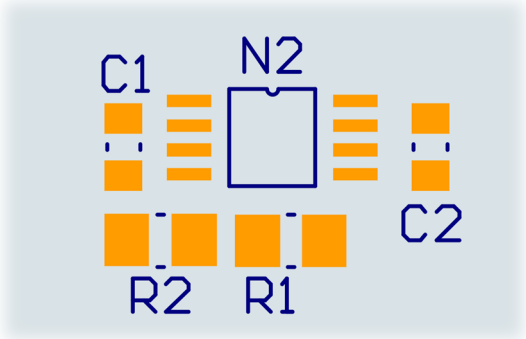


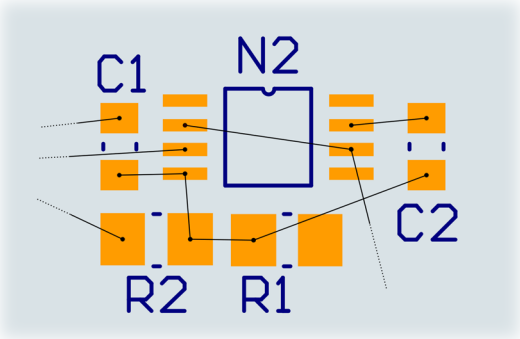
PCB layout generation

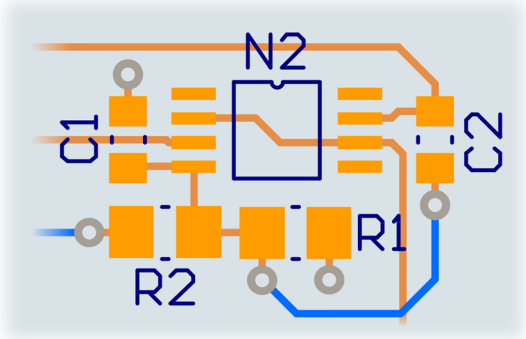


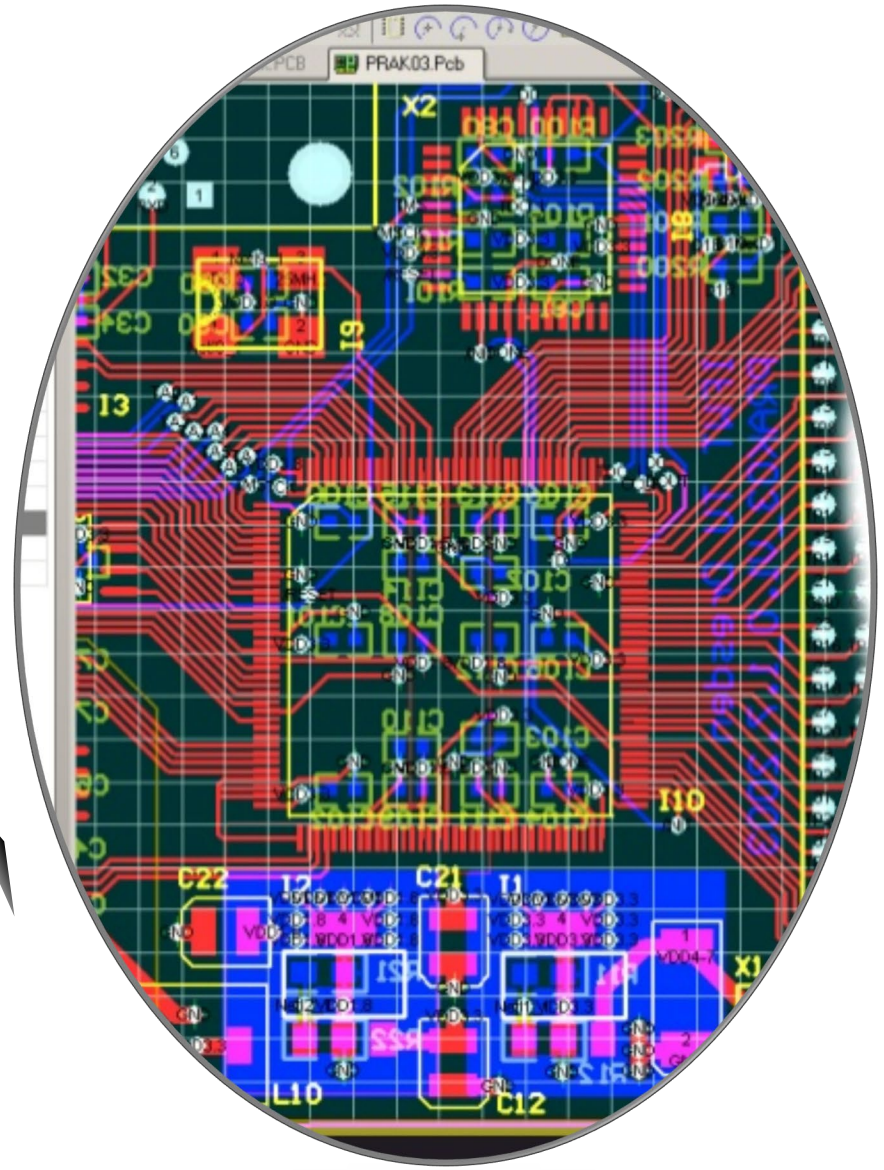
Manufacturing documentation





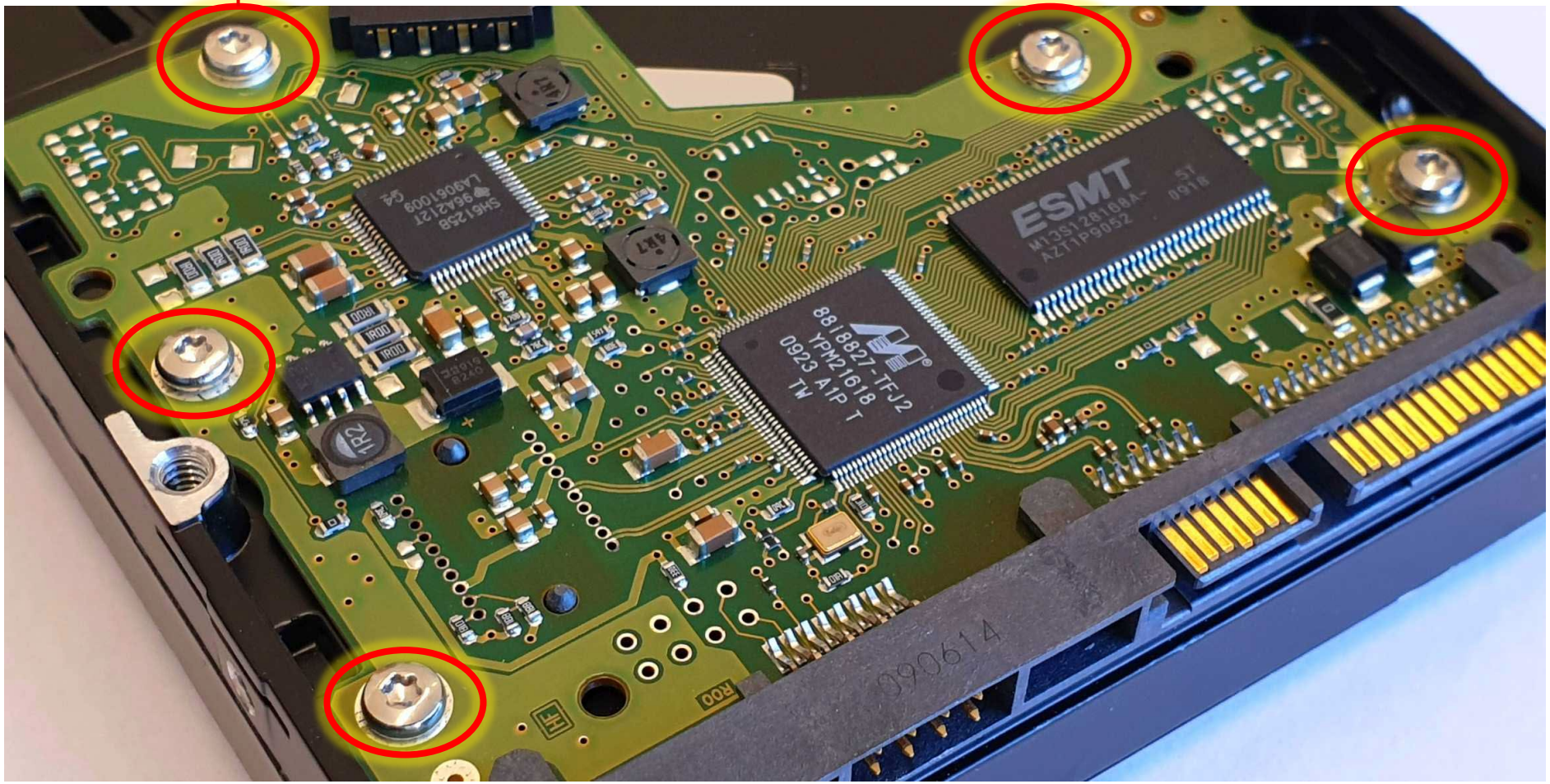


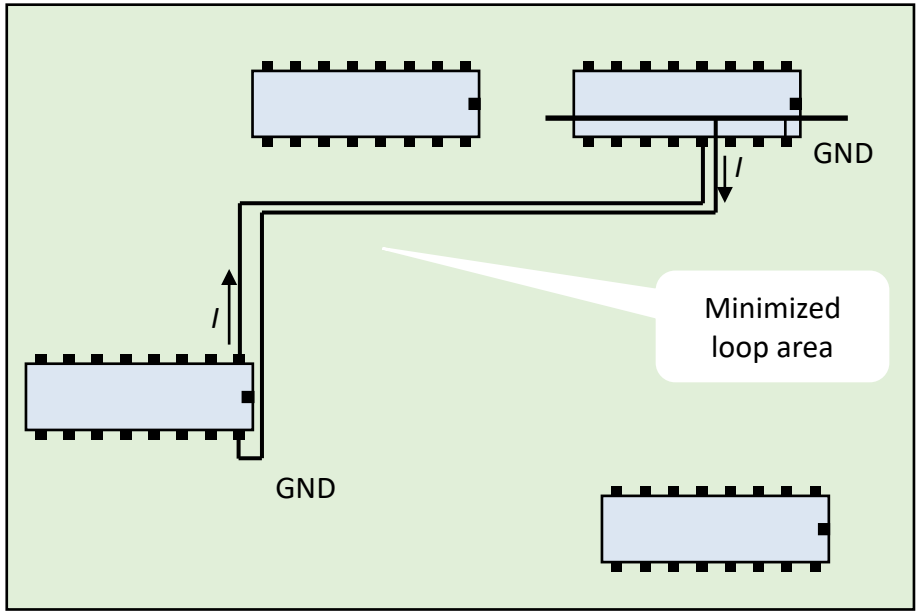


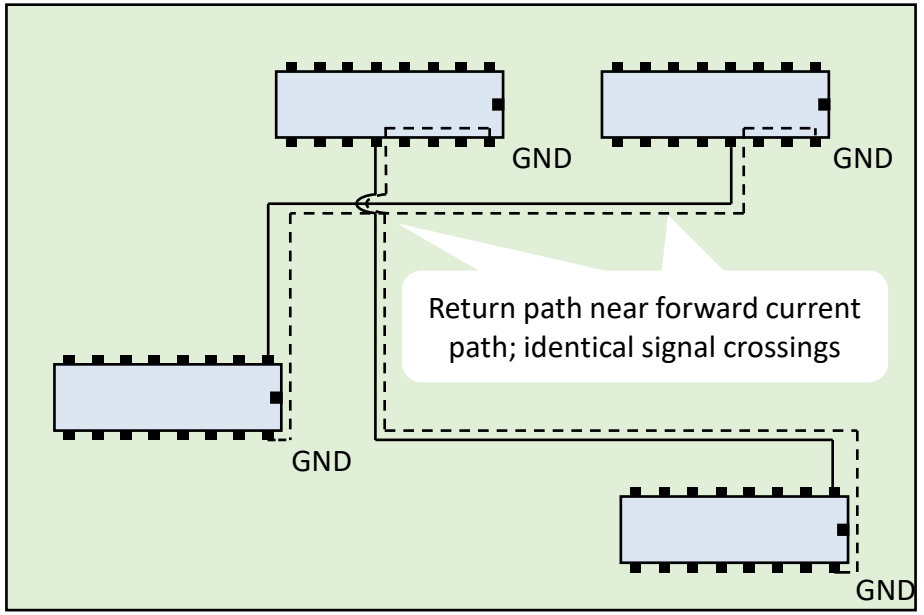


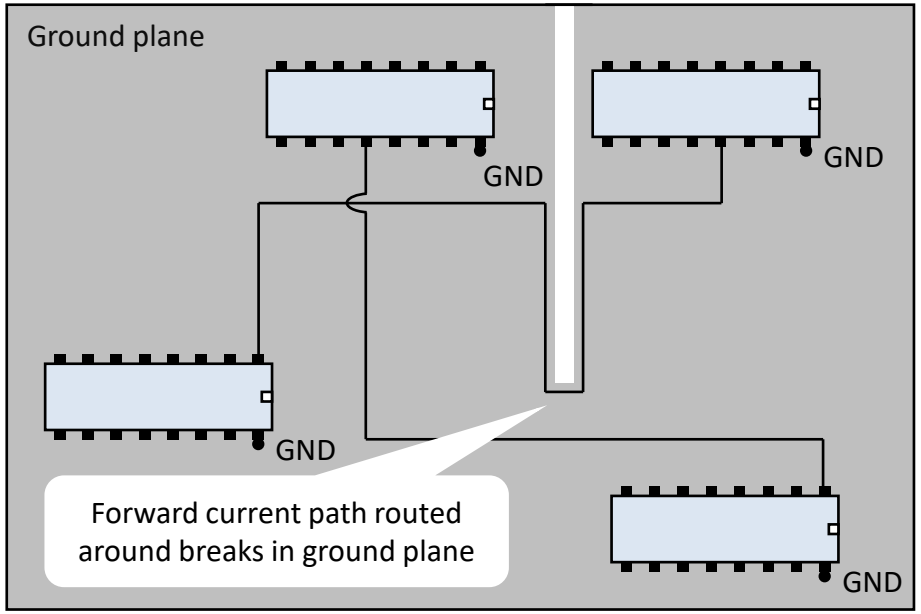
PCB layout

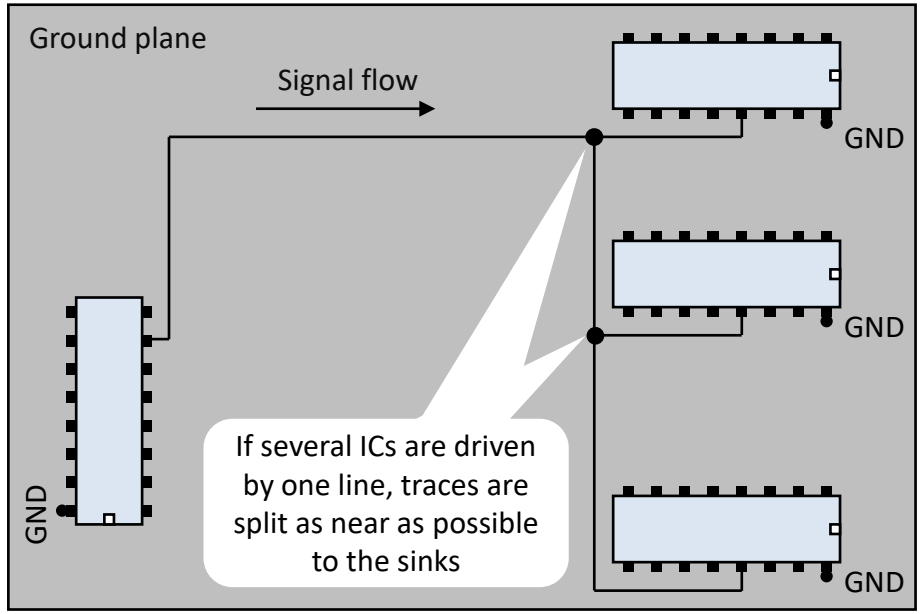
Keepout area

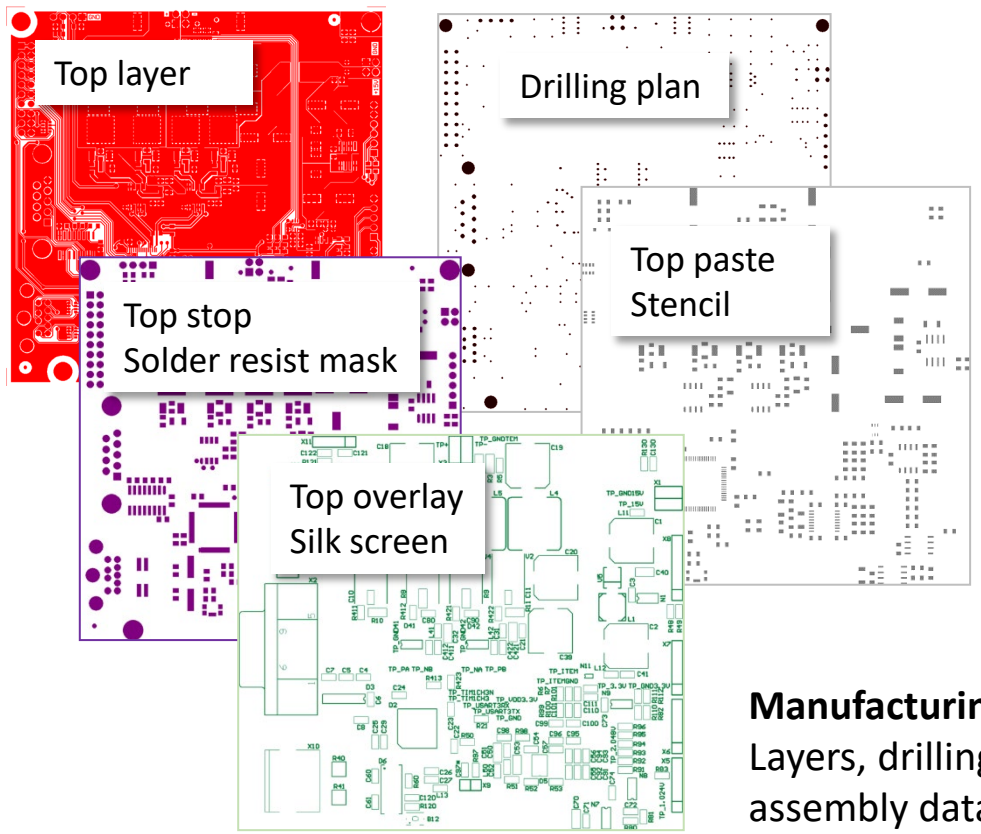




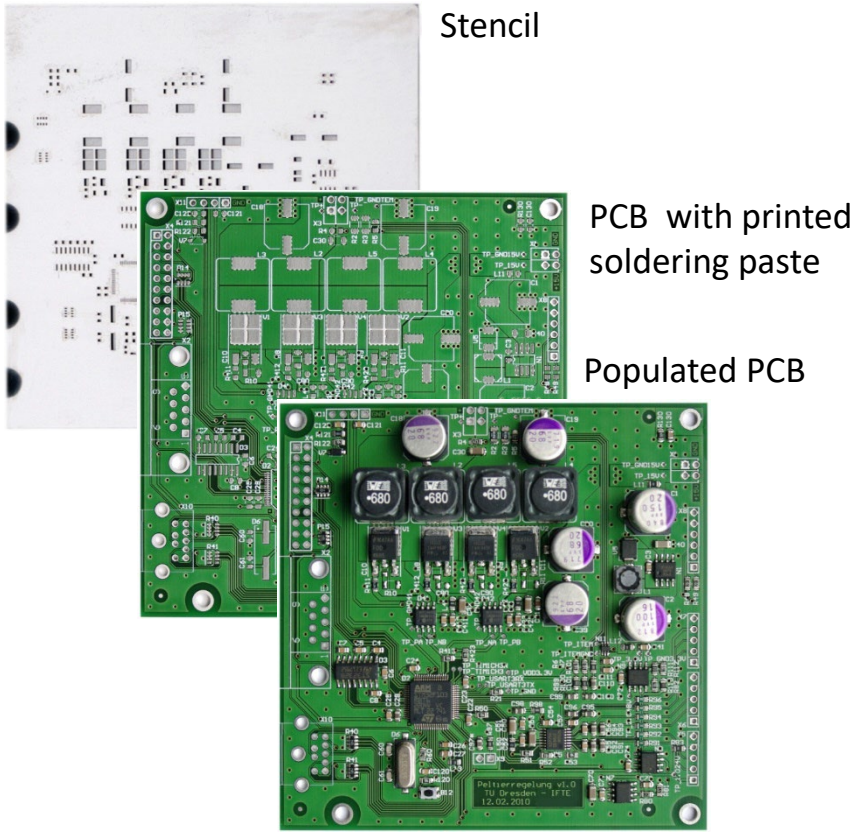


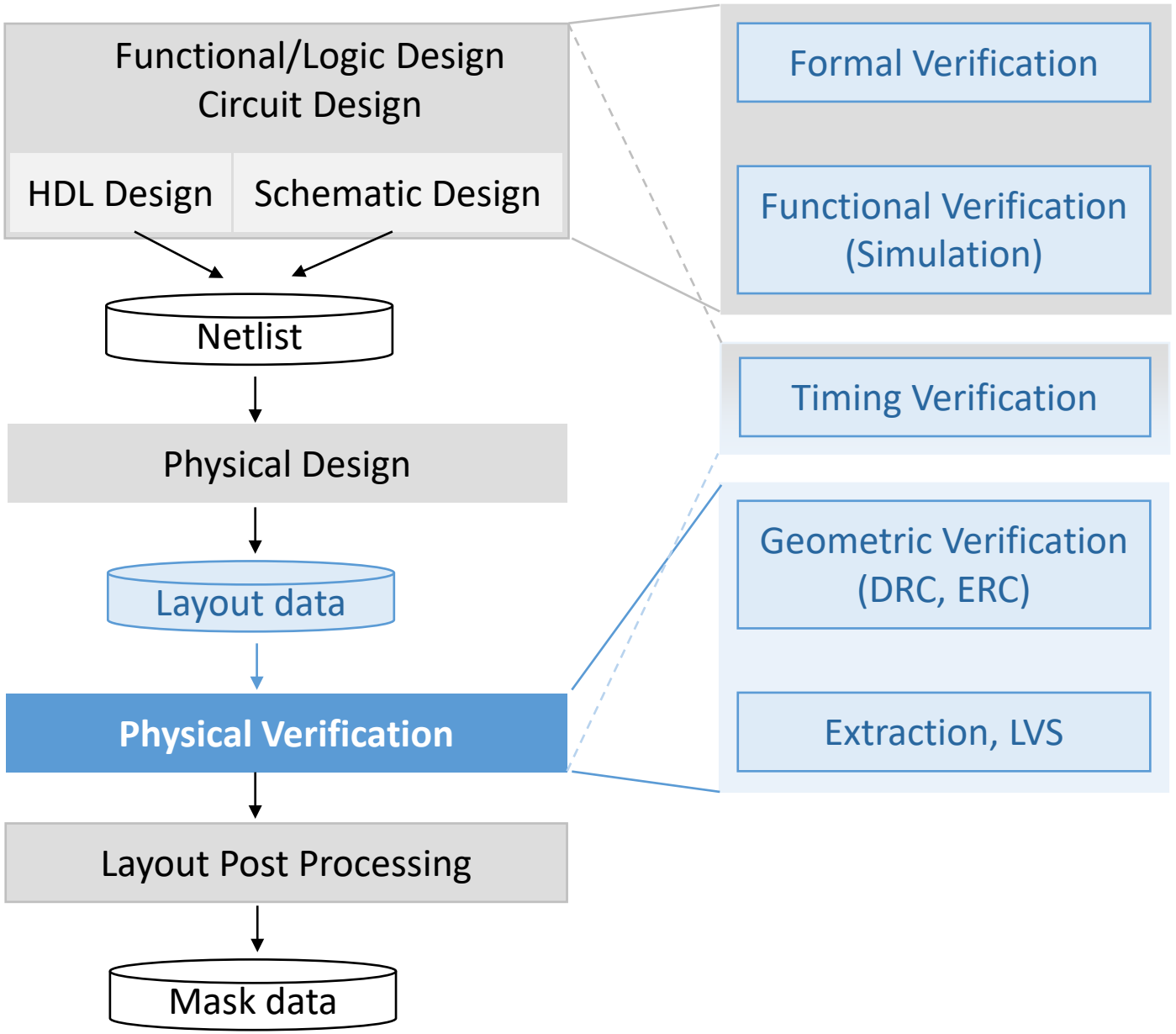


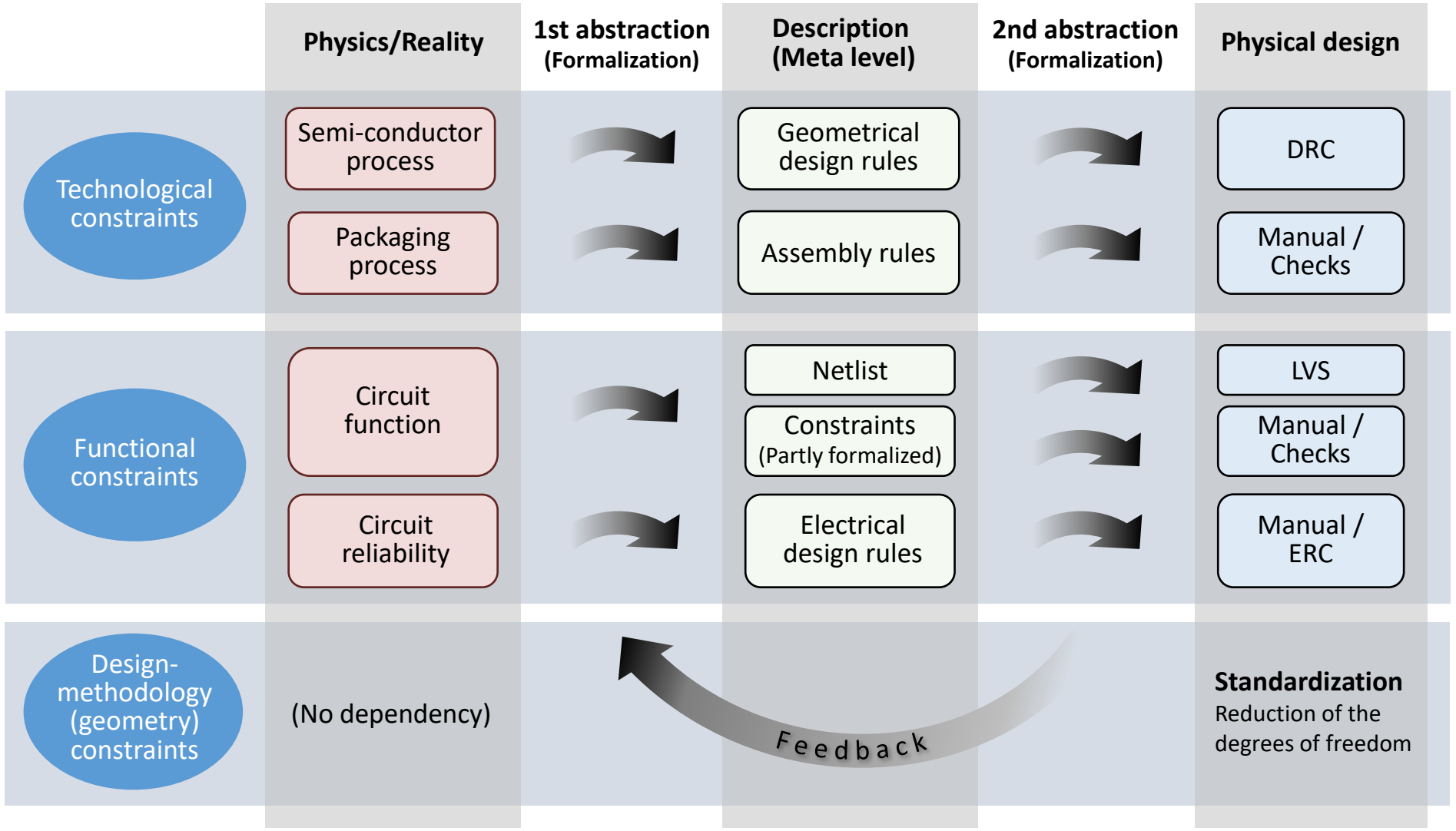




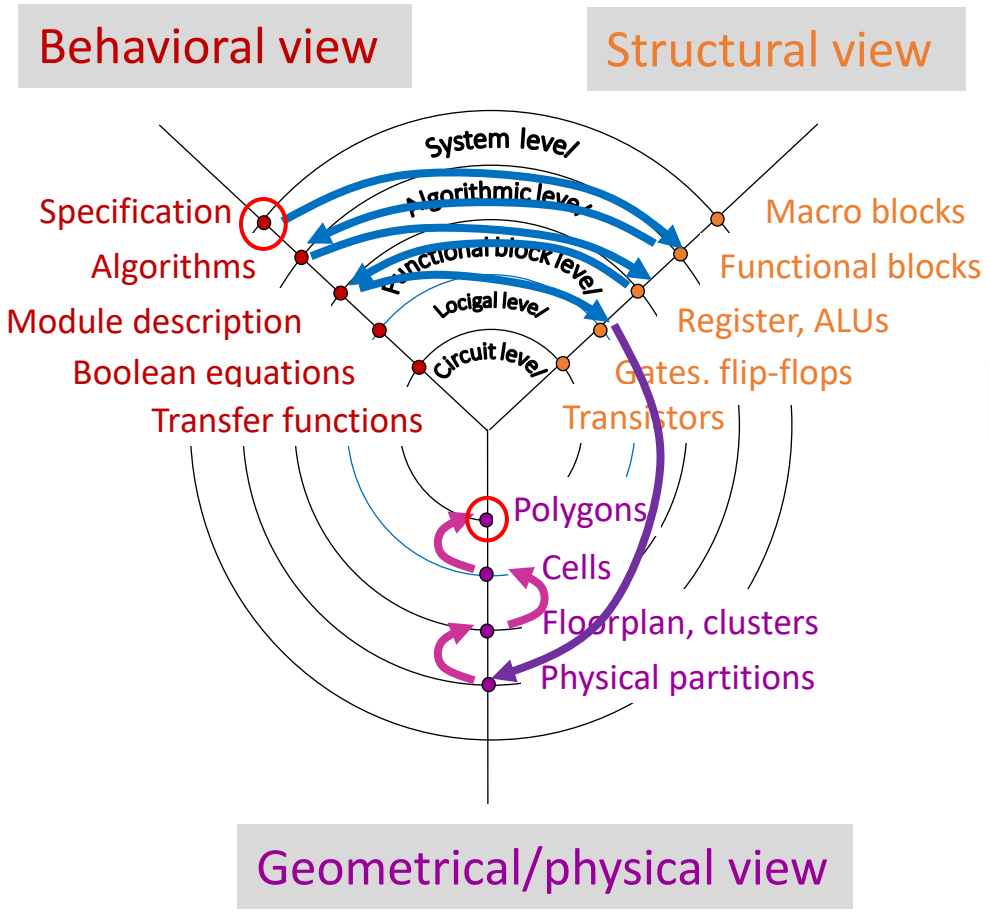
Manufacturing files
Layers, drilling data, assembly data, etc.

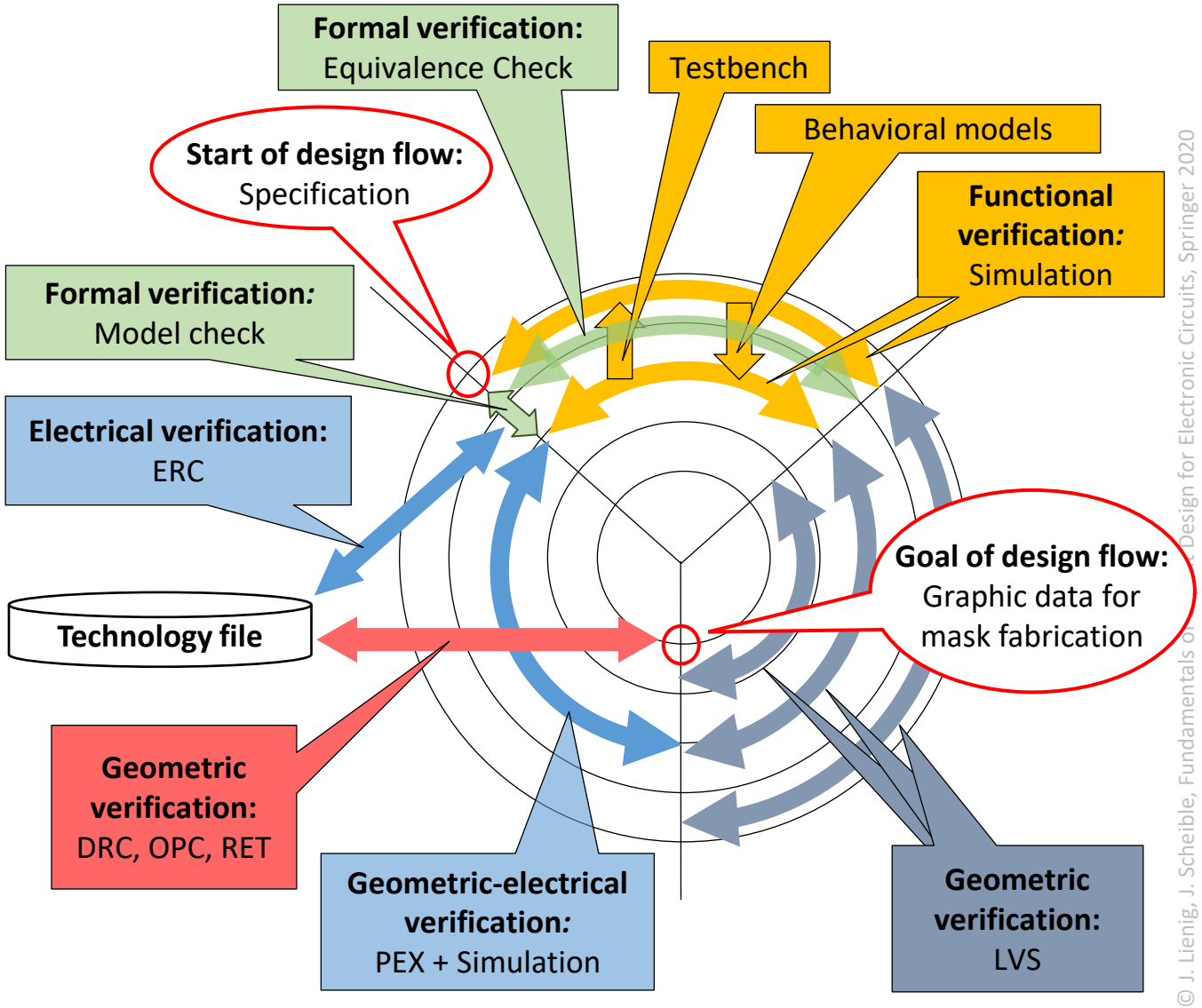


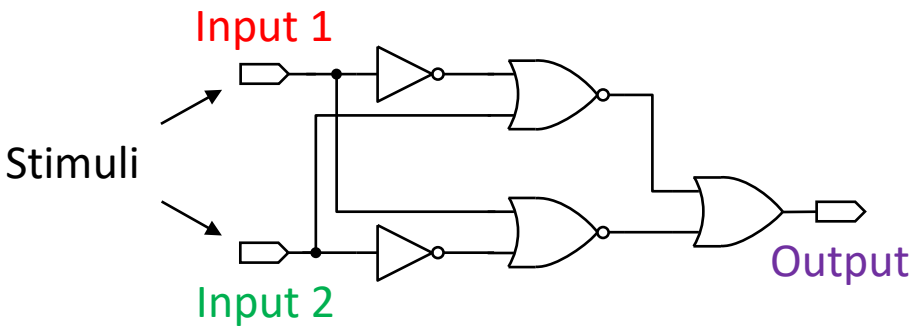




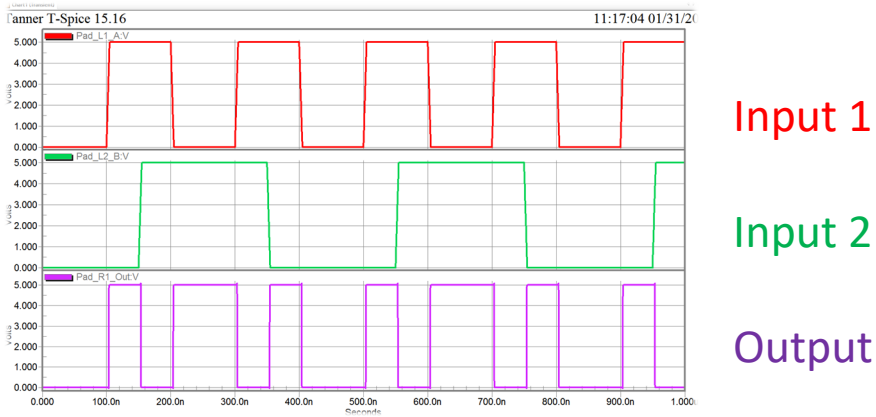
Check	What is checked?	How is it checked?	Method
Model check	Logical characteristic (Assumption is true?)	Mathematical models	Formal verification
Equivalence check	Logical equivalence of two descriptions	Mathematical models	Formal verification
Simulation	Circuit behavior vs. specification	Virtual experiment (stimuli and output)	Functional verification
DRC (OPC, RET)	Layout vs. technological constraints (manufacturability)	Geometrical design rules	Geometric verification
LVS	Layout vs. schematic	Netlist extraction from layout, rule based	Geometric verification
PEX (plus simulation)	Impact of parasitics on circuit behavior	Parameter extraction from layout, rule based; followed by simulation	Geometric and functional verification
ERC	Layout vs. electric process boundaries (reliability)	Connectivity extraction from layout, rule based	Geometric verification
Testing	Compliance for practical usage	Real experiment, customer checking	Validation

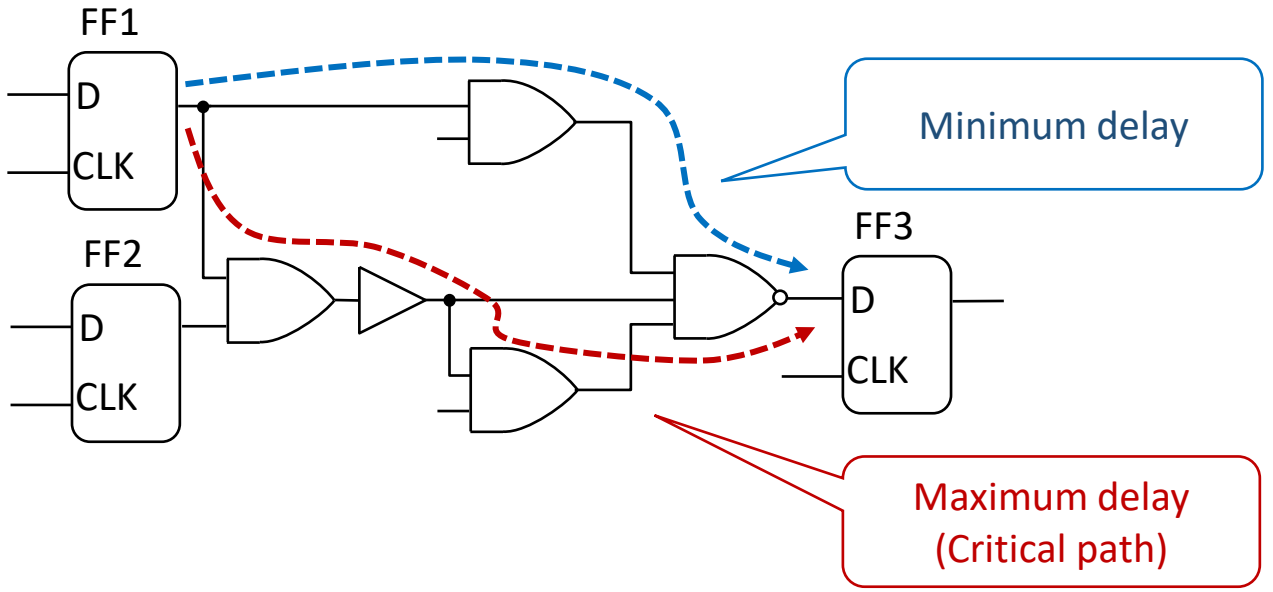


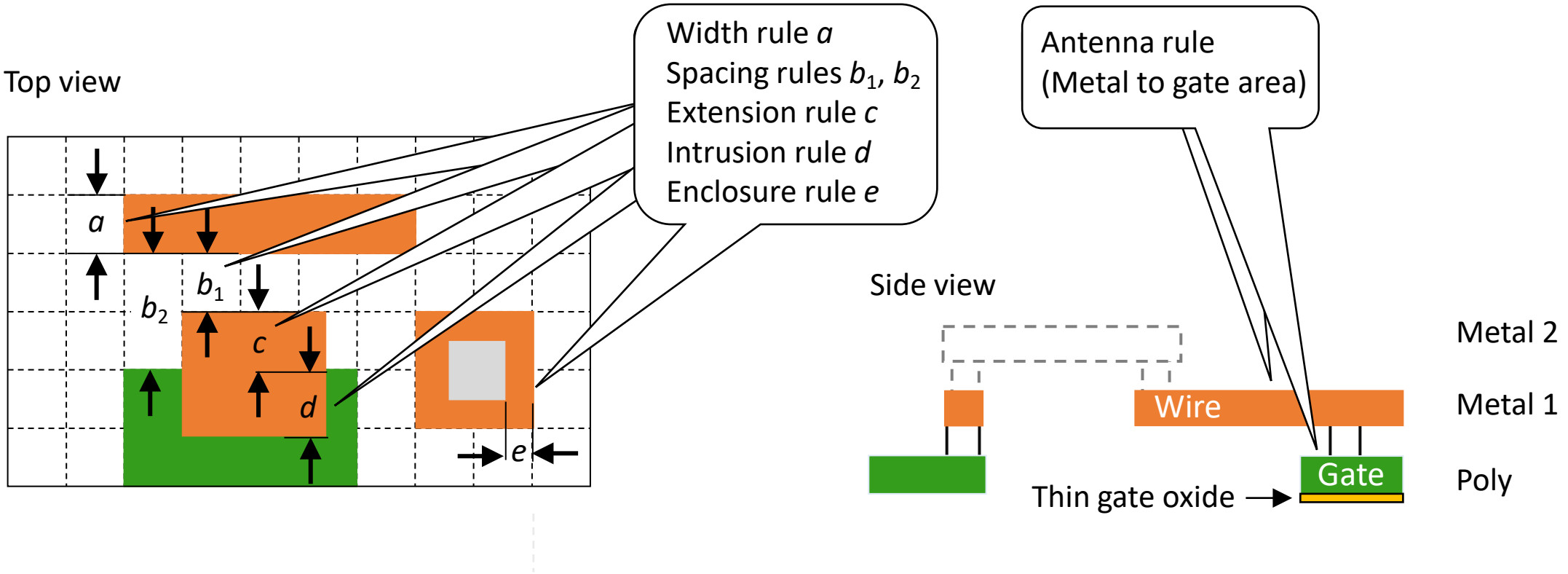


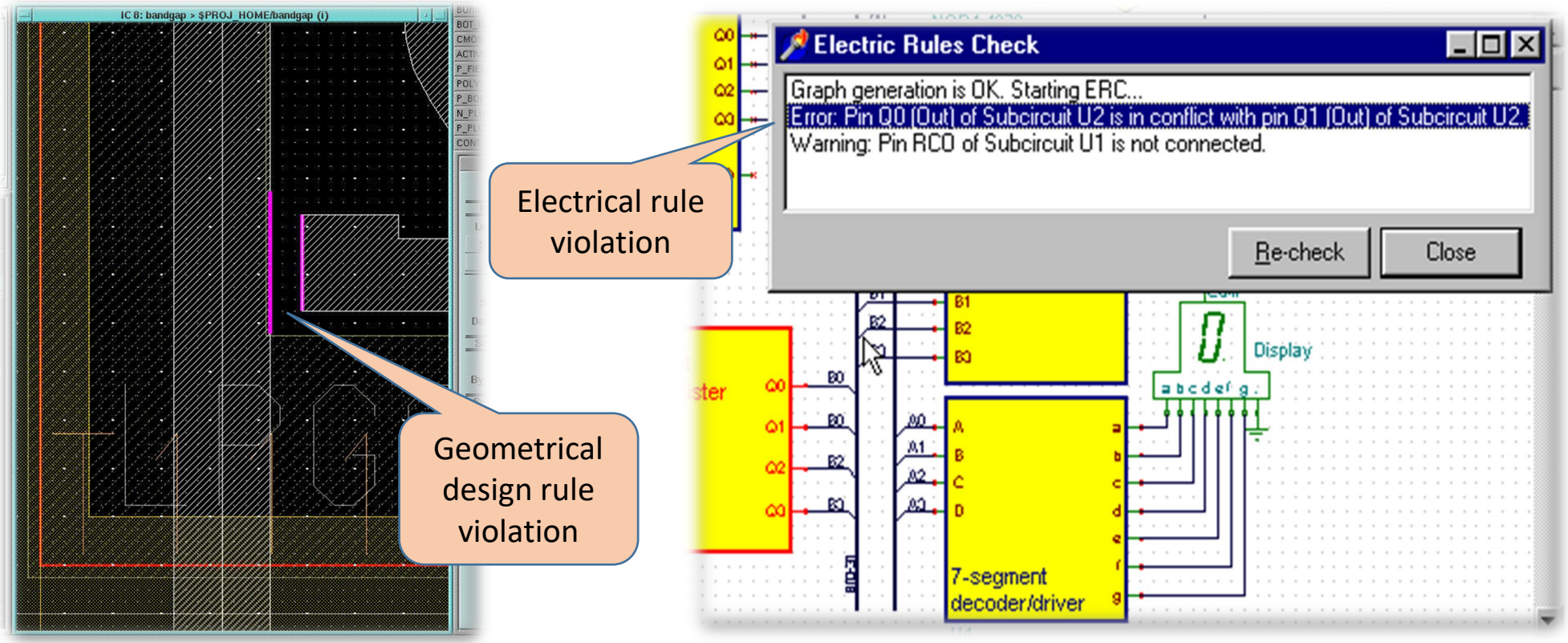


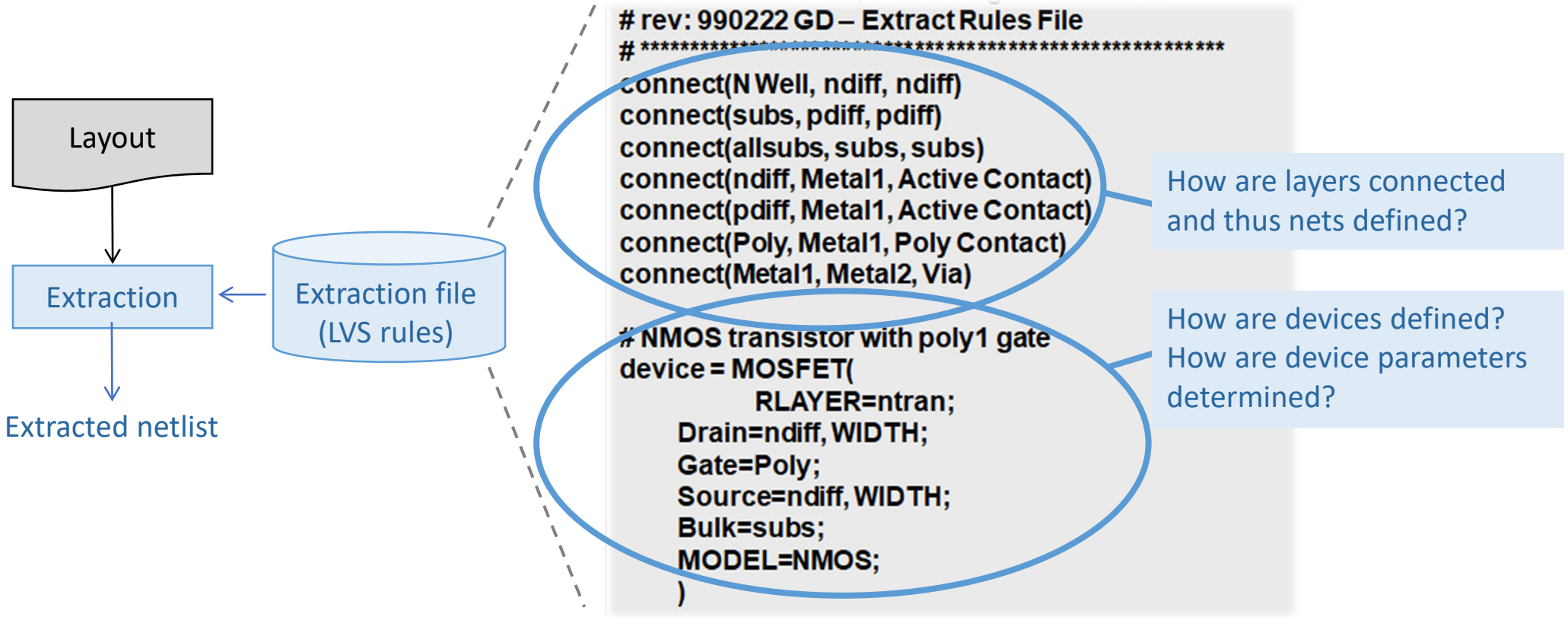
XOR gate

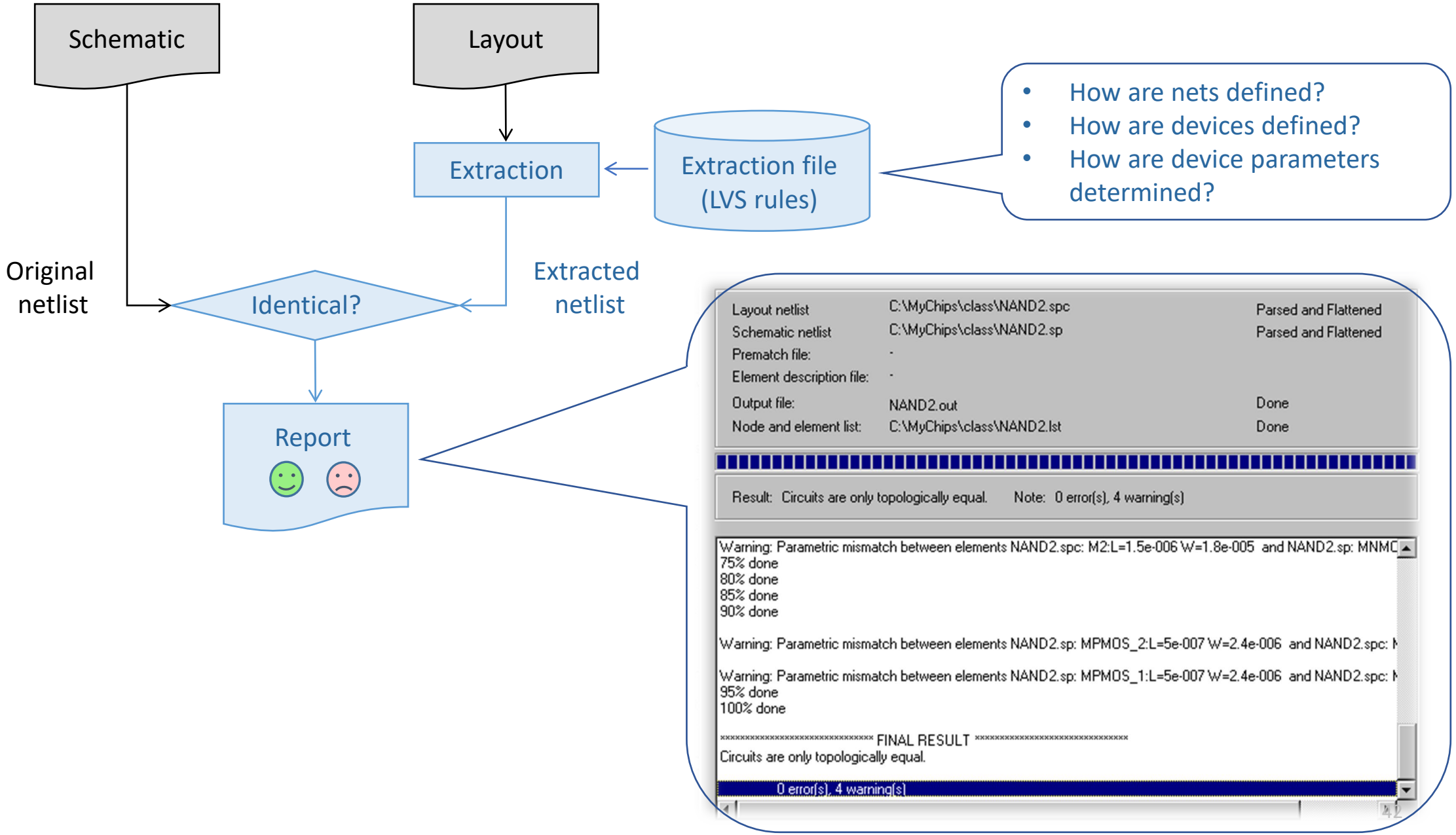


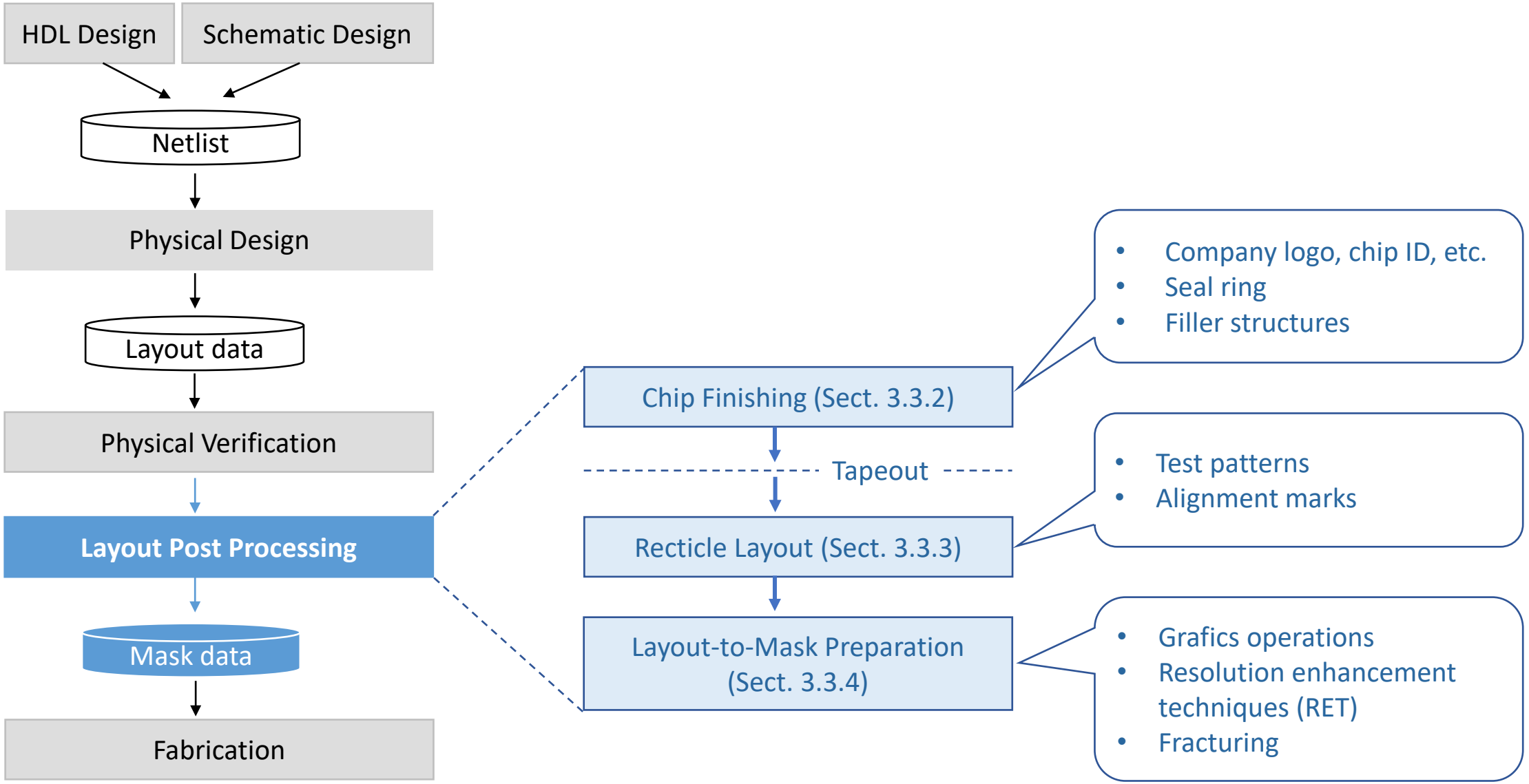


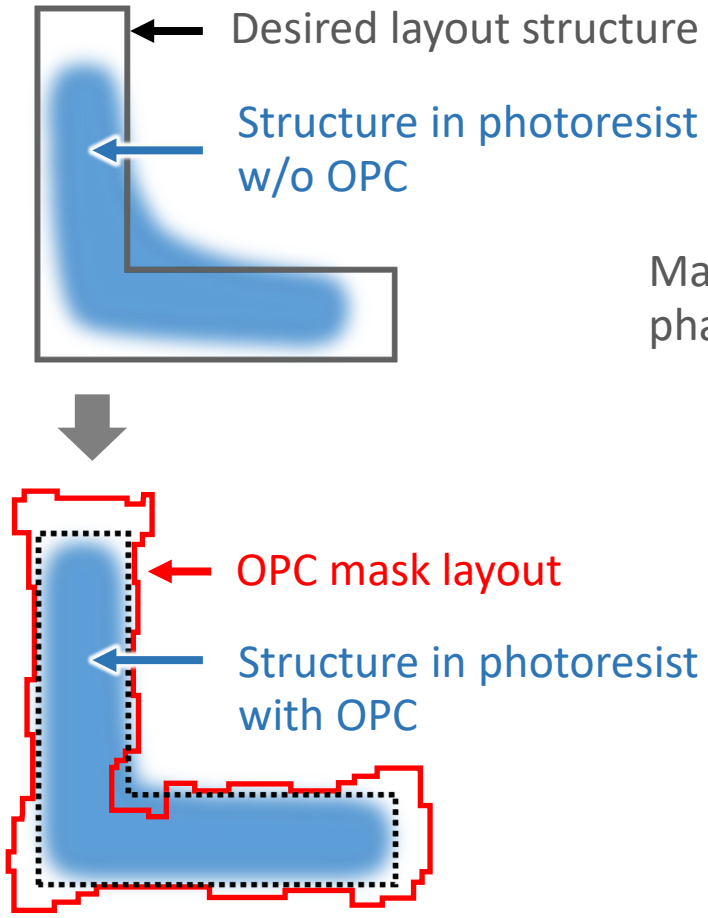




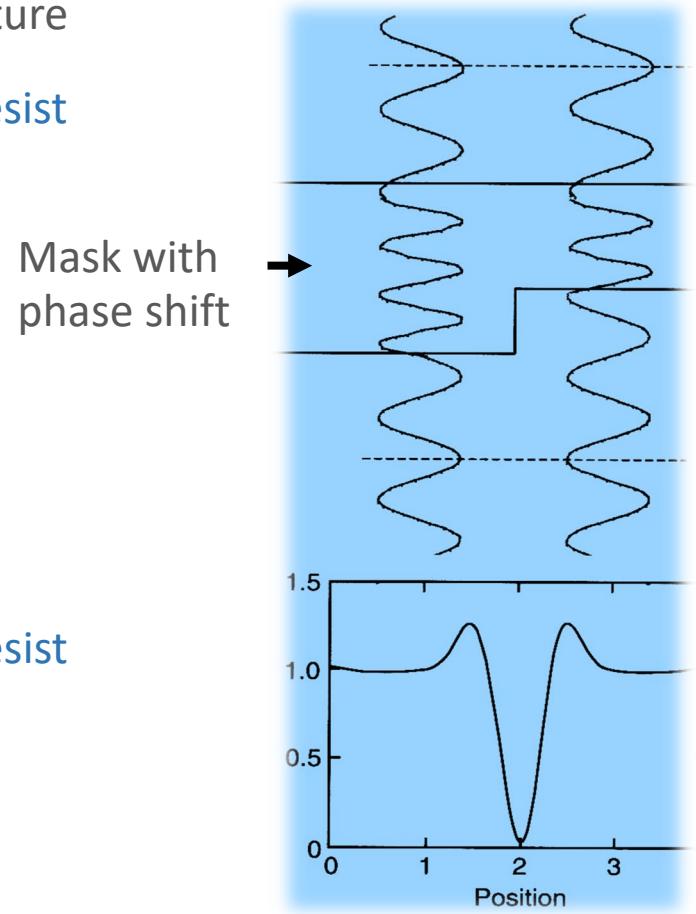




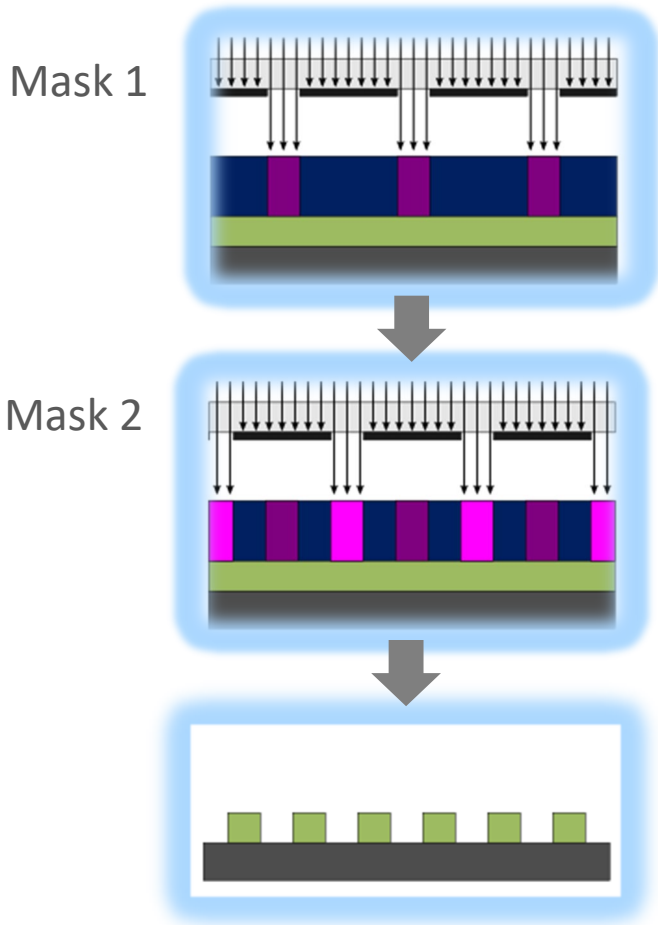




Optical Proximity Correction (OPC)



Phase Shift Mask



Double Patterning