Chapter 3: Bridges to Technology: Interfaces, Design Rules, and Libraries

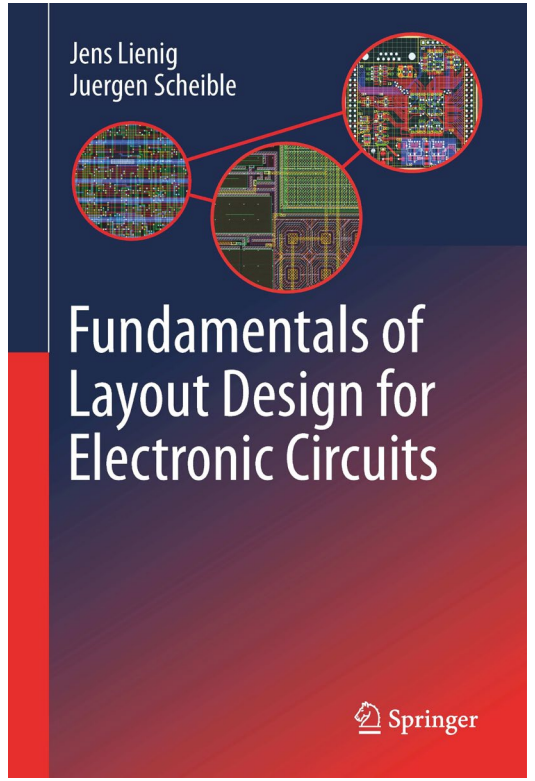
3.1 Circuit Data: Schematic and Netlists

3.2 Layout Data: Layers and Polygons

3.3 Mask Data: Layout Post Processing

3.4 Geometrical Design Rules

3.5 Libraries



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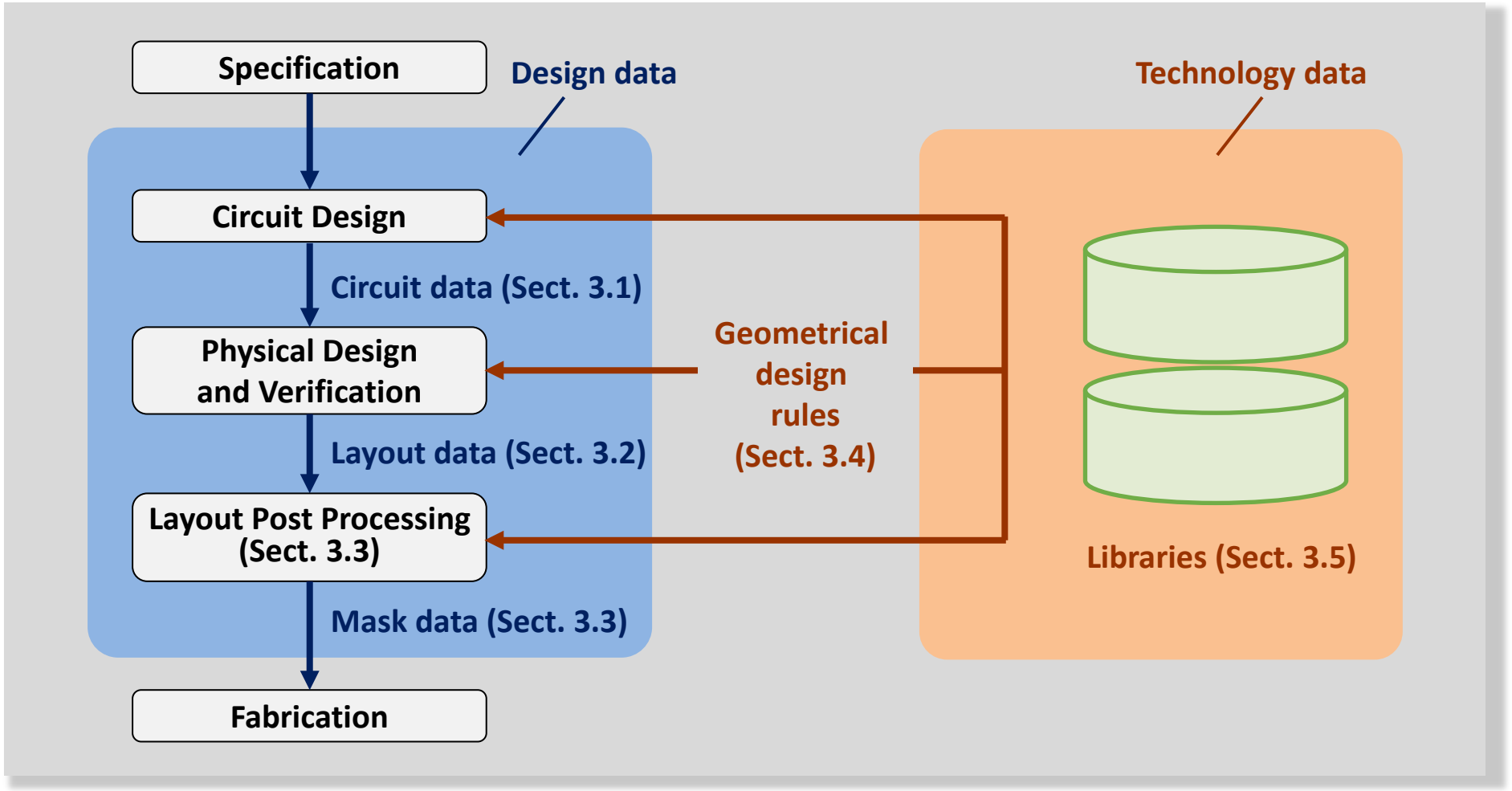
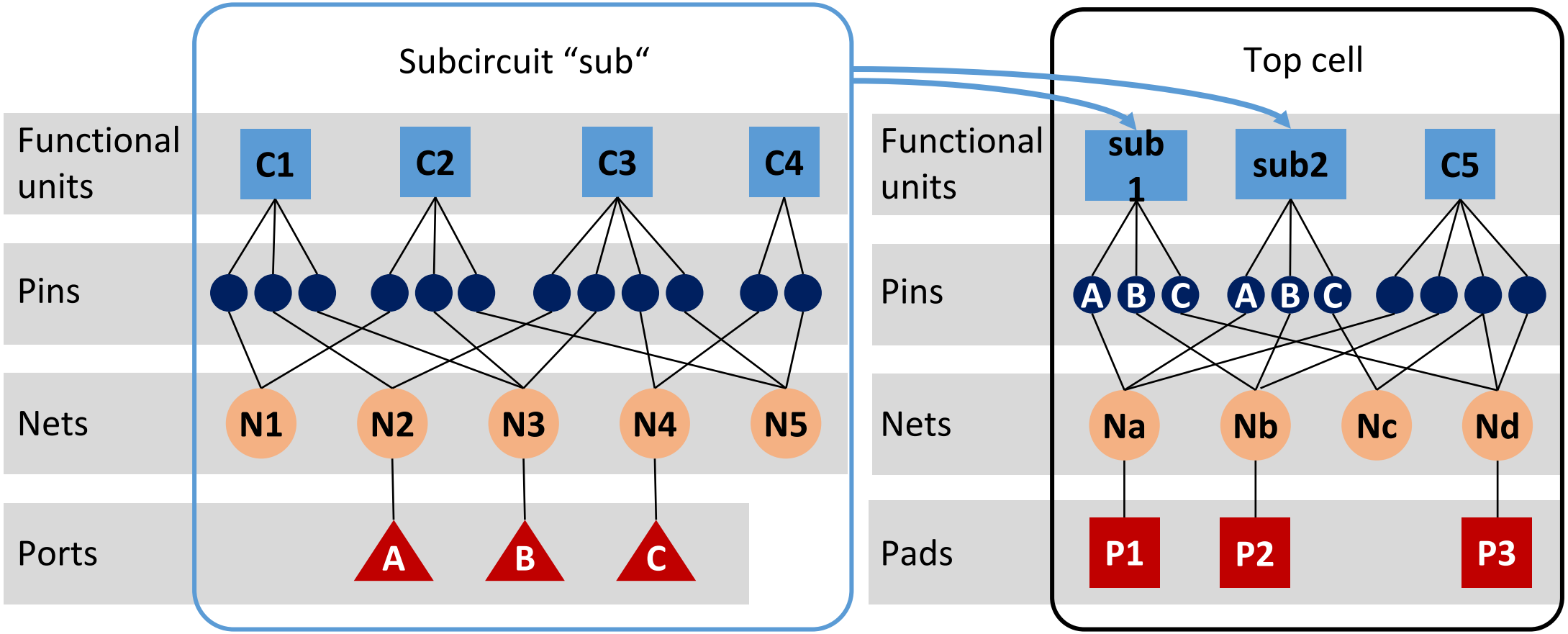
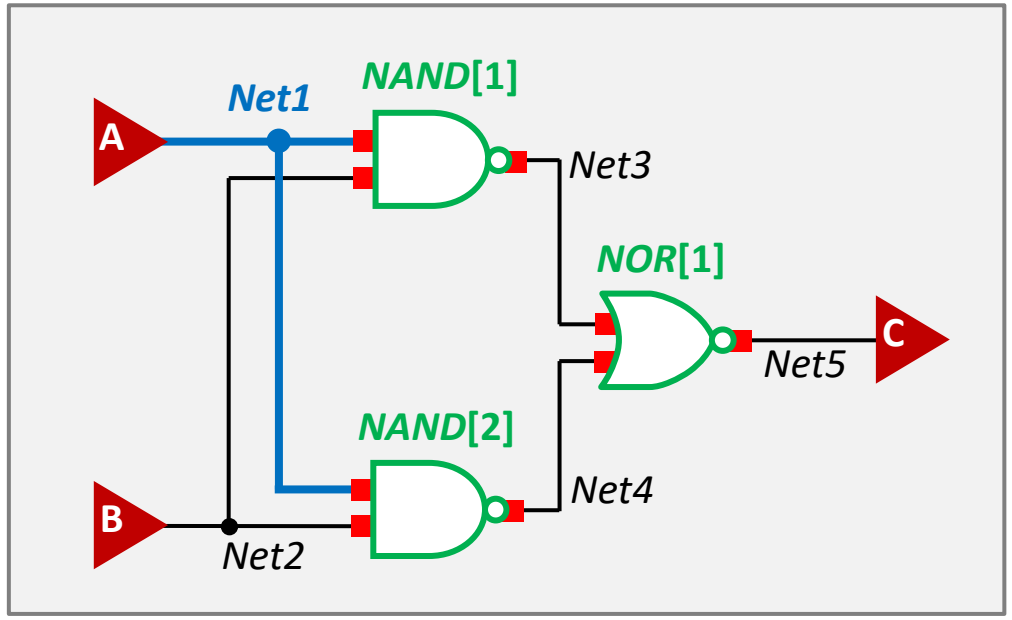




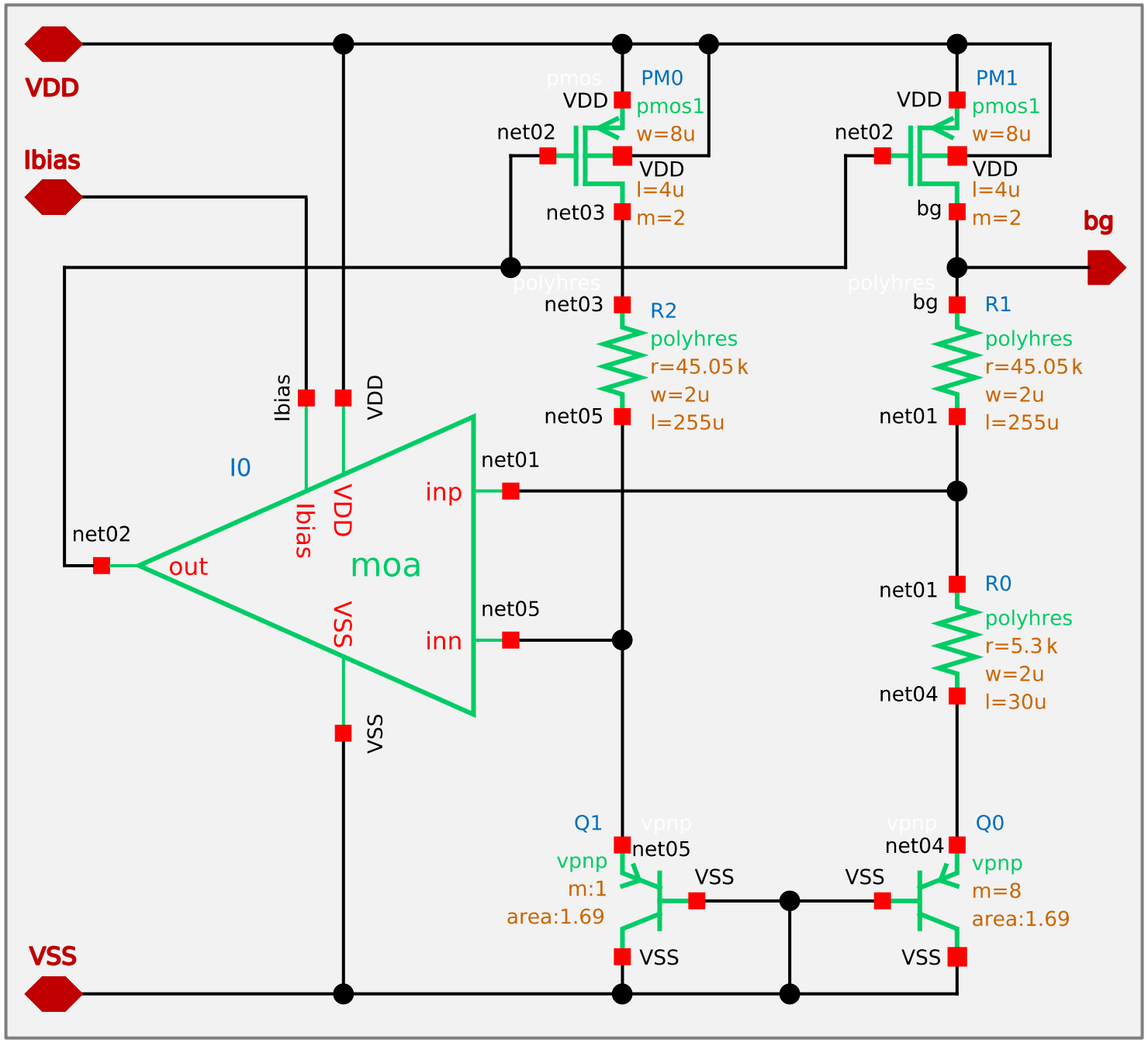


Pin-oriented netlist

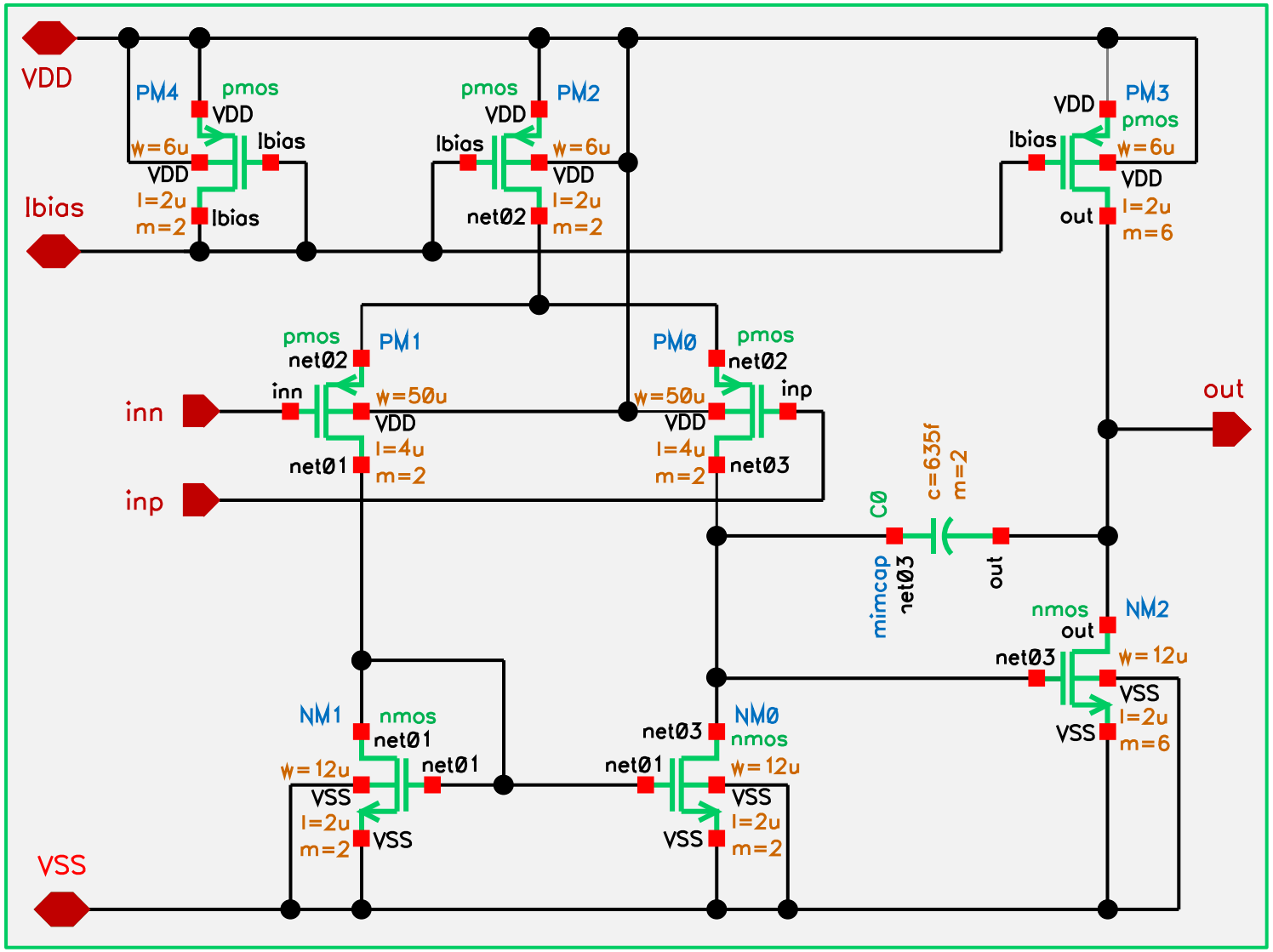
(*A*: ***Net1***)
(*B: Net2*)
(*C: Net5*)
(*NAND*[1]: *IN1* ***Net1***, *IN2 Net2*, *OUT Net3*)
(*NAND*[2]: *IN1* ***Net1***, *IN2 Net2*, *OUT Net4*)
(*NOR*[1]: *IN1 Net3*, *IN2 Net4*, *OUT Net5*)

Net-oriented netlist

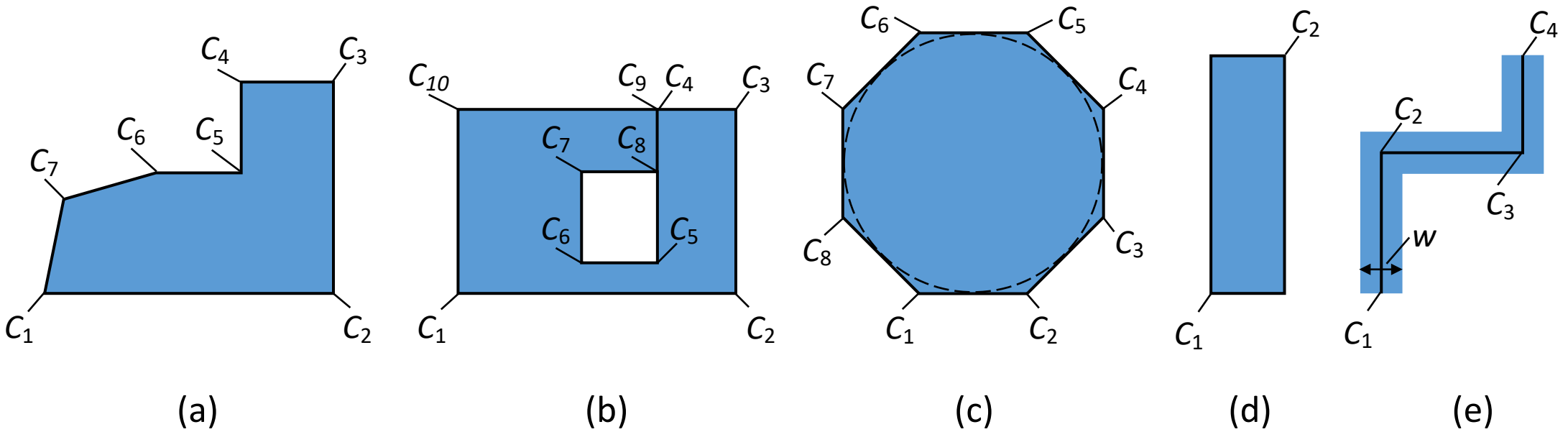
(***Net1***: *A*, *NAND*[1].*IN1*, *NAND*[2].*IN1*)
(*Net2*: *B*, *NAND*[1].*IN2*, *NAND*[2].*IN2*)
(*Net3*: *NAND*[1].*OUT*, *NOR*[1].*IN1*)
(*Net4*: *NAND*[2].*OUT*, *NOR*[1].*IN2*)
(*Net5*: *NOR*[1].*OUT*, *C*)

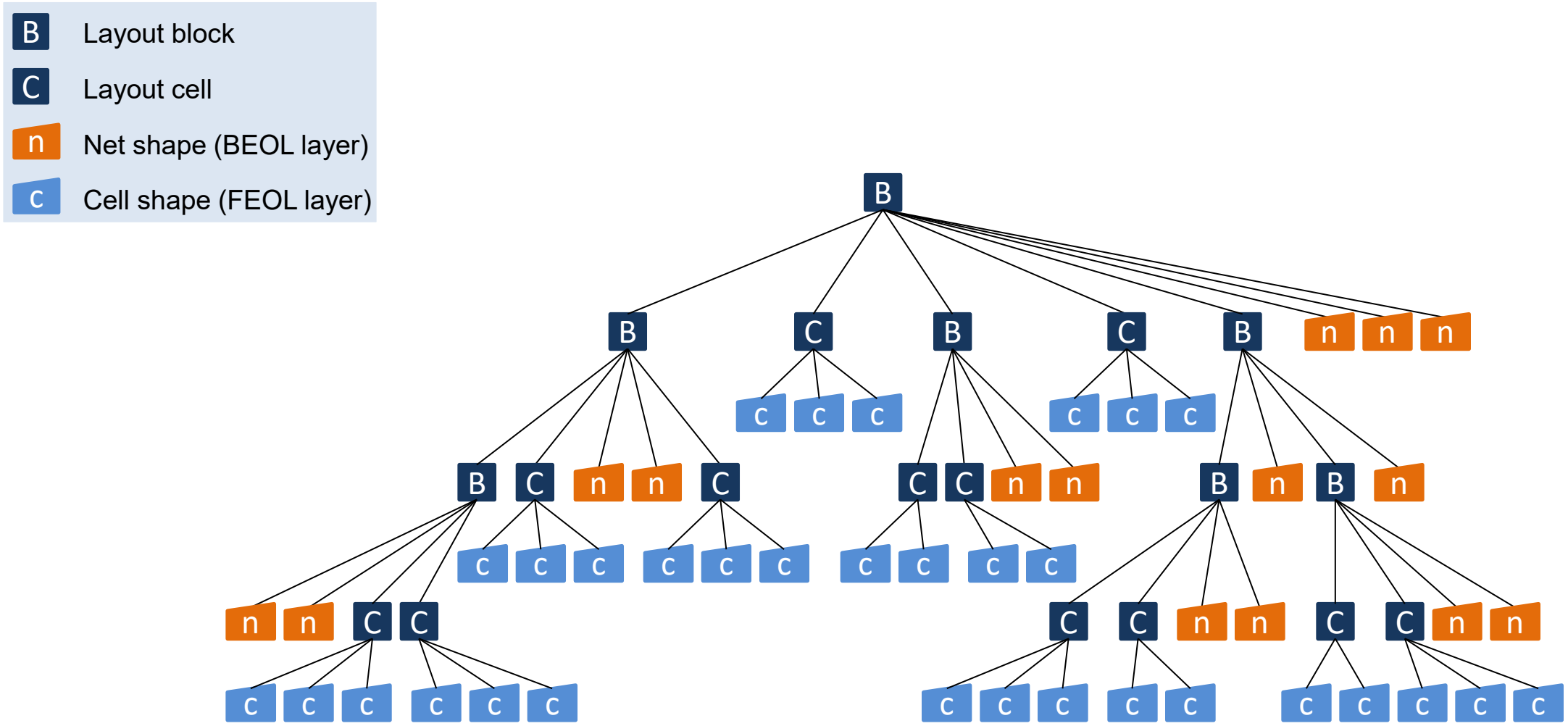



```
.SUBCKT bgap Ibias VDD VSS bg
QQ1 VSS VSS net05 vpnp M=1 EA=1.69
QQ0 VSS VSS net04 vpnp M=8 EA=1.69
XI0 Ibias VDD VSS net05 net01 net02 / moa
MPM1 bg net02 VDD VDD pmos W=8u L=4u M=2
MPM0 net03 net02 VDD VDD pmos W=8u L=4u M=2
RR2 net03 net05 45.05k polyhres W=2u L=255u
RR1 bg net01 45.05k polyhres W=2u L=255u
RR0 net01 net04 5.3k polyhres W=2u L=30u
.ENDS
```

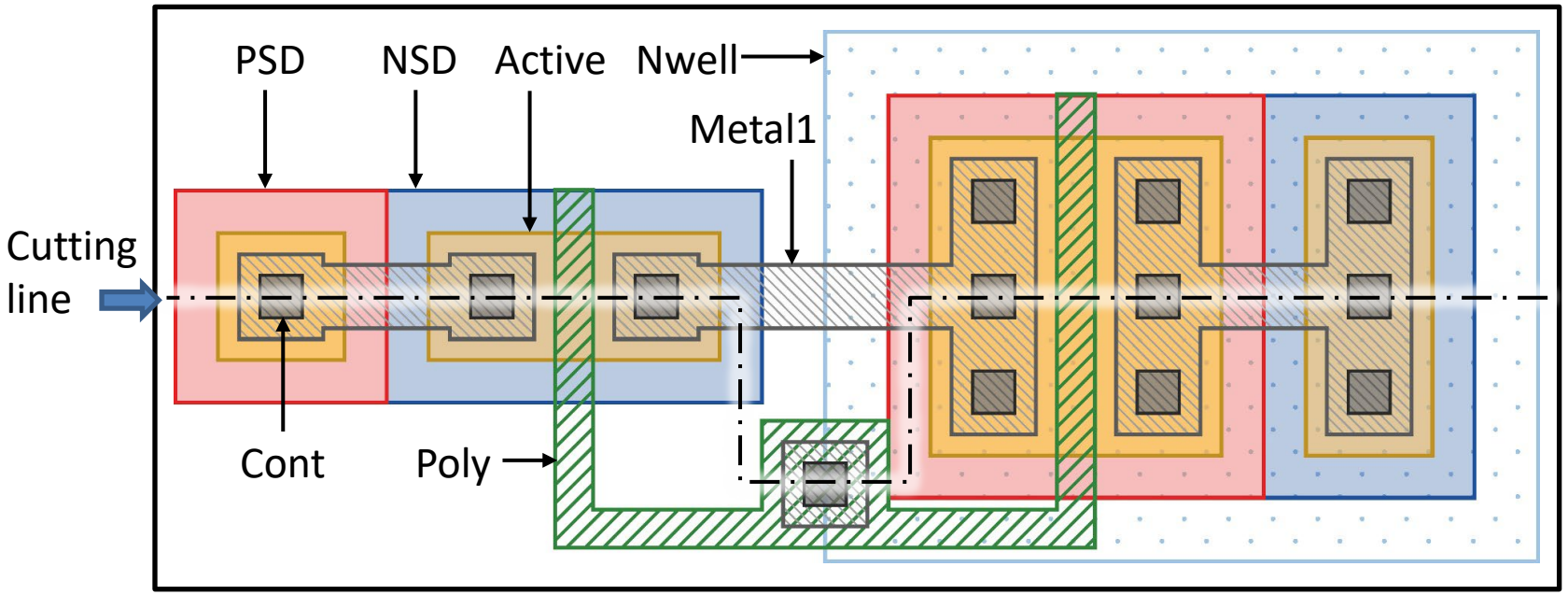



```
.SUBCKT moa Ibias VDD VSS inn inp out
MPM4 Ibias Ibias VDD VDD pmos W=6u L=2u M=2
MPM3 out Ibias VDD VDD pmos W=6u L=2u M=6
MPM0 net03 inp net02 VDD pmos W=50u L=4u M=2
MPM1 net01 inn net02 VDD pmos W=50u L=4u M=2
MPM2 net02 Ibias VDD VDD pmos W=6u L=2u M=2
MNM2 out net03 VSS VSS nmos W=12u L=2u M=6
MNM1 net01 net01 VSS VSS nmos W=12u L=2u M=2
MNM0 net03 net01 VSS VSS nmos W=12u L=2u M=2
CC0 net03 out 635f mimcap M=2
.ENDS
```

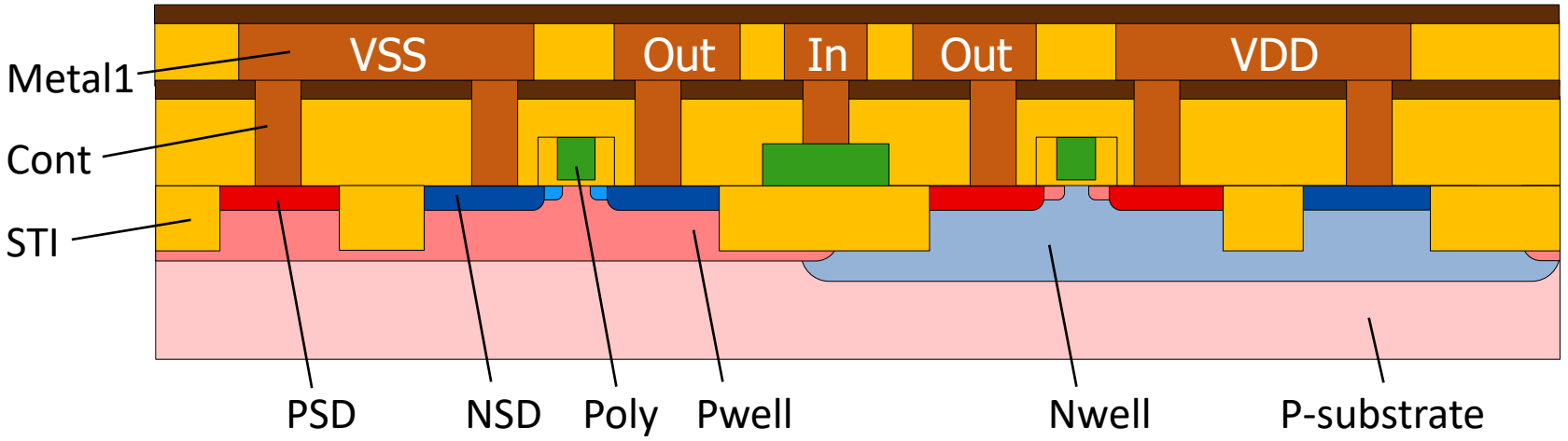




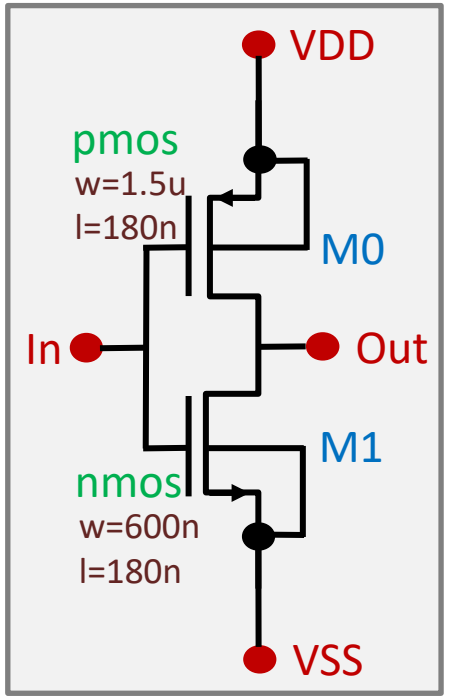
Layout

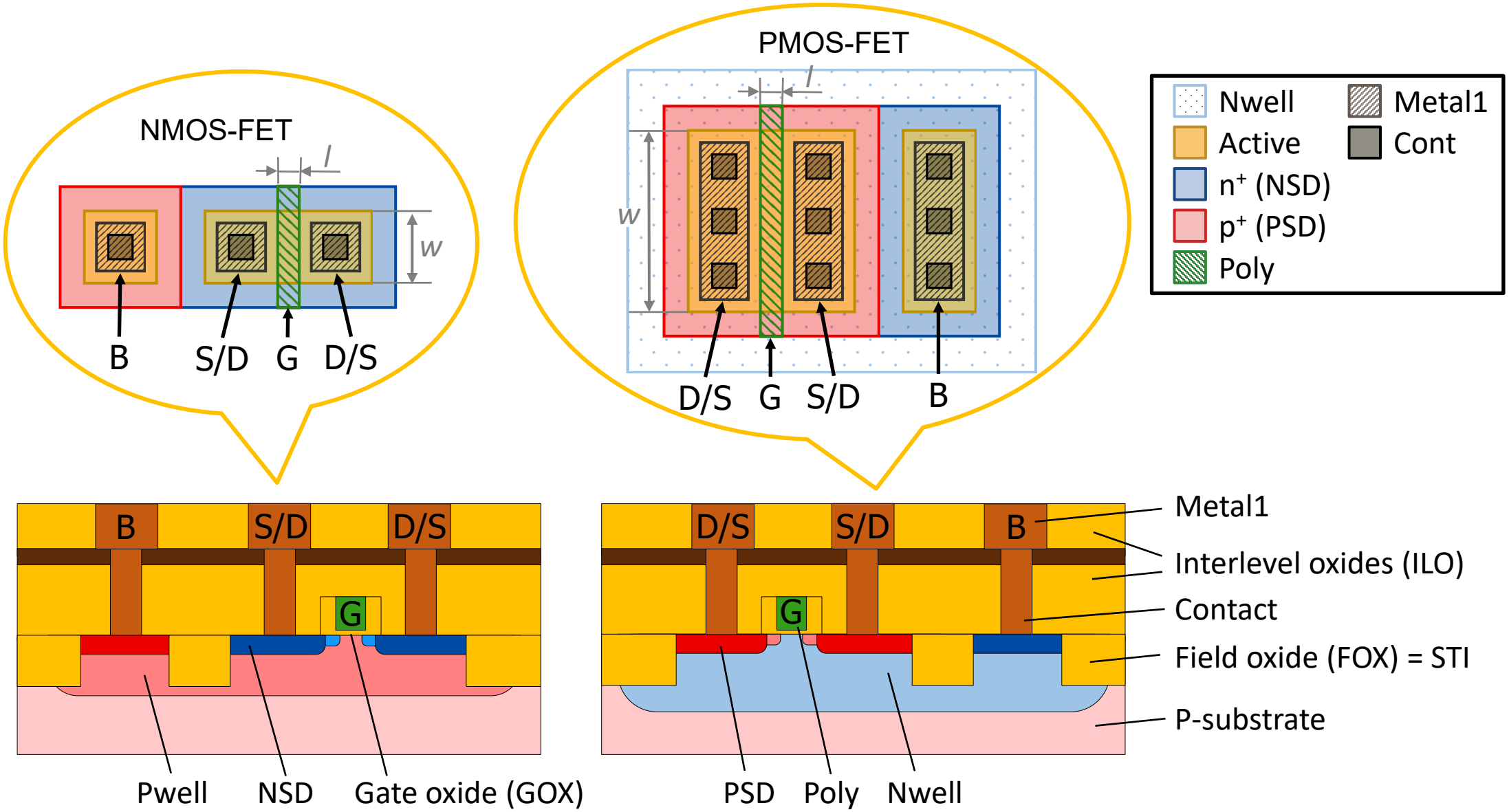


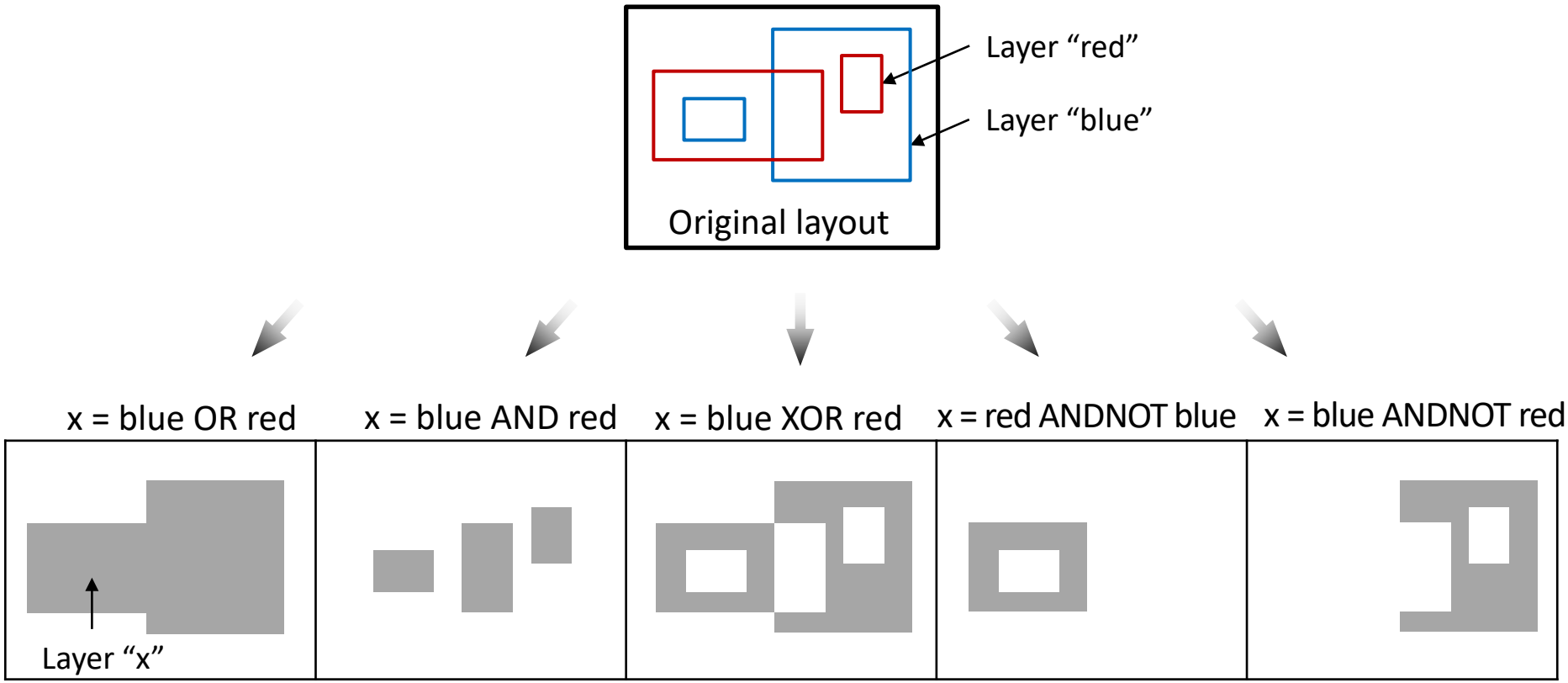
Sectional view

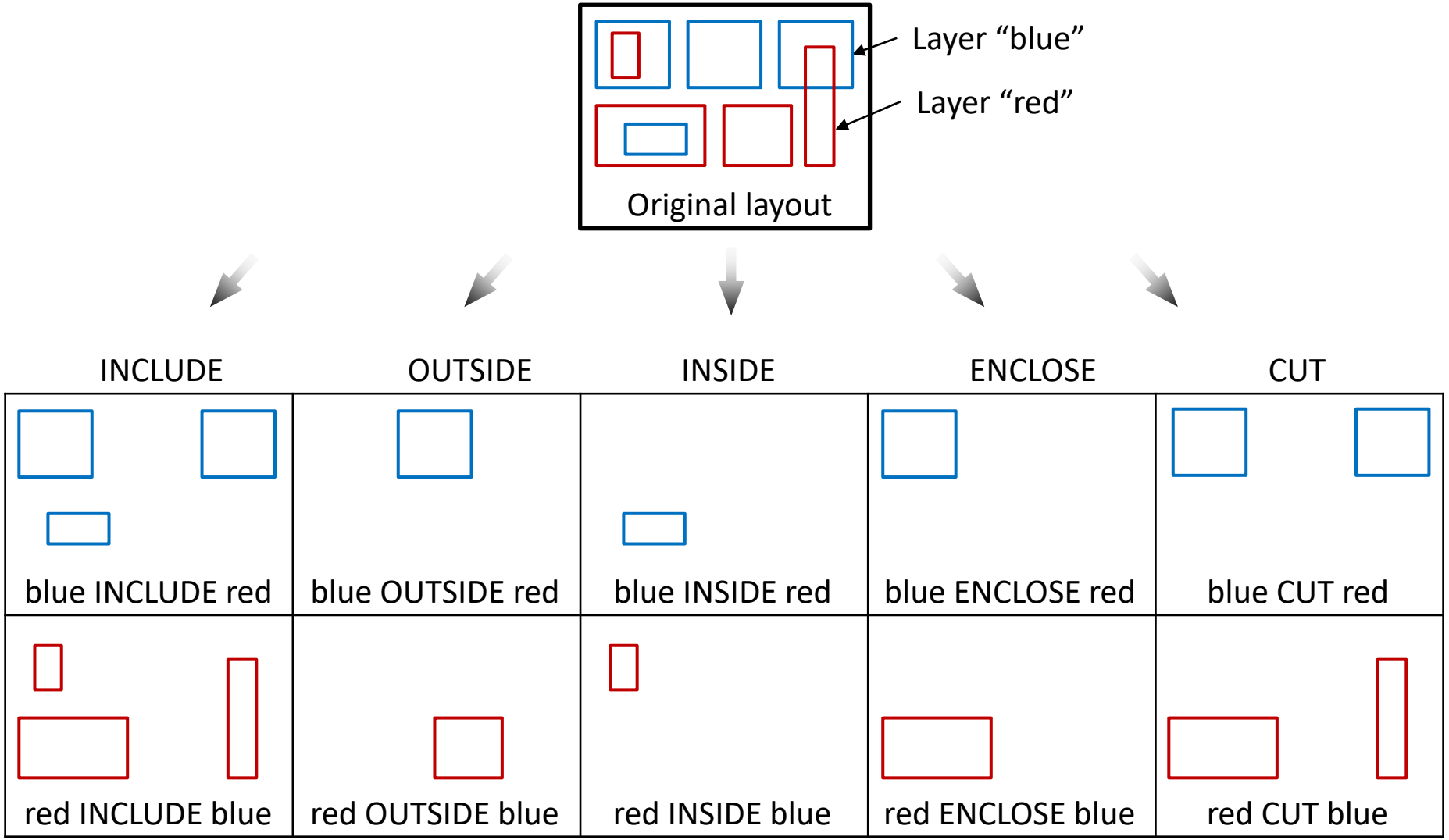


Circuit diagram

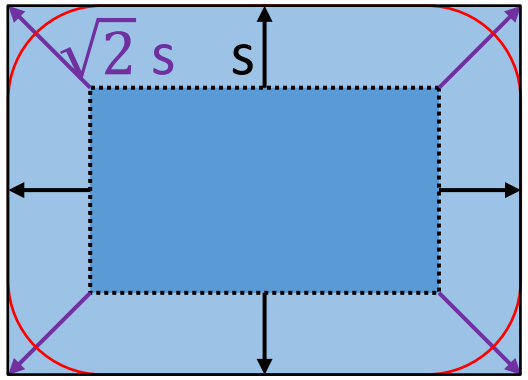


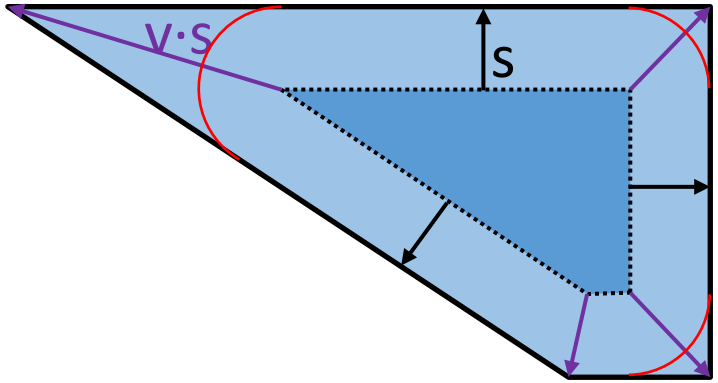




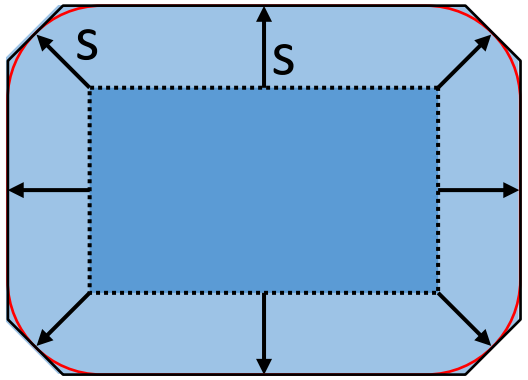


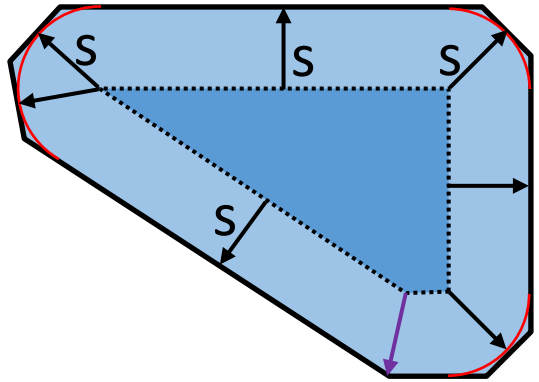
Sizing without beveling

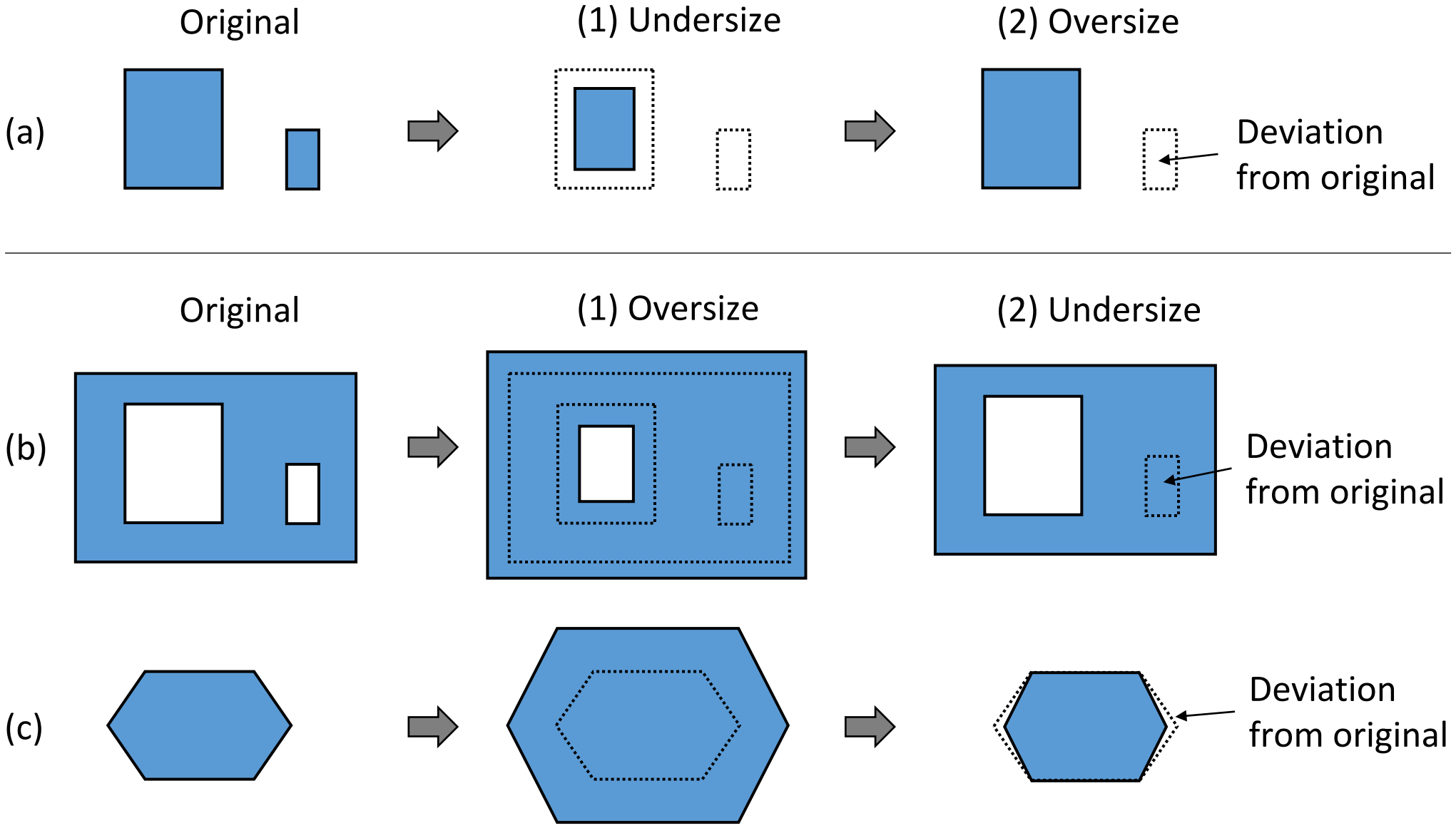


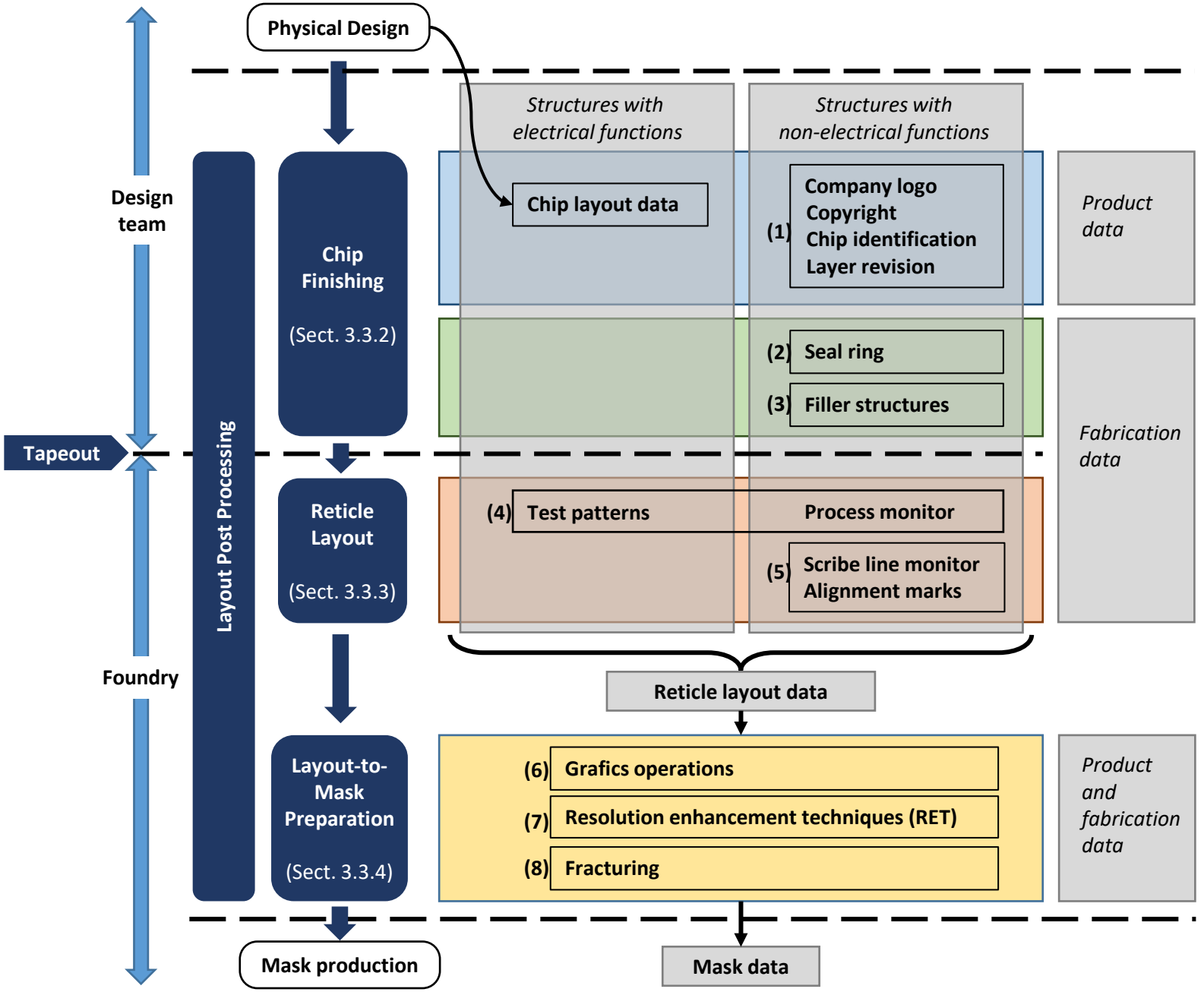


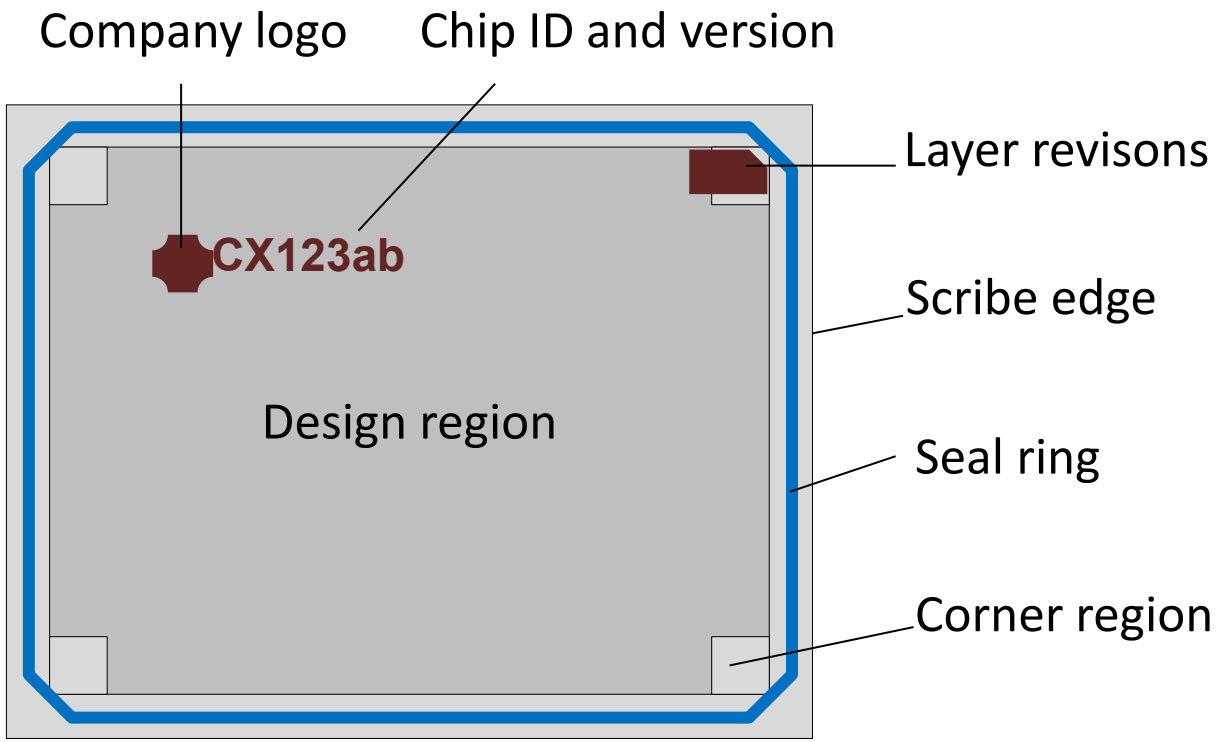
Sizing with beveling

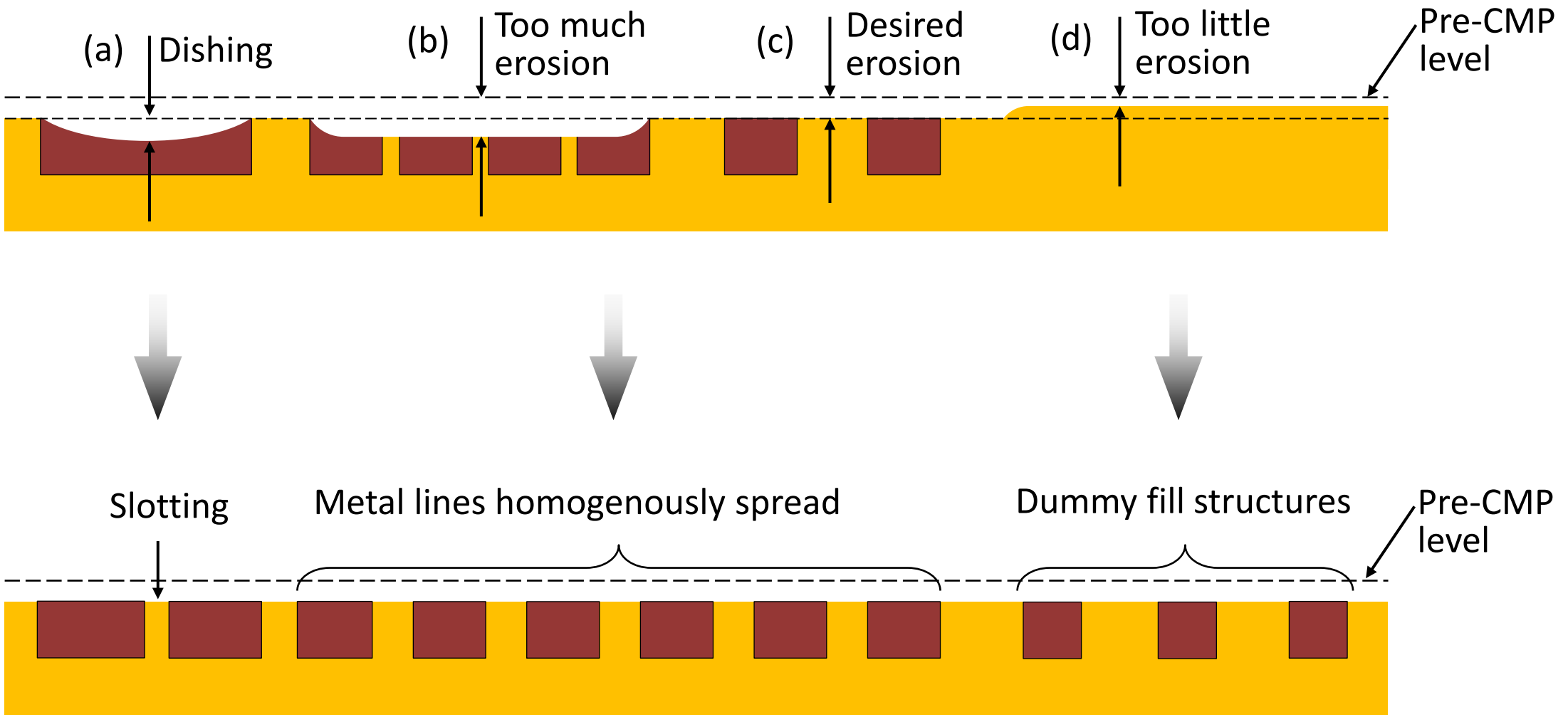


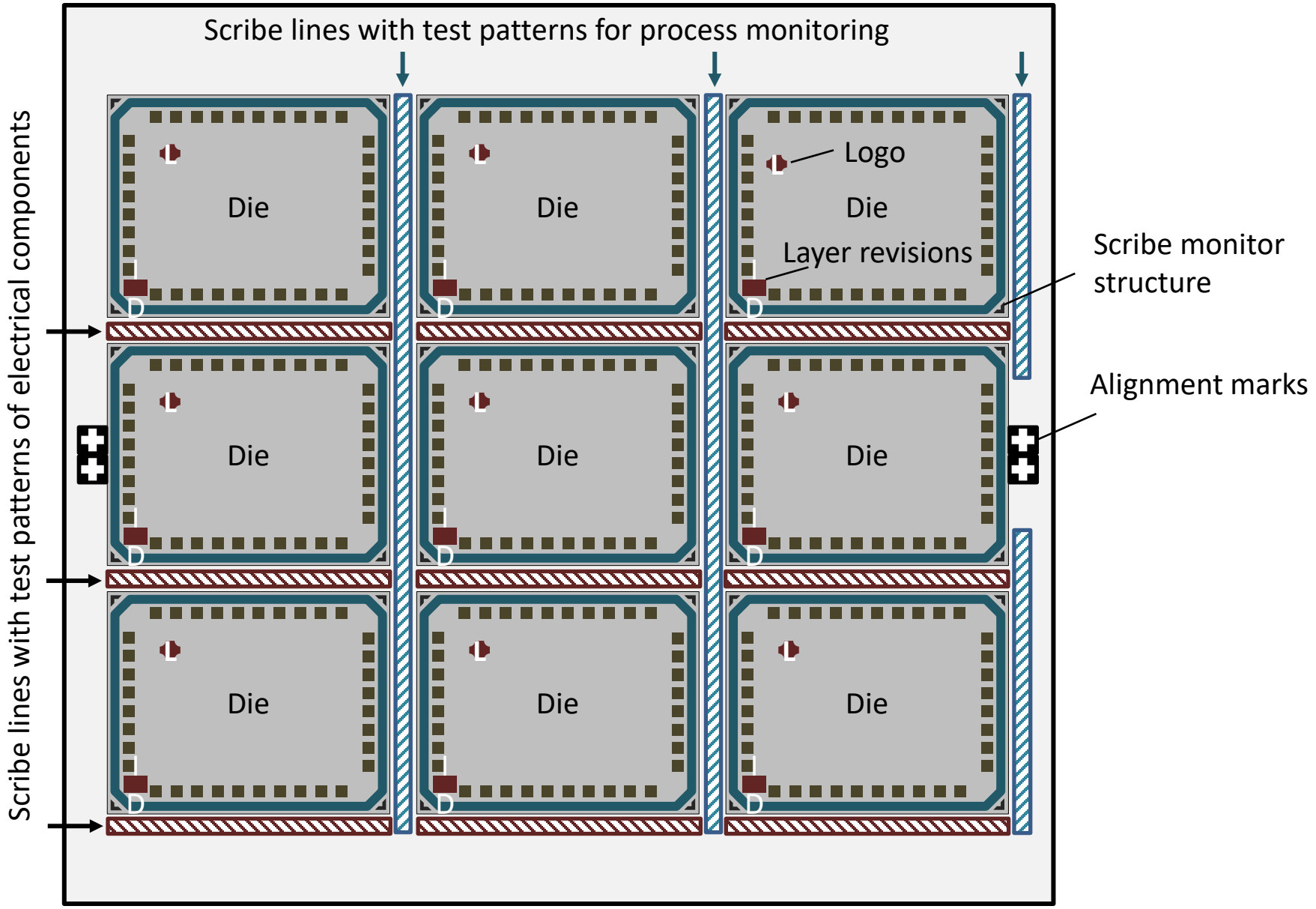


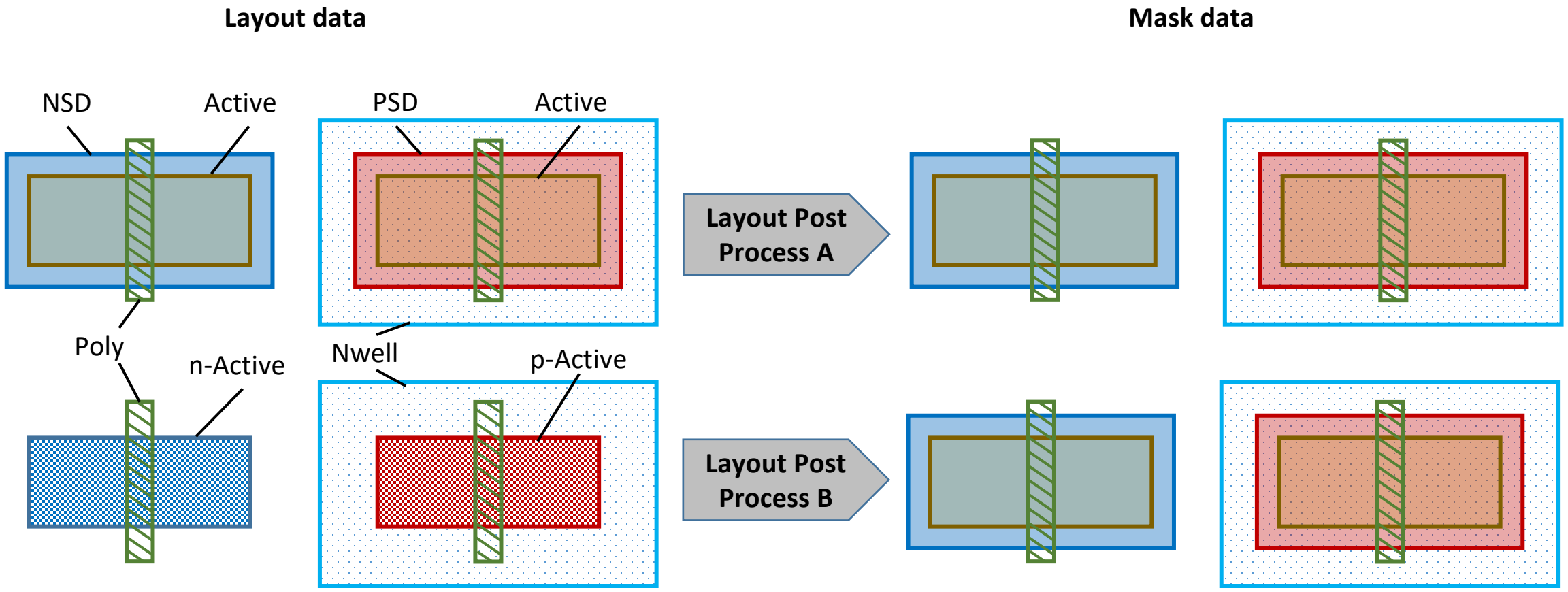


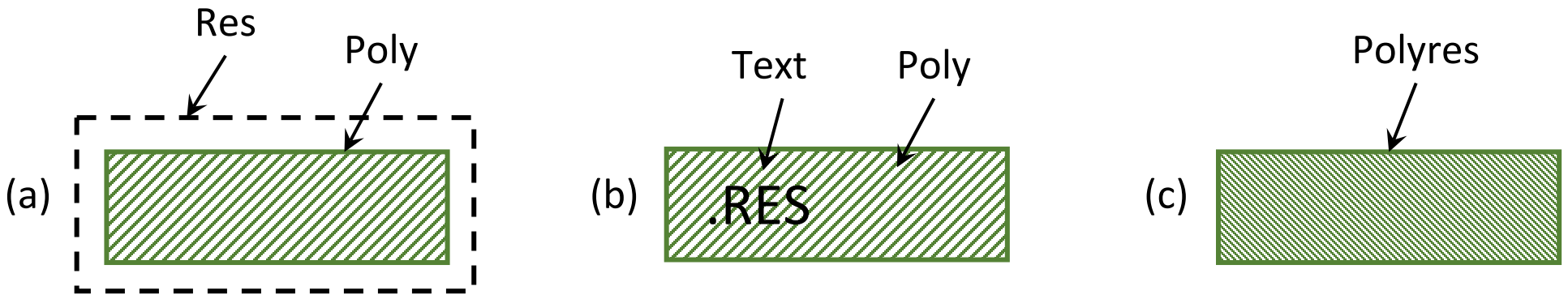




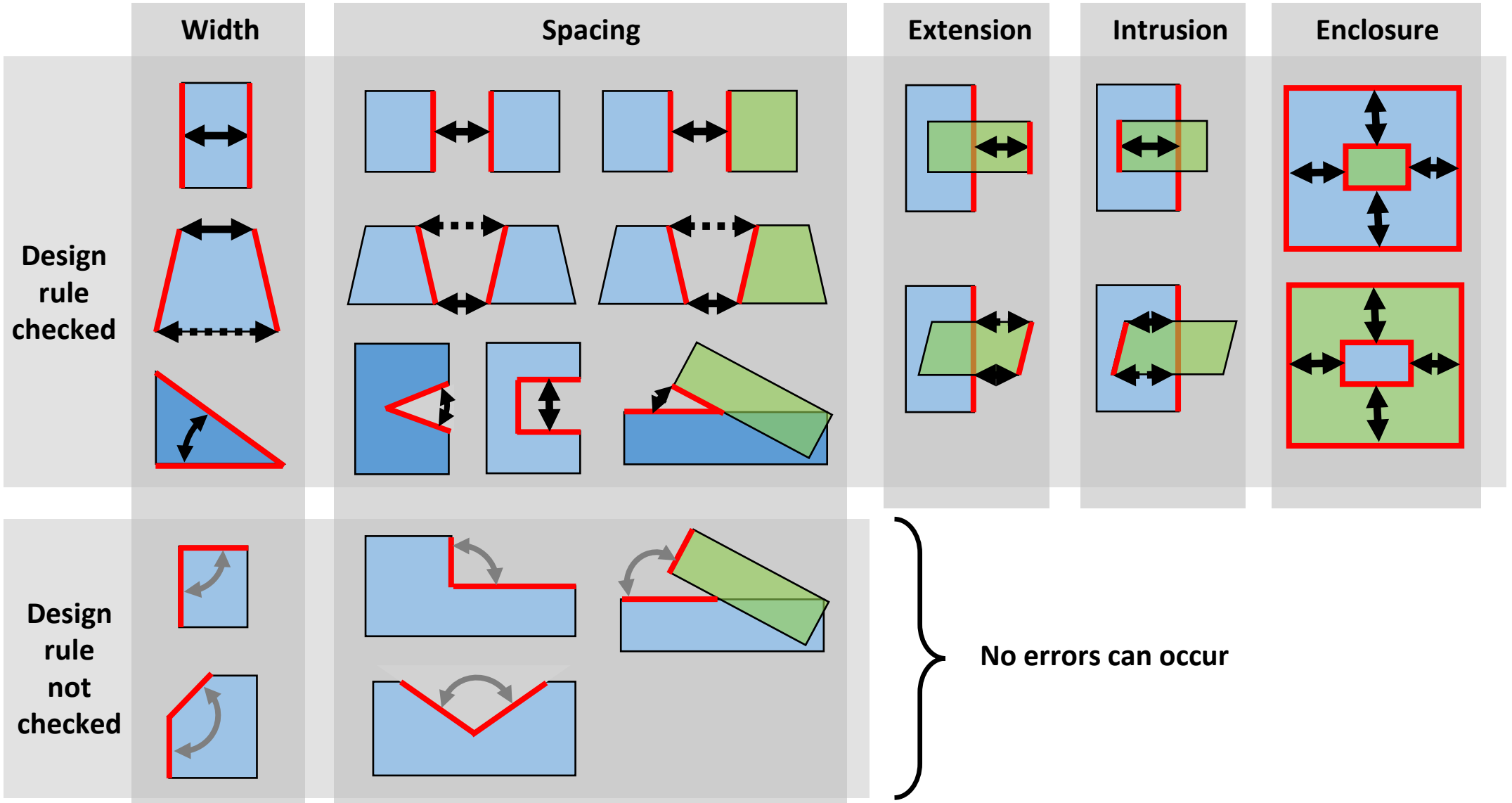


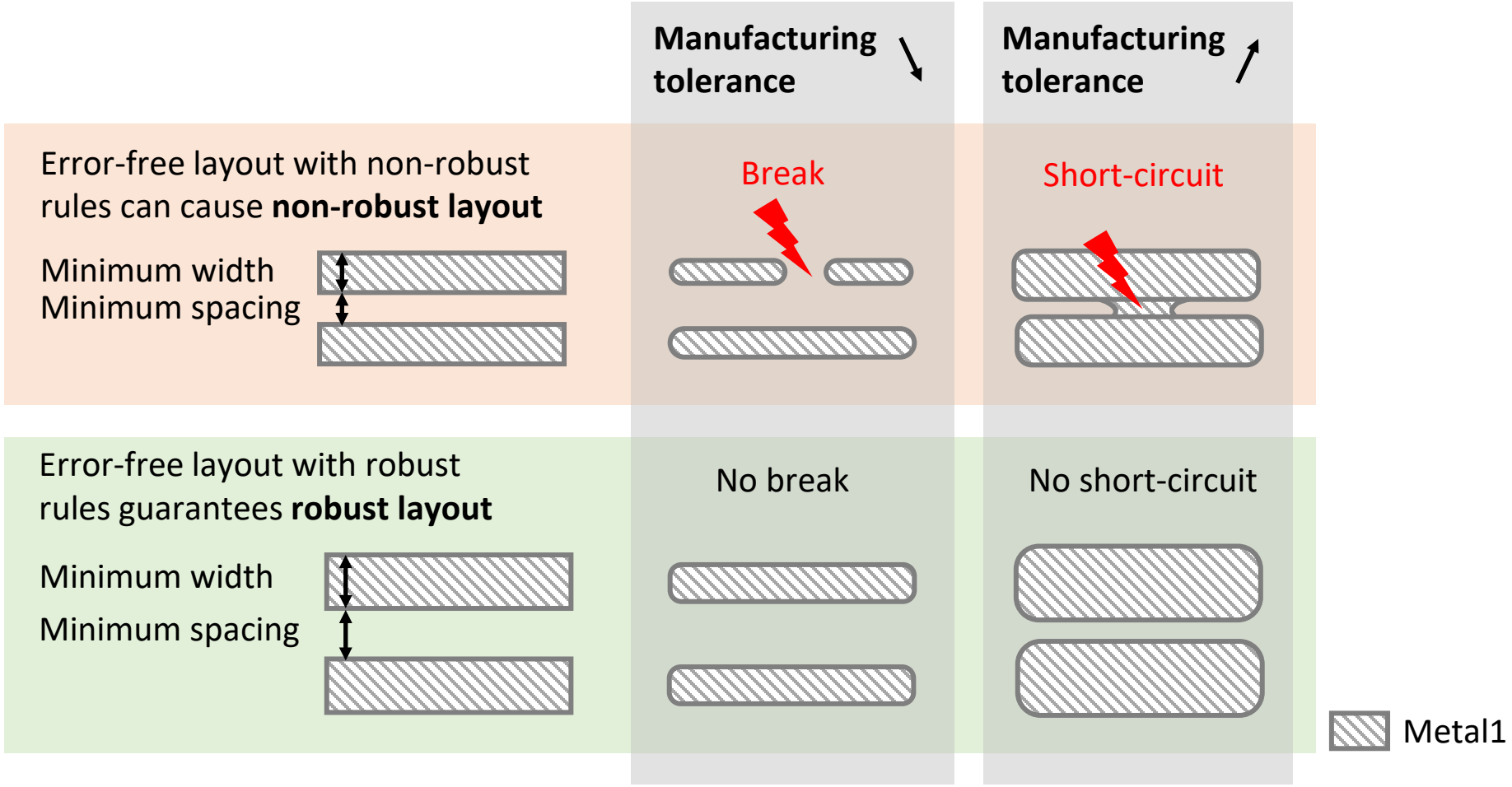


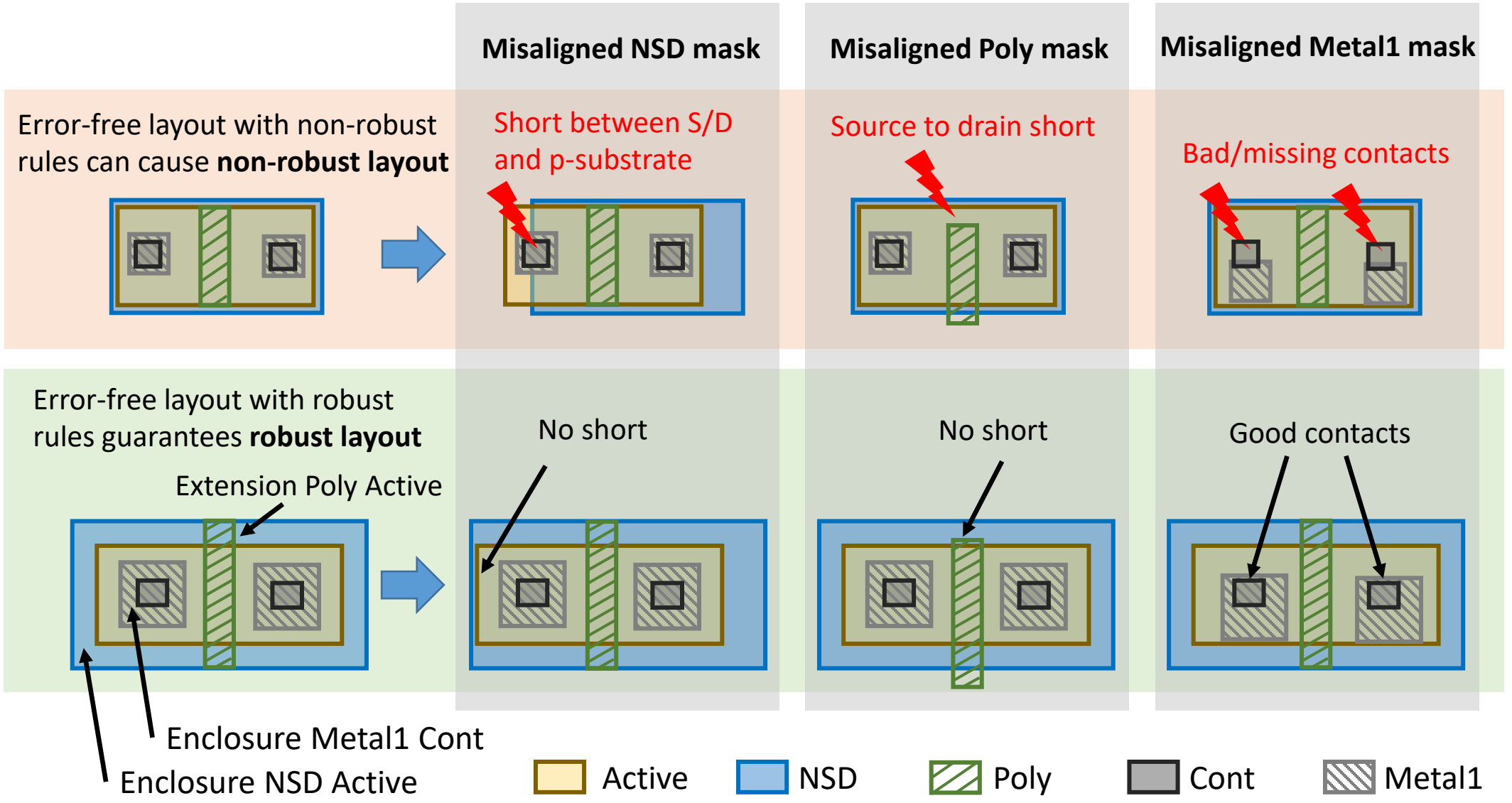


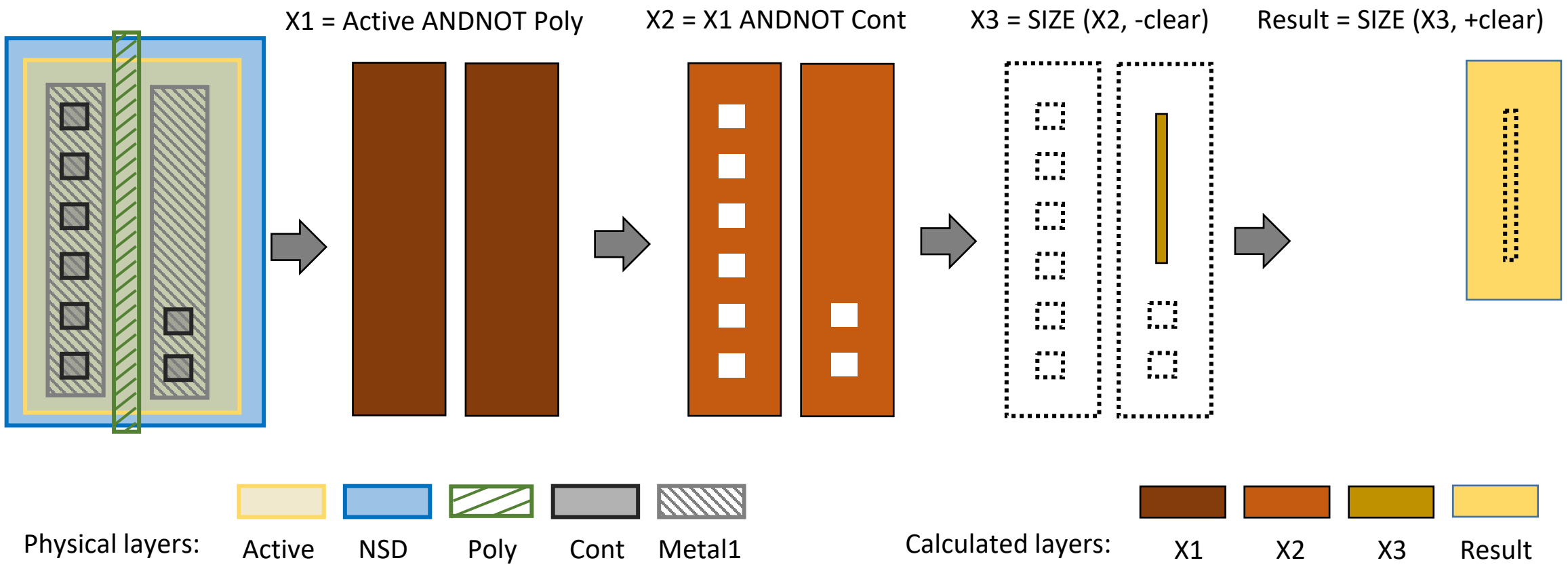


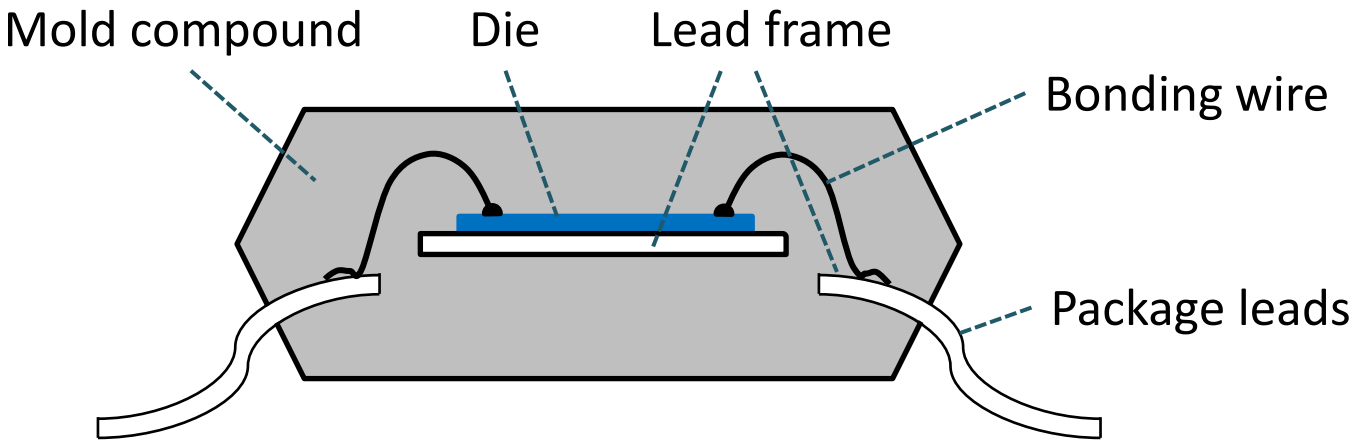
Design Rule	Relationship between edges	Number of shapes	Number of layers
Width	Inside / inside	1	1
Spacing	Outside / outside	(a) 1 or 2 (b) 2	(a) 1 (b) 2
Extension	Inside / outside	2	2
Intrusion	Inside / inside	2	2
Enclosure	Outside / inside	2	2

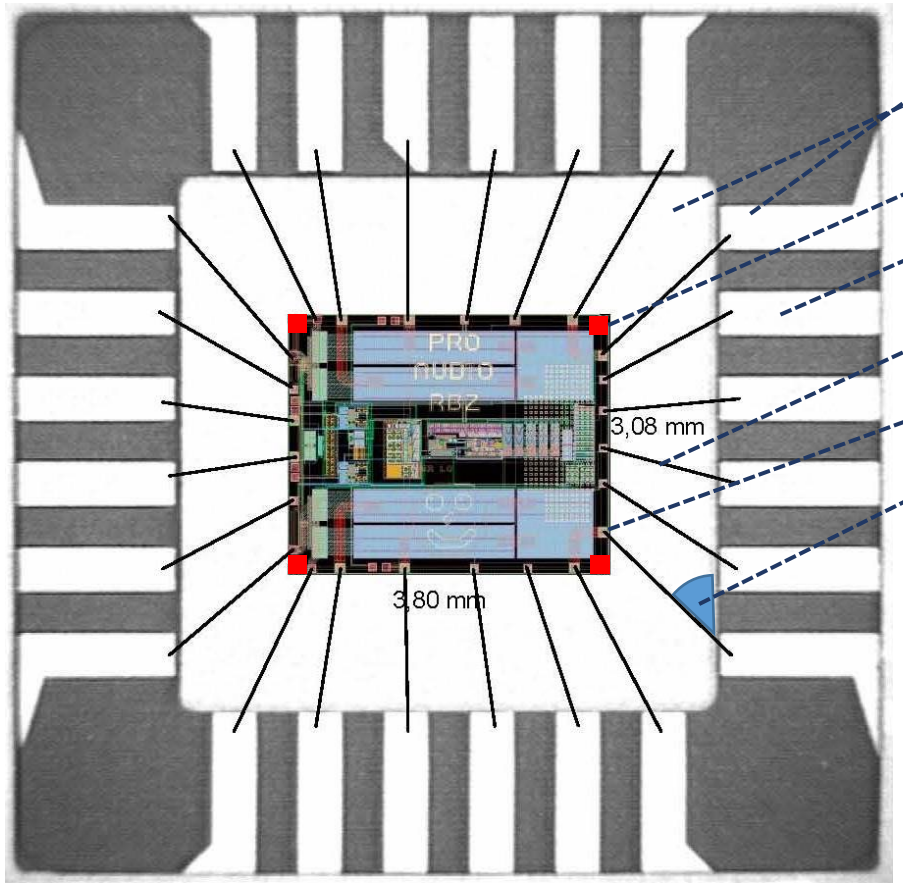












Lead frame

Forbidden area for bond pads

Contact points on the lead frame

Bonding wire

Bond pad

Bonding-wire angle

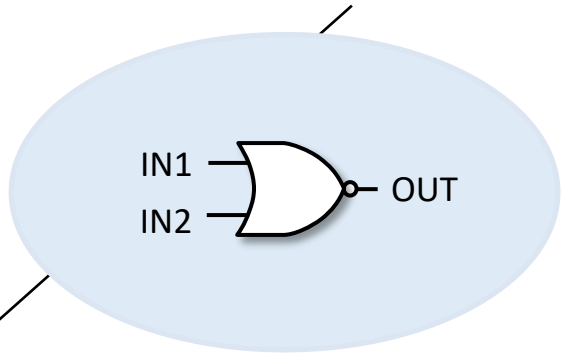
Model

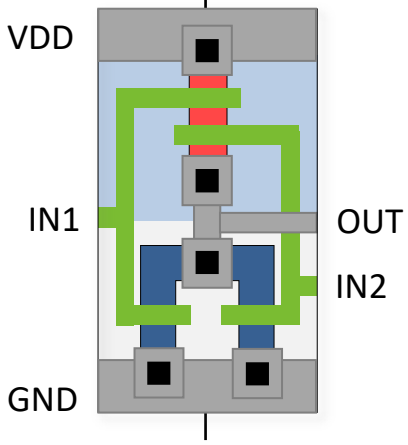
```
entity NOR2 is
  port(IN1: in std_logic;
       IN2: in std_logic;
       OUT: out std_logic)
end entity NOR2;

                    is

       OUT   <= NOT(IN1 OR IN2);
  end architecture RTL;
```

Symbol





Layout