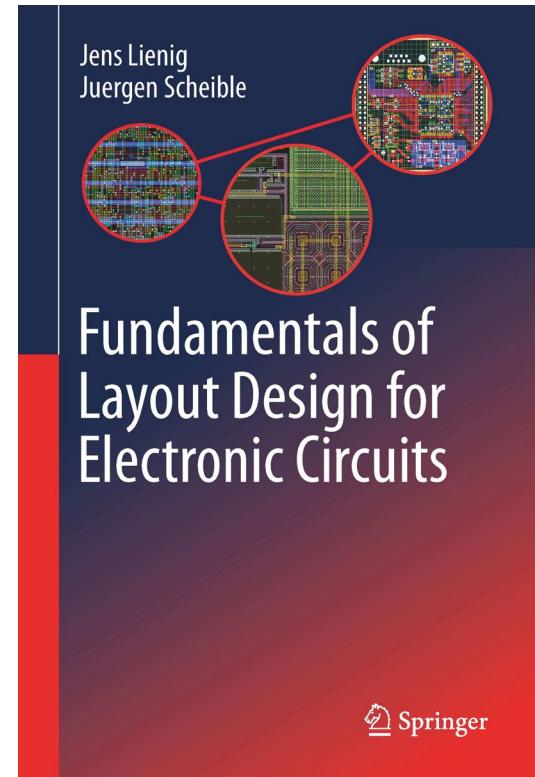


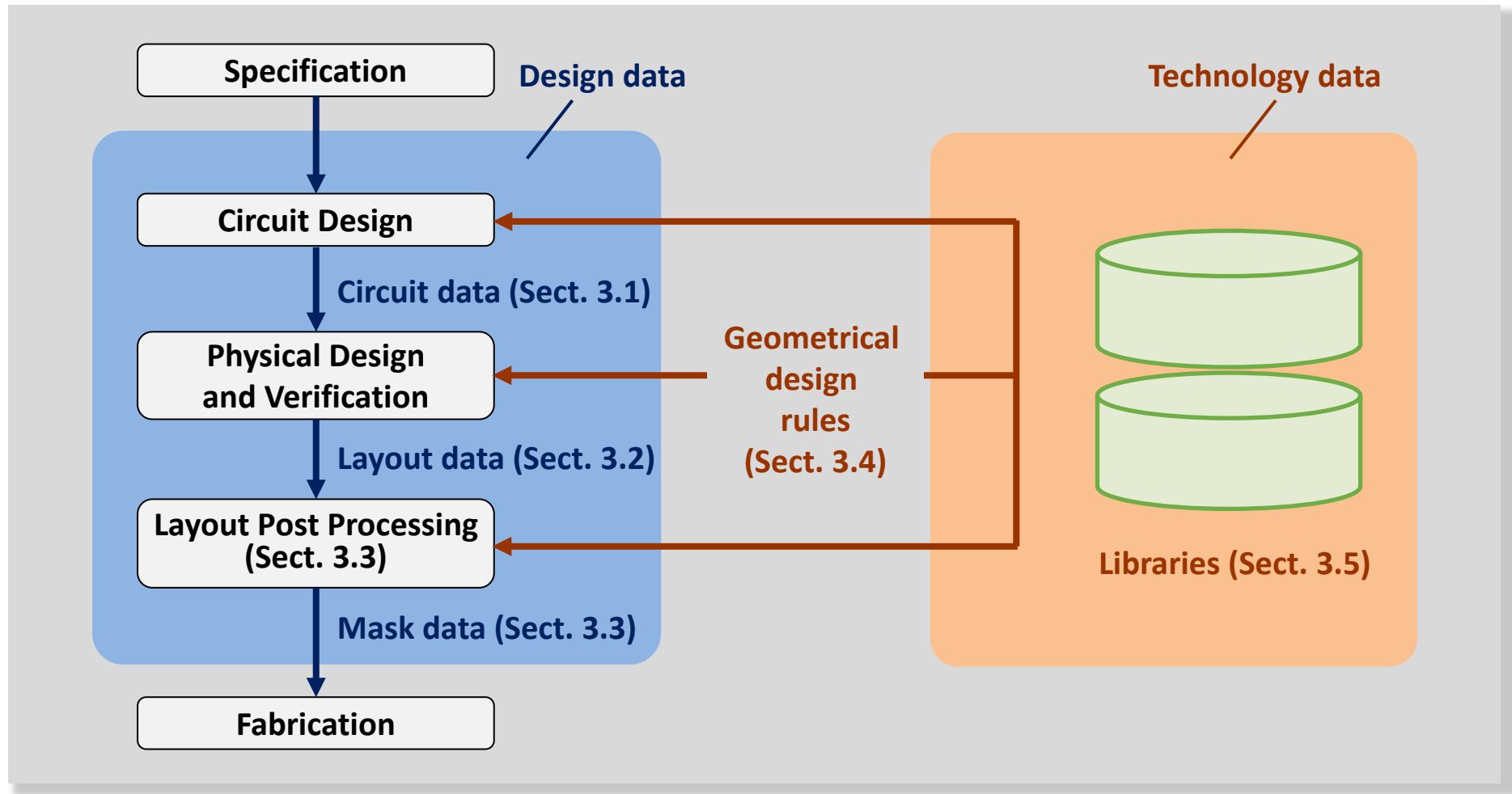
# Chapter 3: Bridges to Technology: Interfaces, Design Rules, and Libraries

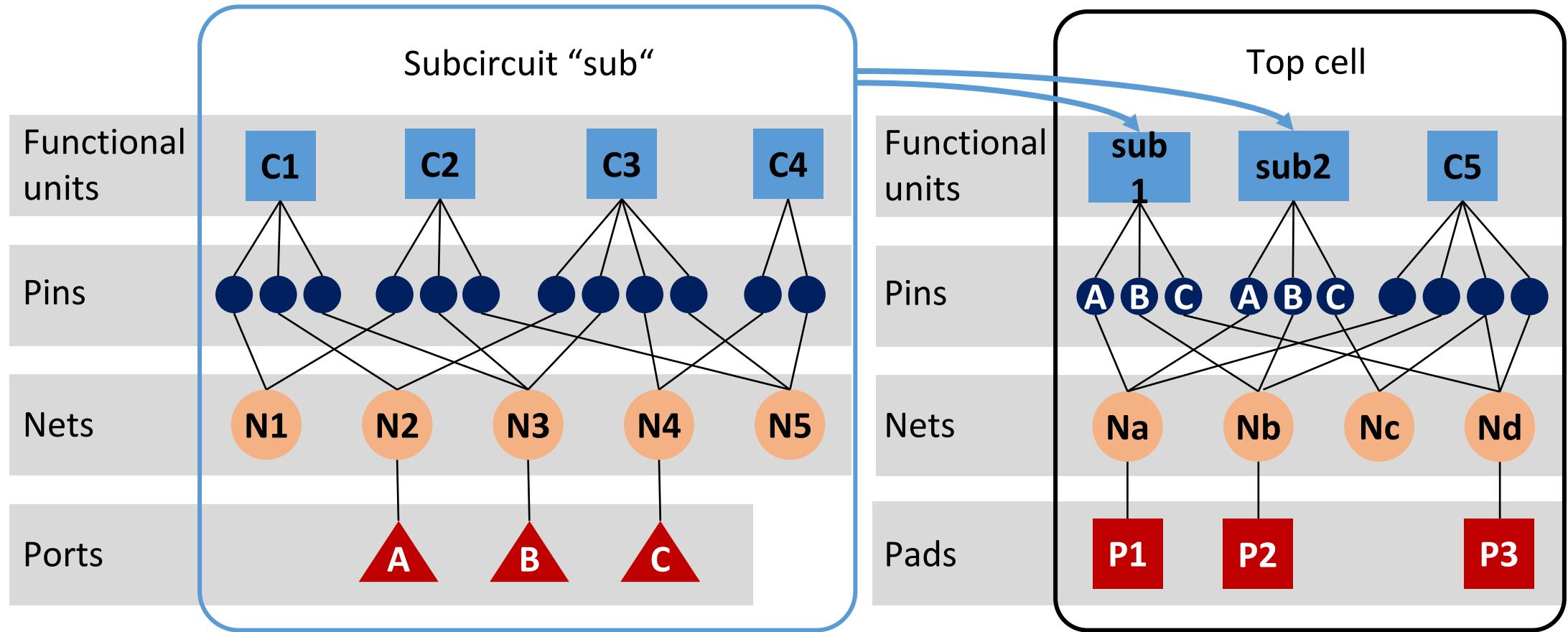
- 3.1 Circuit Data: Schematic and Netlists
- 3.2 Layout Data: Layers and Polygons
- 3.3 Mask Data: Layout Post Processing
- 3.4 Geometrical Design Rules
- 3.5 Libraries

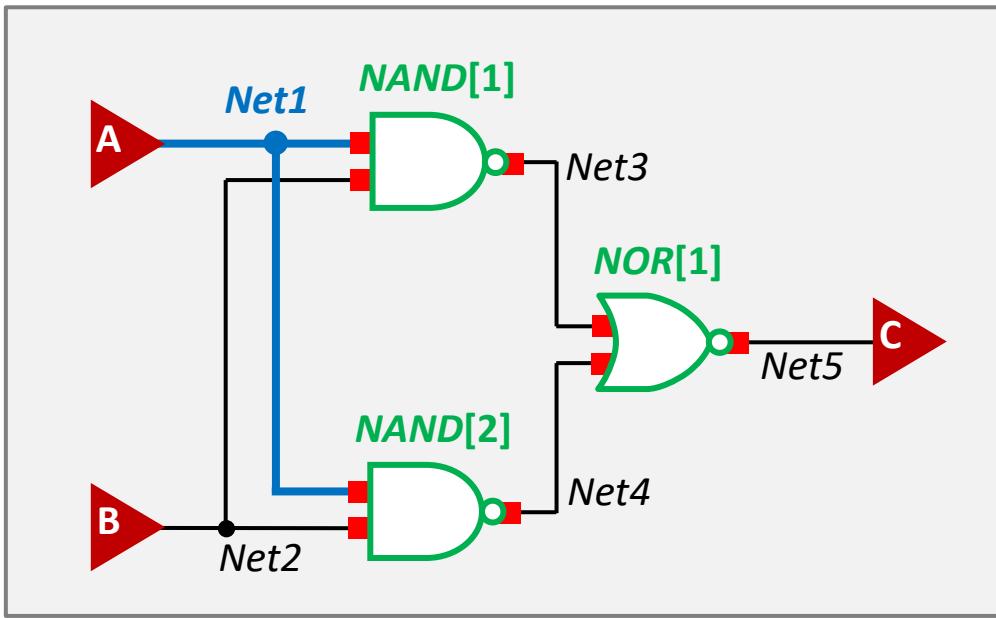


# Chapter 3: Bridges to Technology: Interfaces, Design Rules, and Libraries

<b>3.1</b>	<b>Circuit Data: Schematics and Netlists</b>
3.1.1	Structural Description of a Circuit
3.1.2	Idealizations in Circuit Descriptions
3.1.3	Circuit Representations: Netlist and Schematic
<b>3.2</b>	<b>Layout Data: Layers and Polygons</b>
3.2.1	Structure of Layout Data
3.2.2	How to Read a Layout View
3.2.3	Graphics Operations
<b>3.3</b>	<b>Mask Data: Layout Post Processing</b>
3.3.1	Overview
3.3.2	Chip Finishing
3.3.3	Reticle Layout
3.3.4	Layout-to-Mask Preparation
<b>3.4</b>	<b>Geometrical Design Rules</b>
3.4.1	Technological Constraints and Geometrical Design Rules
3.4.2	Basic Geometrical Design Rules
3.4.3	Programmed Geometrical Design Rules
3.4.4	Rules for Die Assembly
<b>3.5</b>	<b>Libraries</b>
3.5.1	Process Design Kits and Primitive Device Libraries
3.5.2	Cell Libraries
3.5.3	Libraries for Printed Circuit Board Design





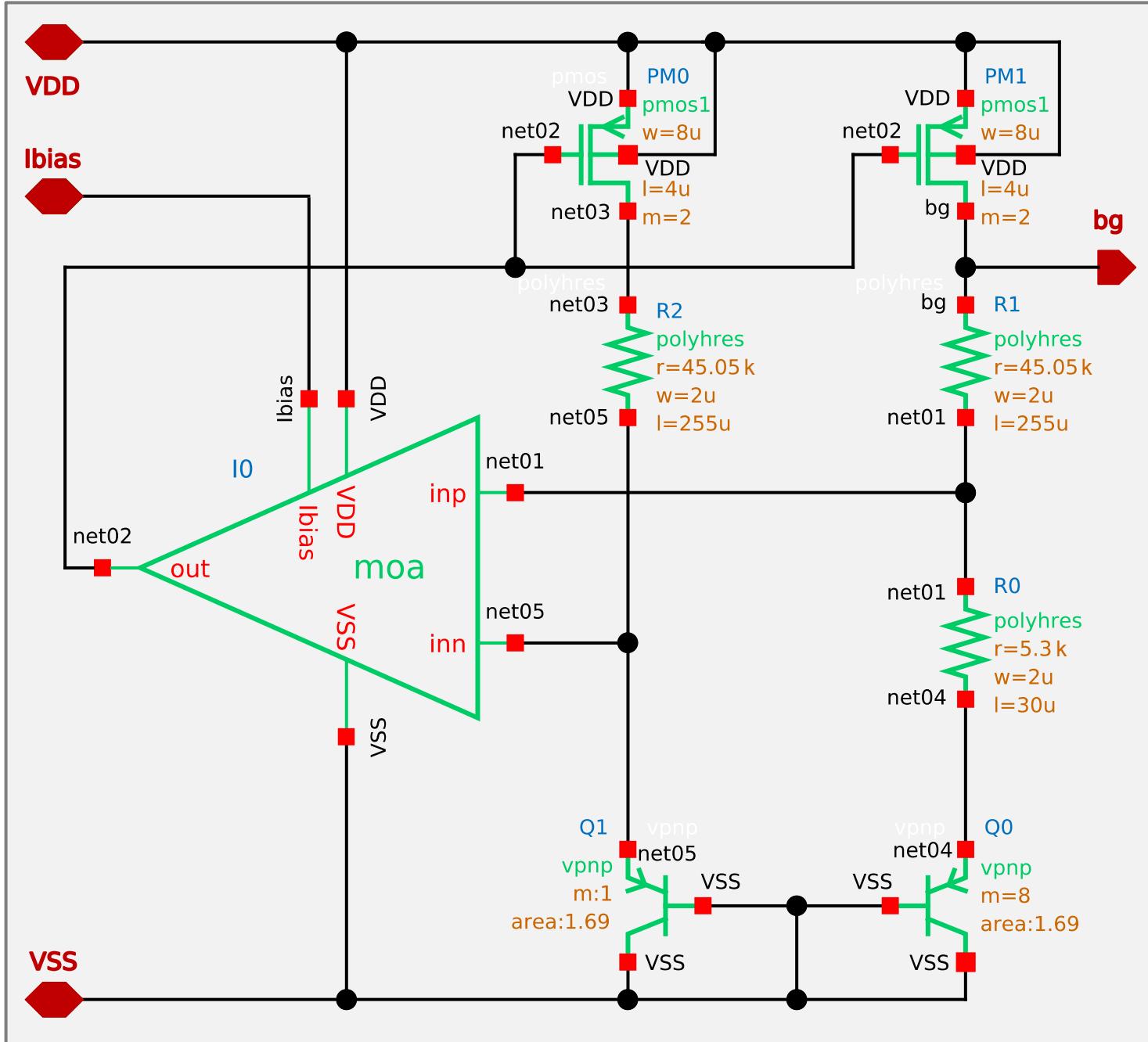


Pin-oriented netlist

```
(A: Net1)
(B: Net2)
(C: Net5)
(NAND[1]: IN1 Net1, IN2 Net2, OUT Net3)
(NAND[2]: IN1 Net1, IN2 Net2, OUT Net4)
(NOR[1]: IN1 Net3, IN2 Net4, OUT Net5)
```

Net-oriented netlist

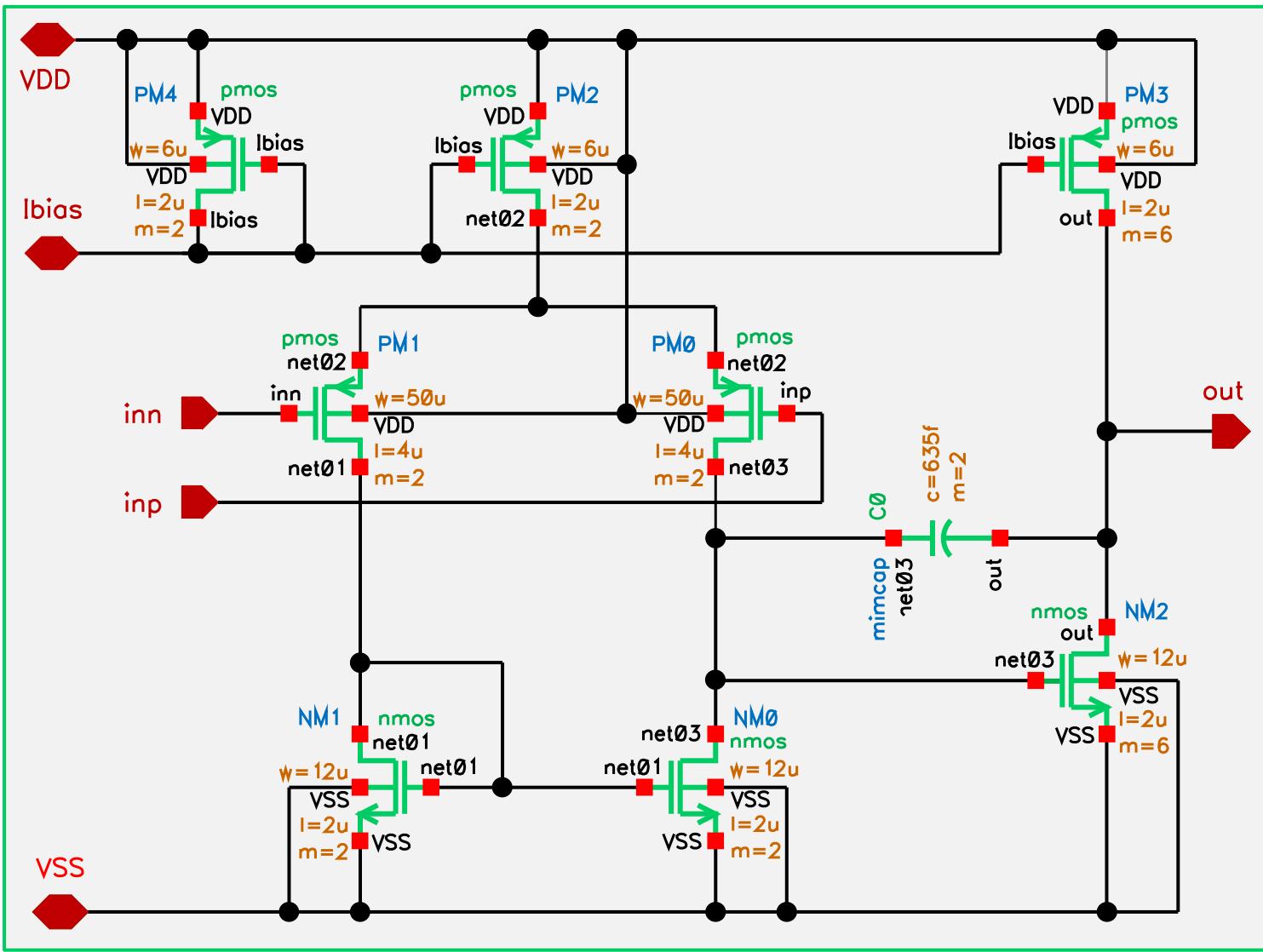
```
(Net1: A, NAND[1].IN1, NAND[2].IN1)
(Net2: B, NAND[1].IN2, NAND[2].IN2)
(Net3: NAND[1].OUT, NOR[1].IN1)
(Net4: NAND[2].OUT, NOR[1].IN2)
(Net5: NOR[1].OUT, C)
```



```

.SUBCKT bgap Ibias VDD VSS bg
QQ1 VSS VSS net05 vpnp M=1 EA=1.69
QQ0 VSS VSS net04 vpnp M=8 EA=1.69
XIO Ibias VDD VSS net05 net01 net02 / moa
MPM1 bg net02 VDD VDD pmos W=8u L=4u M=2
MPM0 net03 net02 VDD VDD pmos W=8u L=4u M=2
RR2 net03 net05 45.05k polyhres W=2u L=255u
RR1 bg net01 45.05k polyhres W=2u L=255u
RR0 net01 net04 5.3k polyhres W=2u L=30u
.ENDS

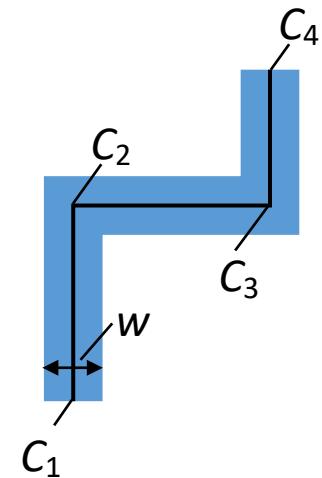
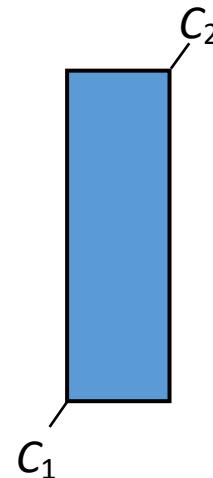
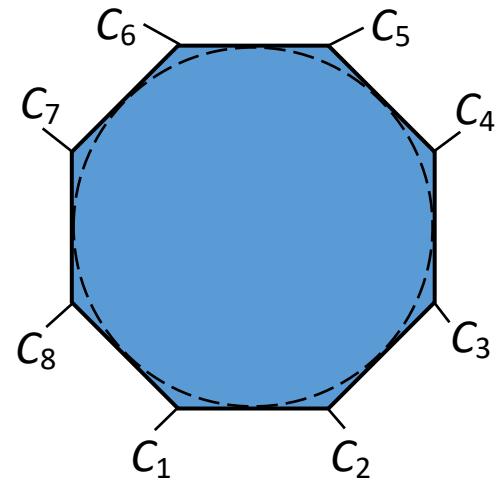
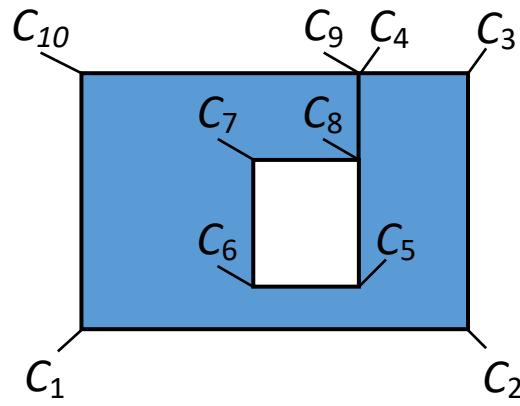
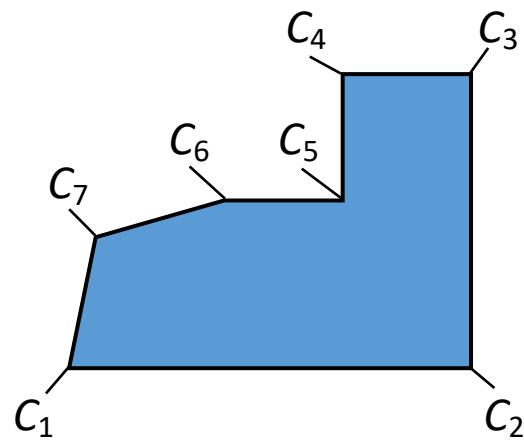
```



```

.SUBCKT moa Ibias VDD VSS inn inp out
MPM4 Ibias Ibias VDD VDD pmos W=6u L=2u M=2
MPM3 out Ibias VDD VDD pmos W=6u L=2u M=6
MPM0 net03 inp net02 VDD pmos W=50u L=4u M=2
MPM1 net01 inn net02 VDD pmos W=50u L=4u M=2
MPM2 net02 Ibias VDD VDD pmos W=6u L=2u M=2
MNM2 out net03 VSS VSS nmos W=12u L=2u M=6
MNM1 net01 net01 VSS VSS nmos W=12u L=2u M=2
MNMO net03 net01 VSS VSS nmos W=12u L=2u M=2
CC0 net03 out 635f mimcap M=2
.ENDS

```



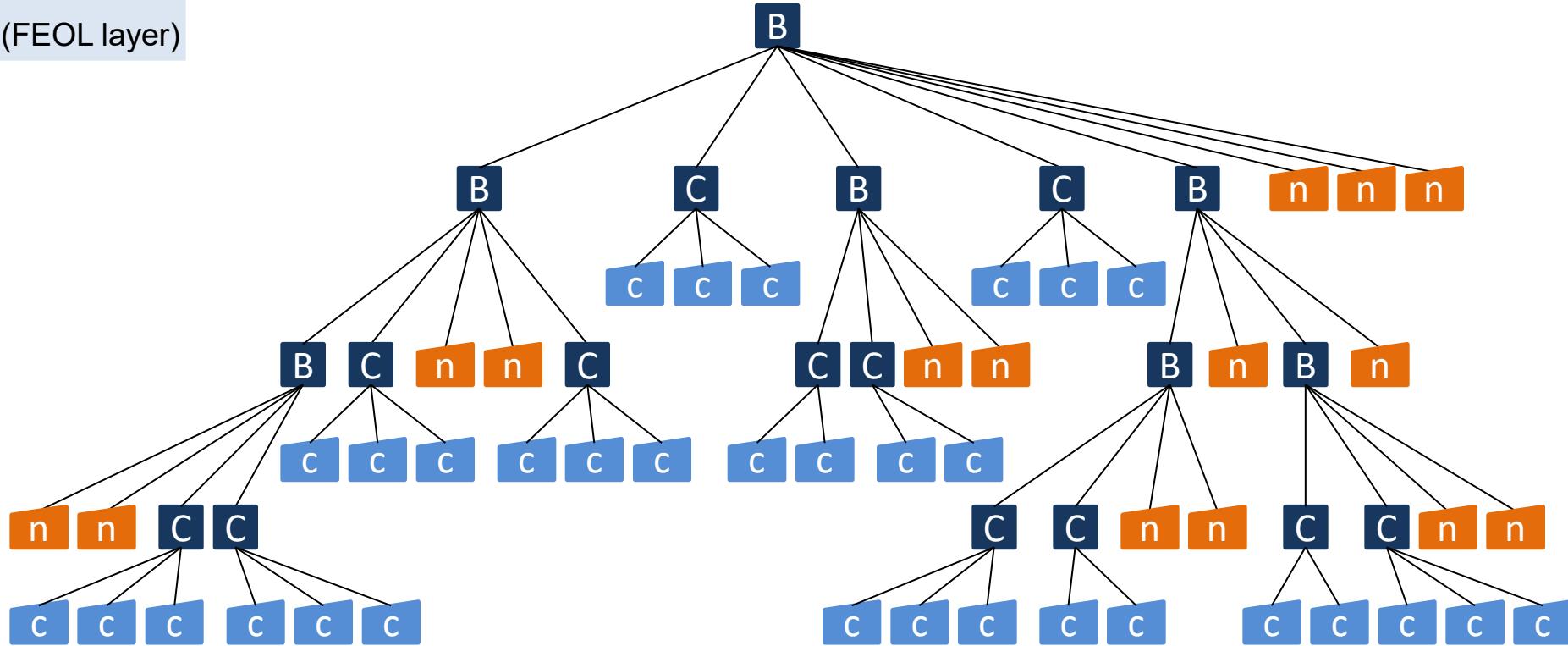
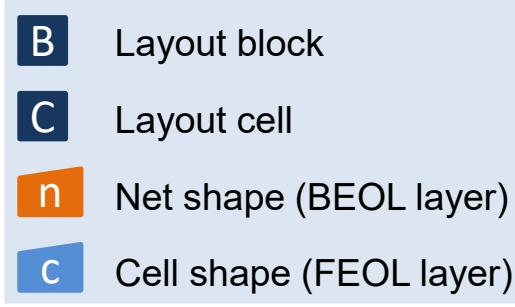
(a)

(b)

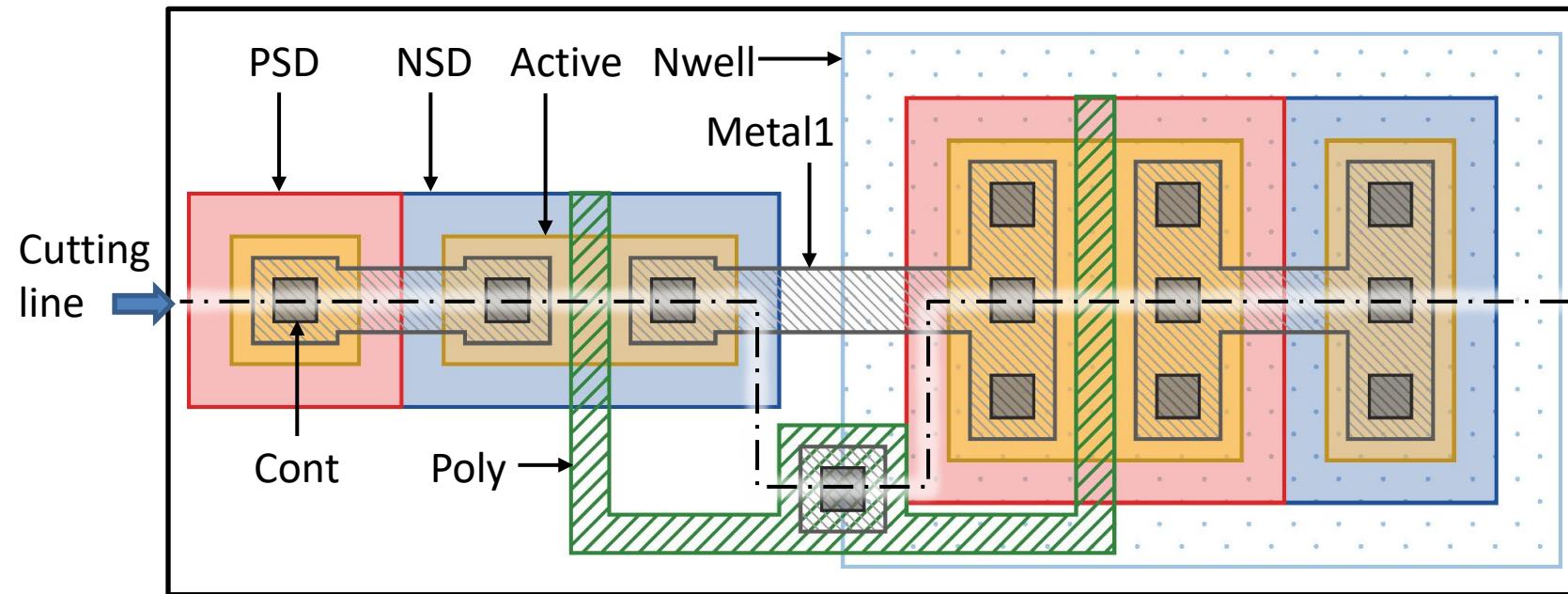
(c)

(d)

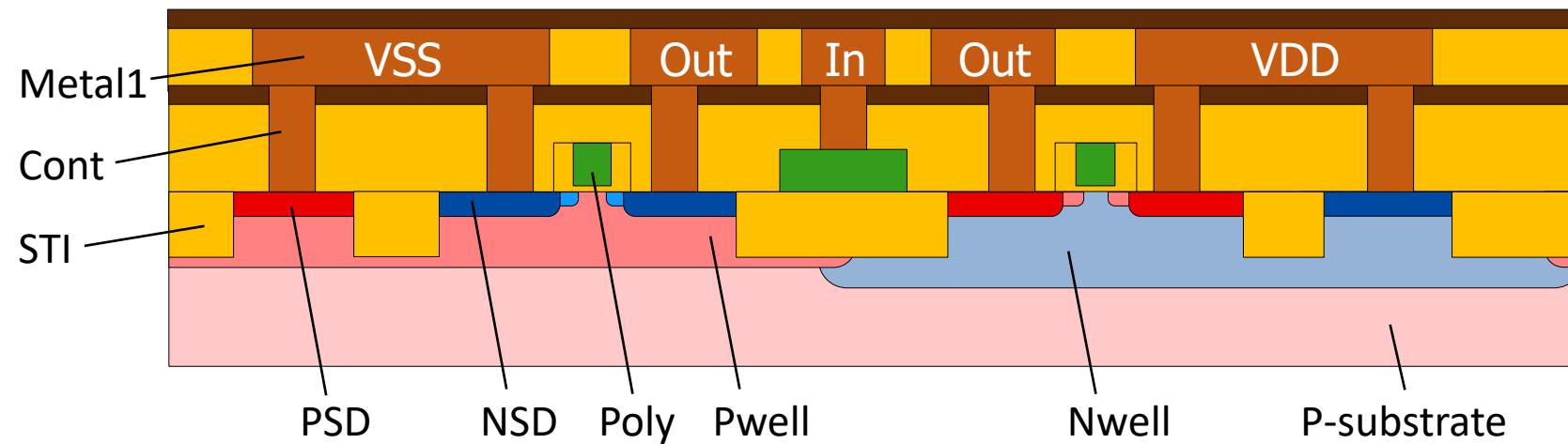
(e)



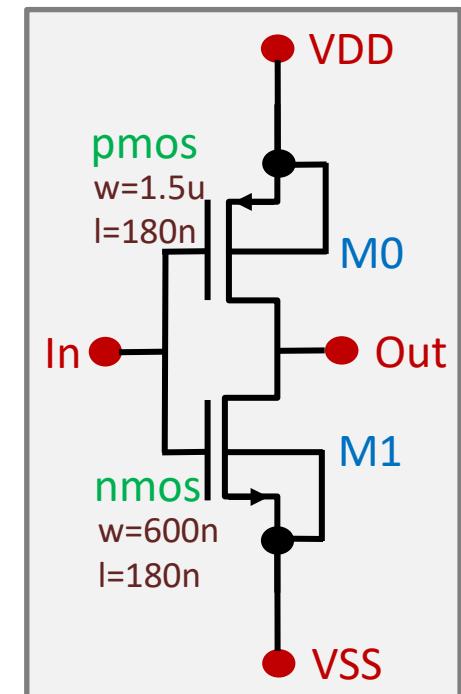
## Layout

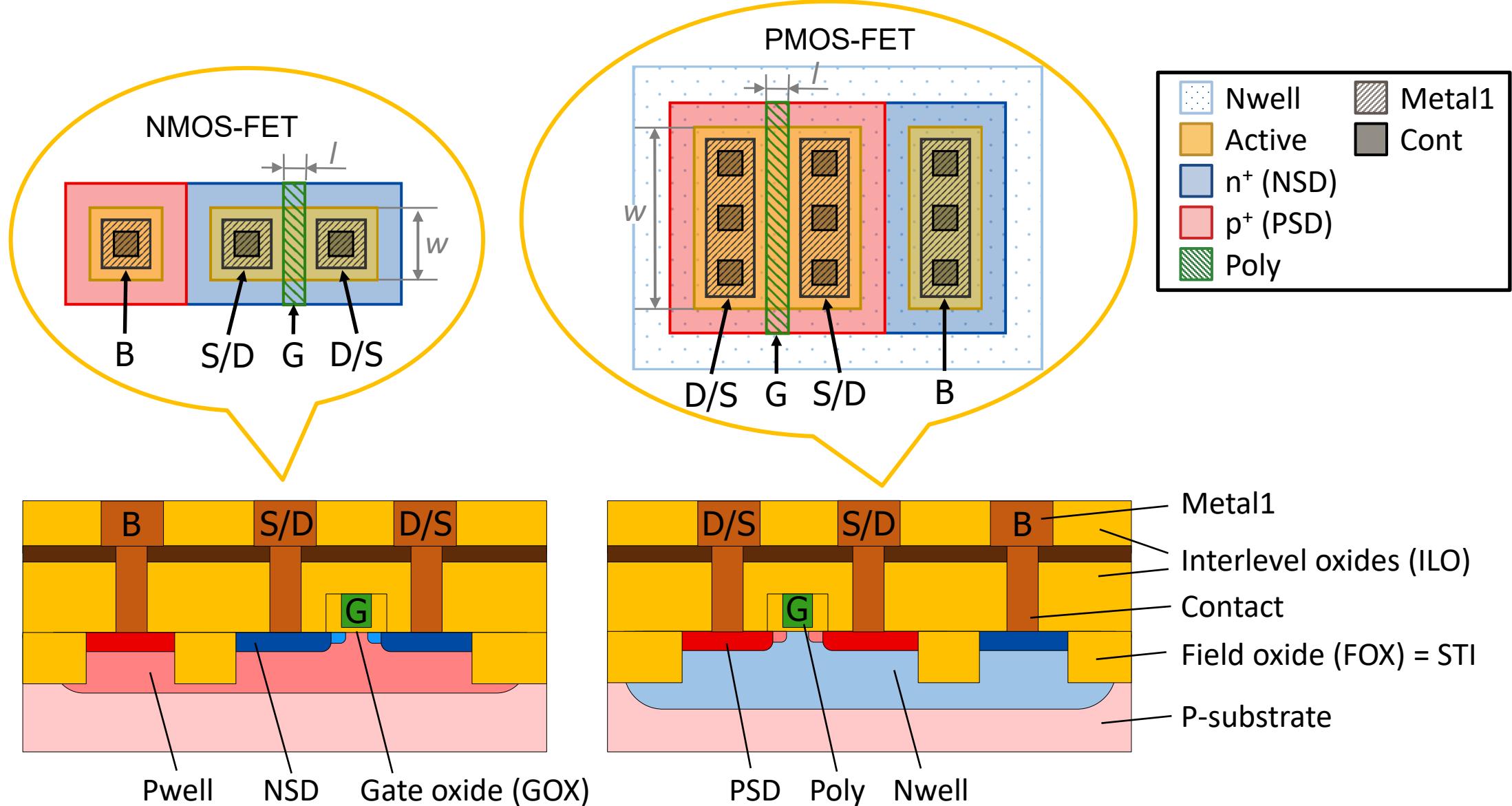


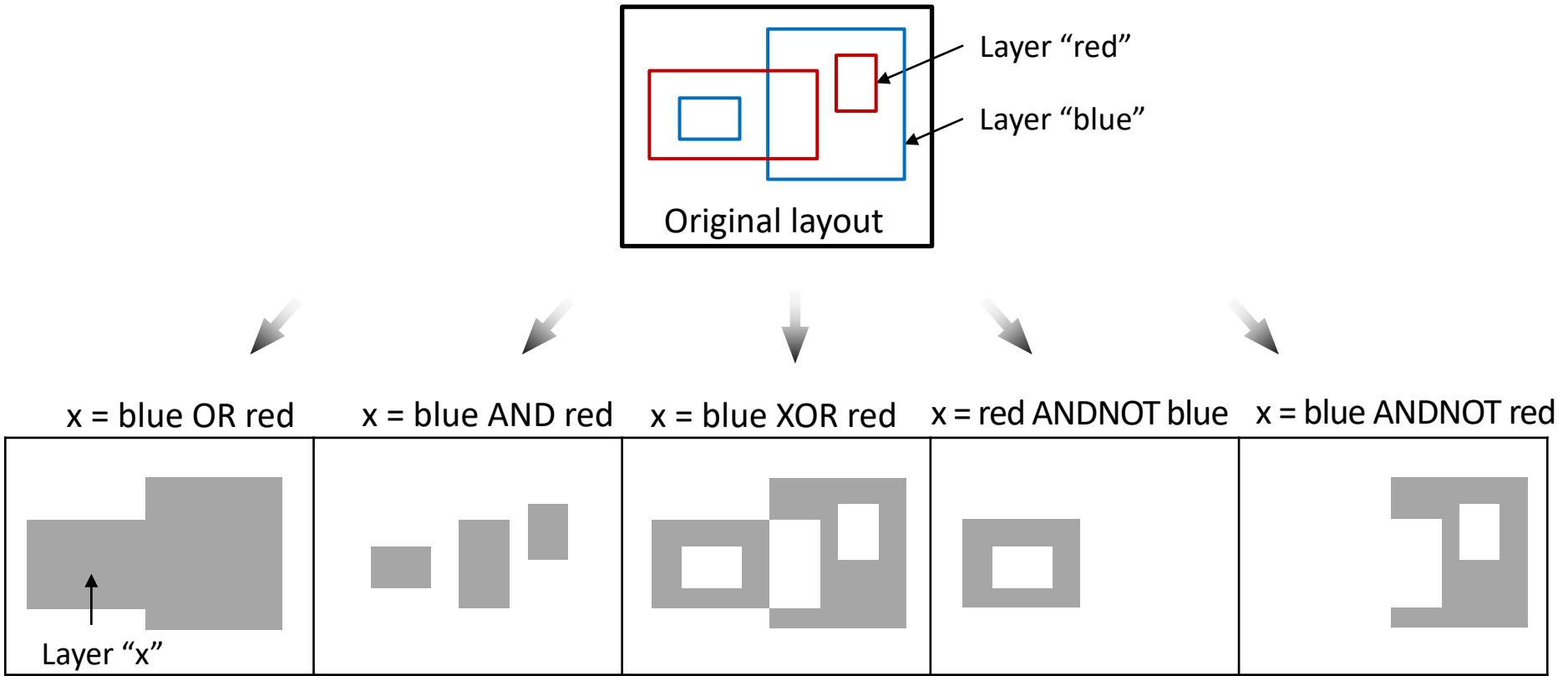
## Sectional view

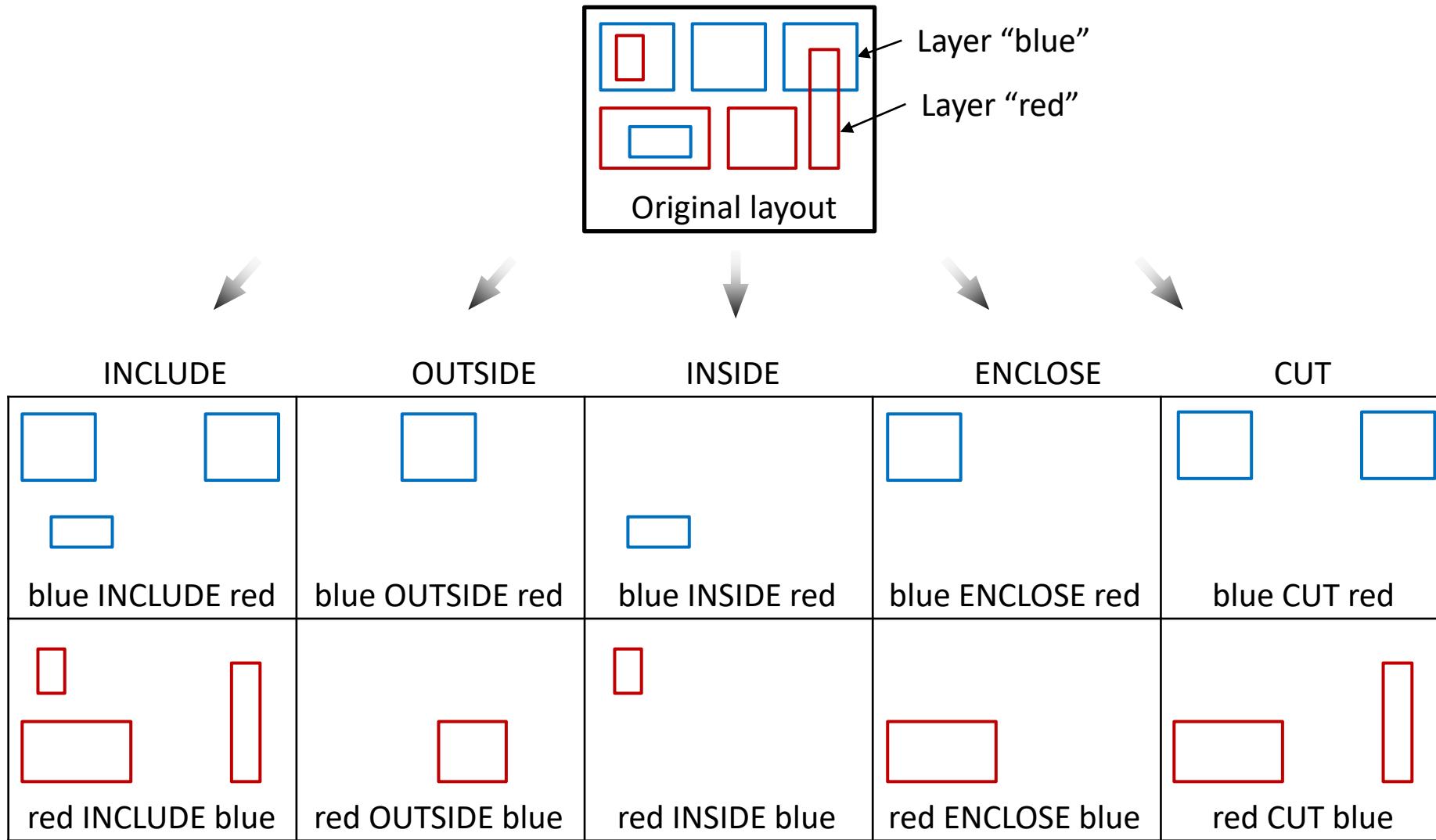


## Circuit diagram

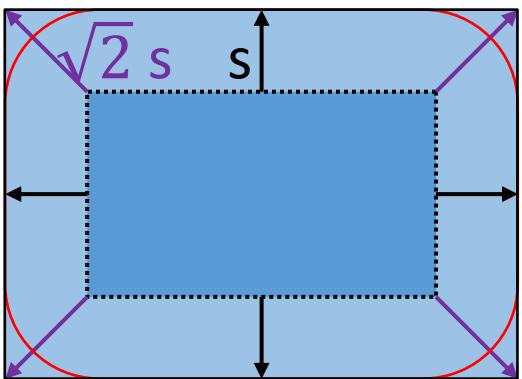




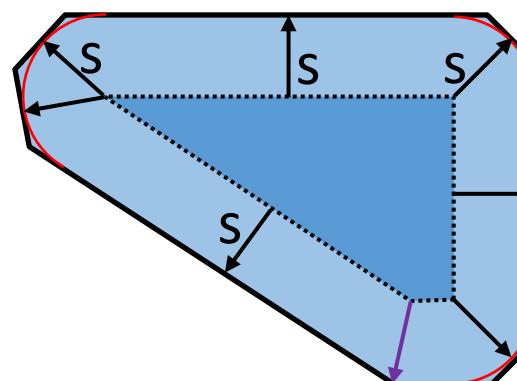
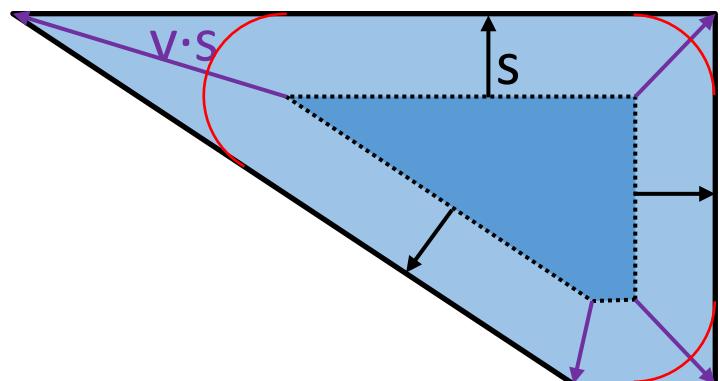
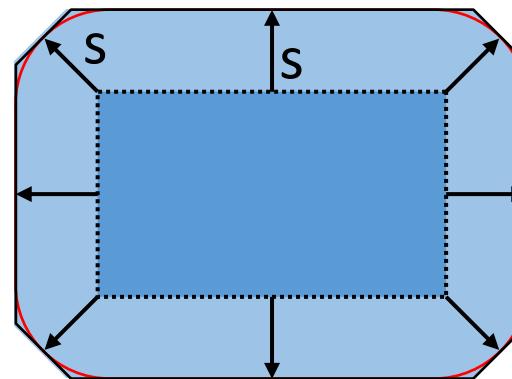


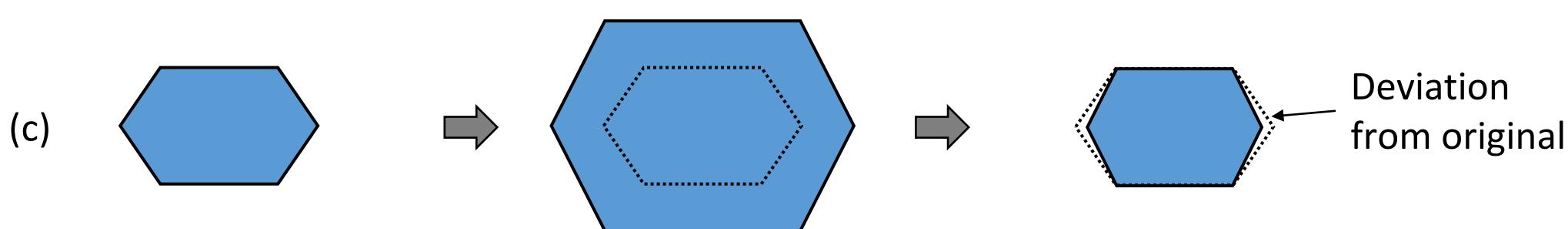
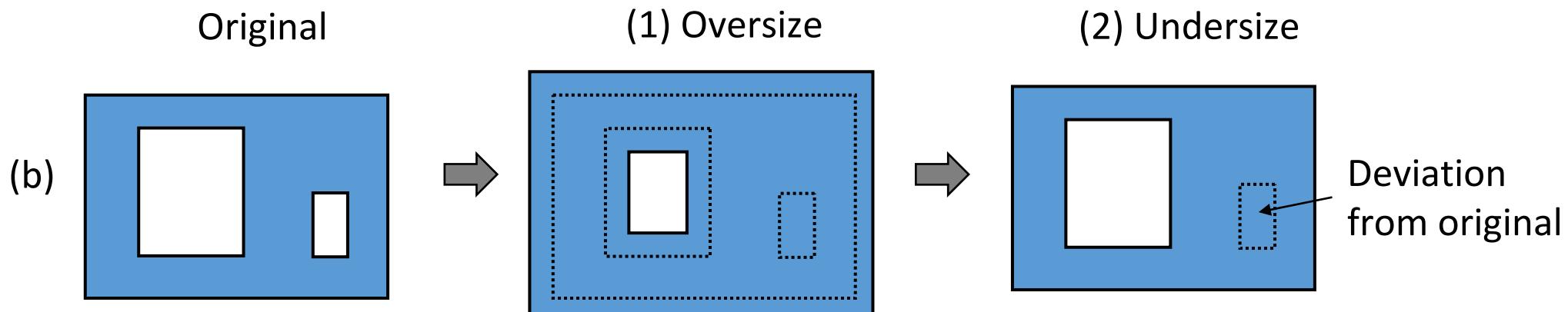
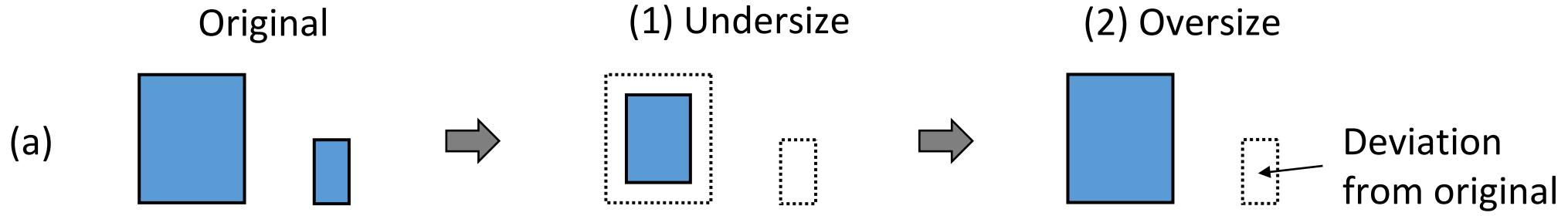


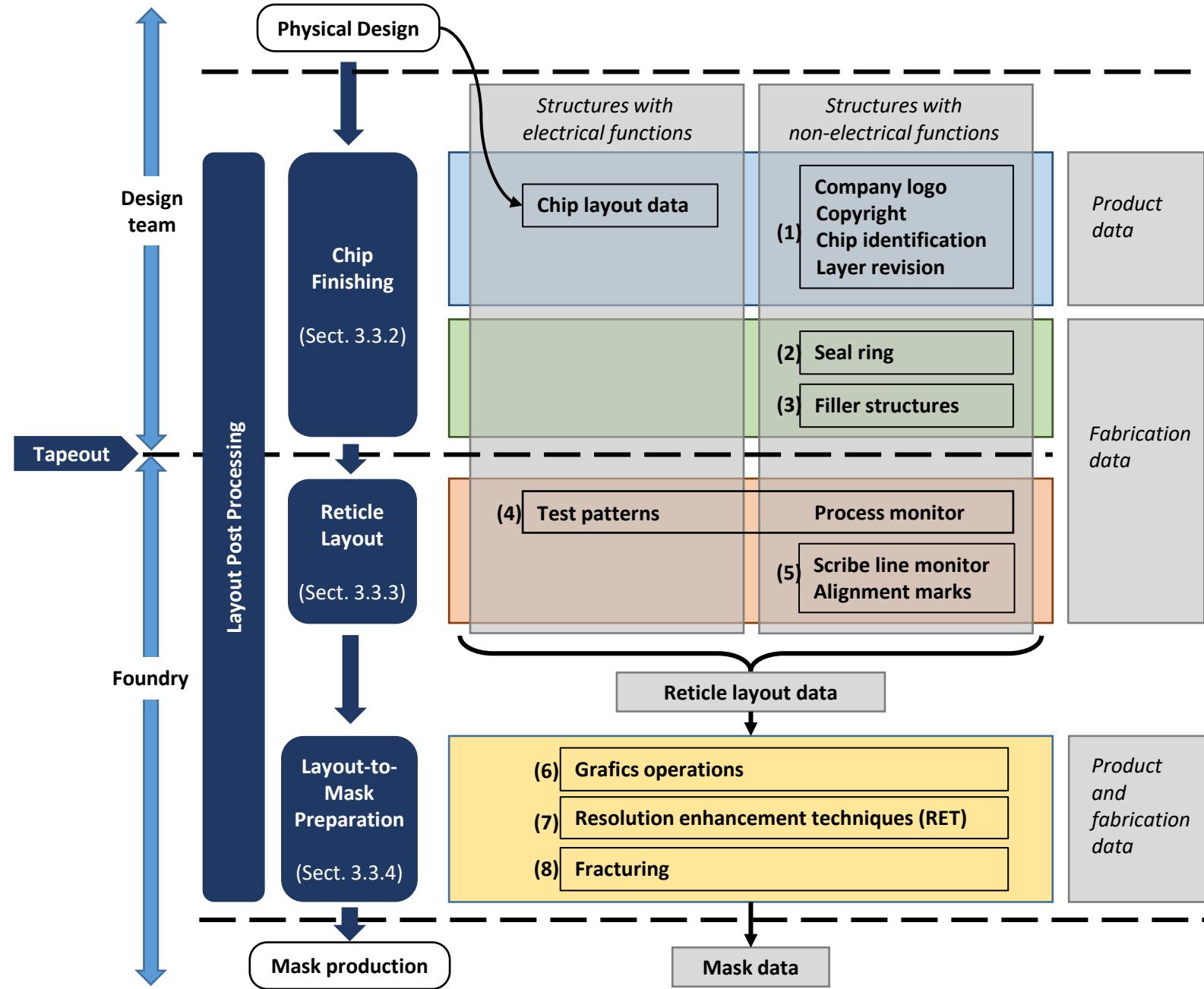
## Sizing without beveling

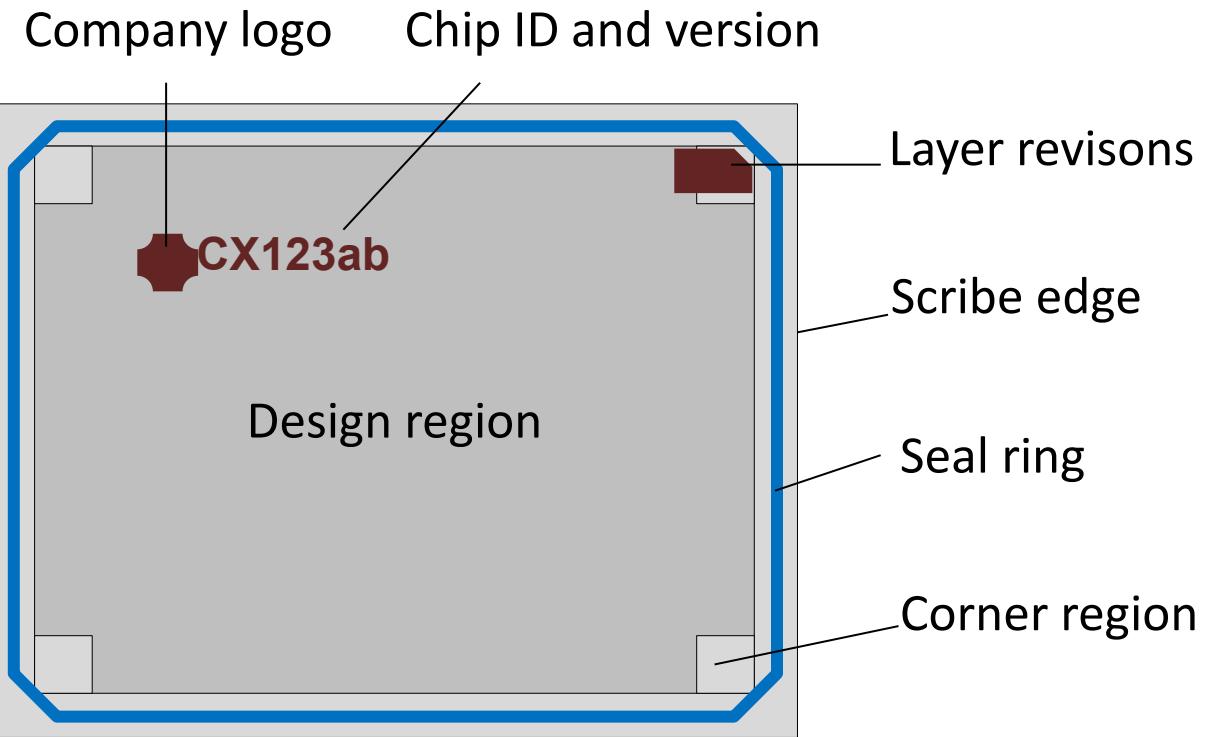


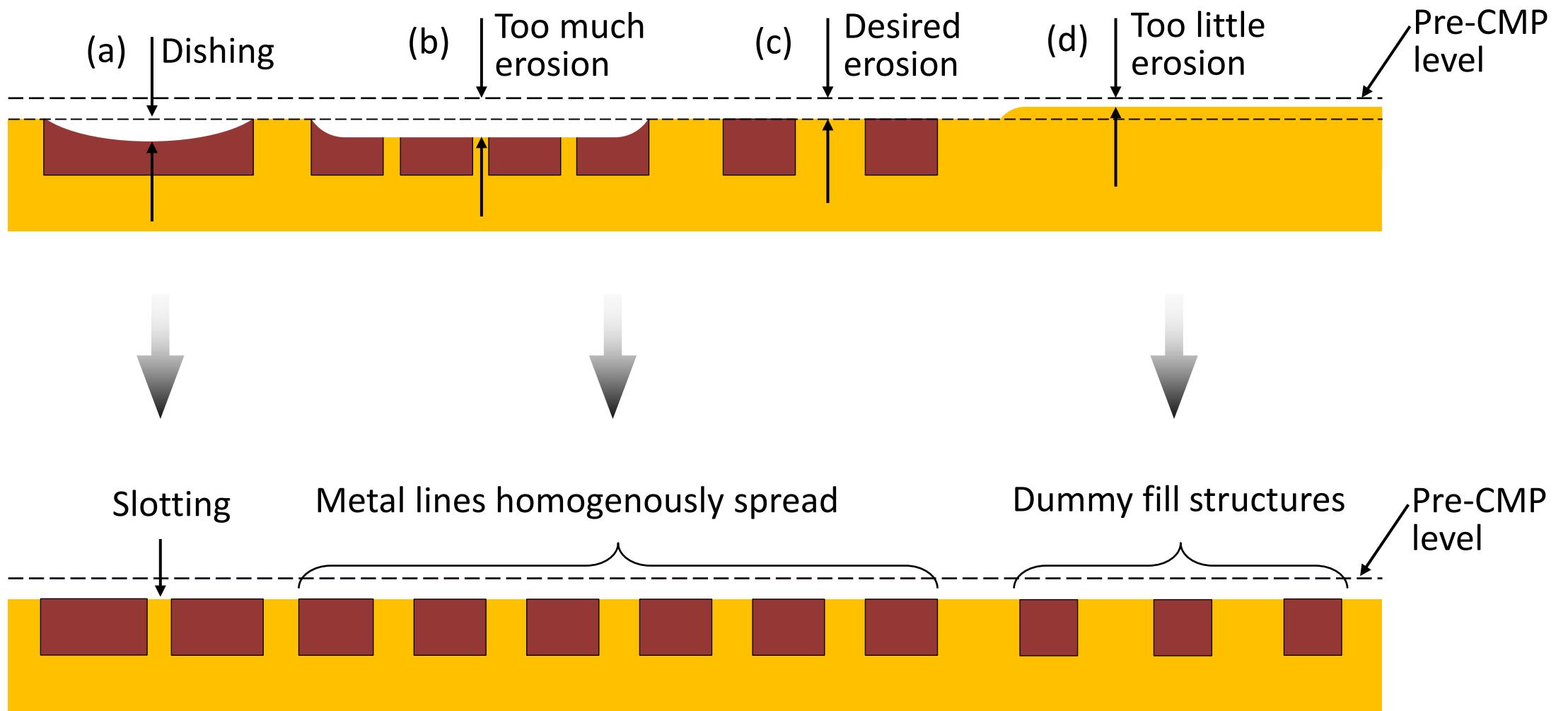
## Sizing with beveling

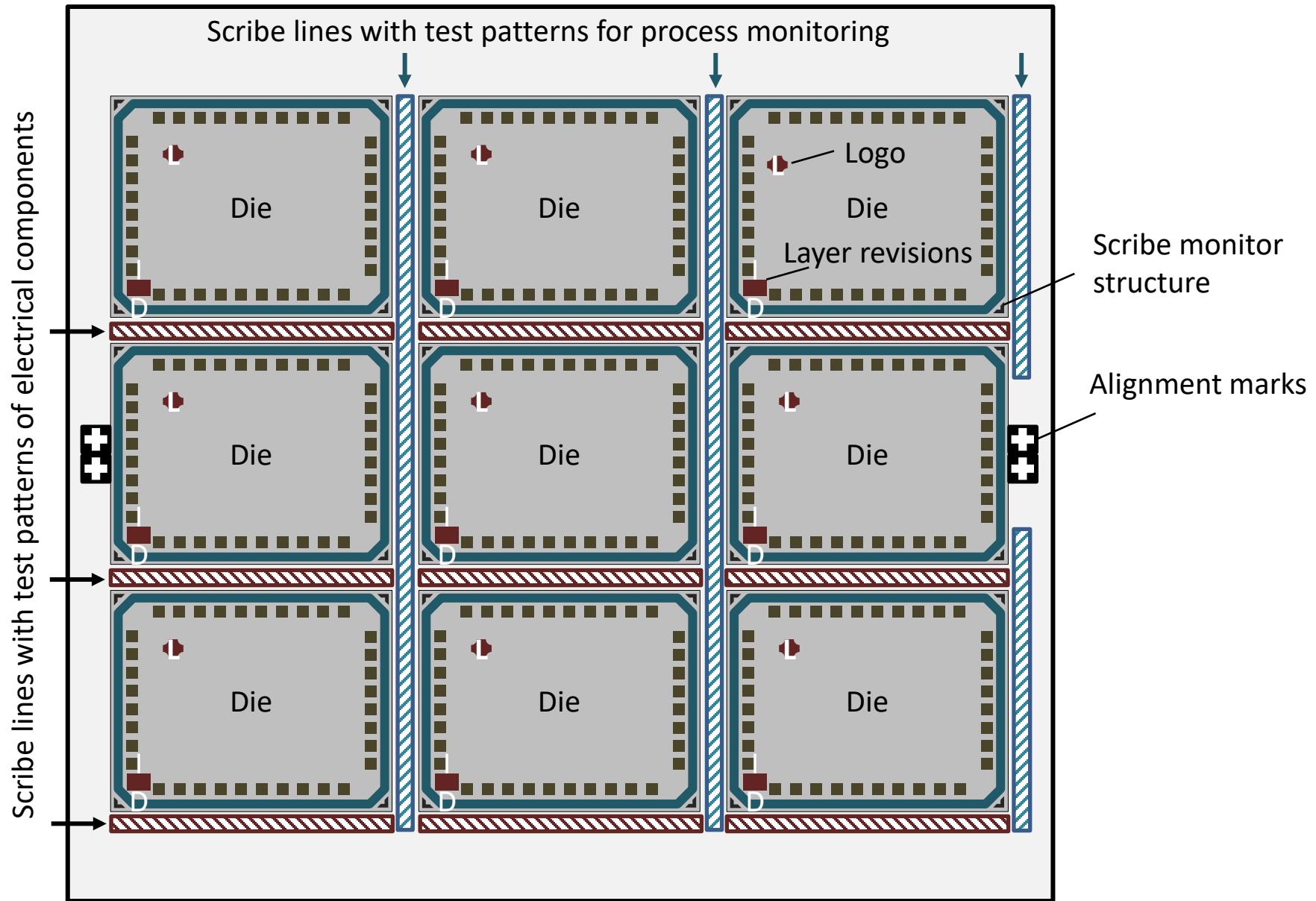


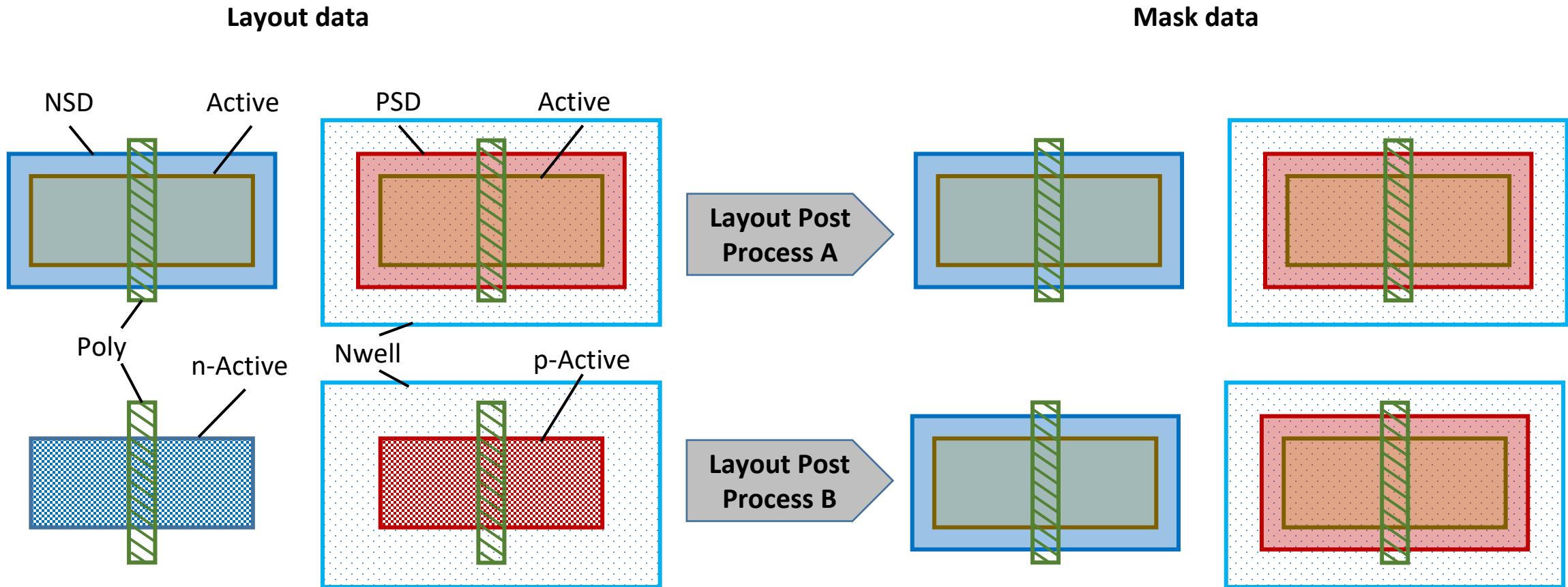


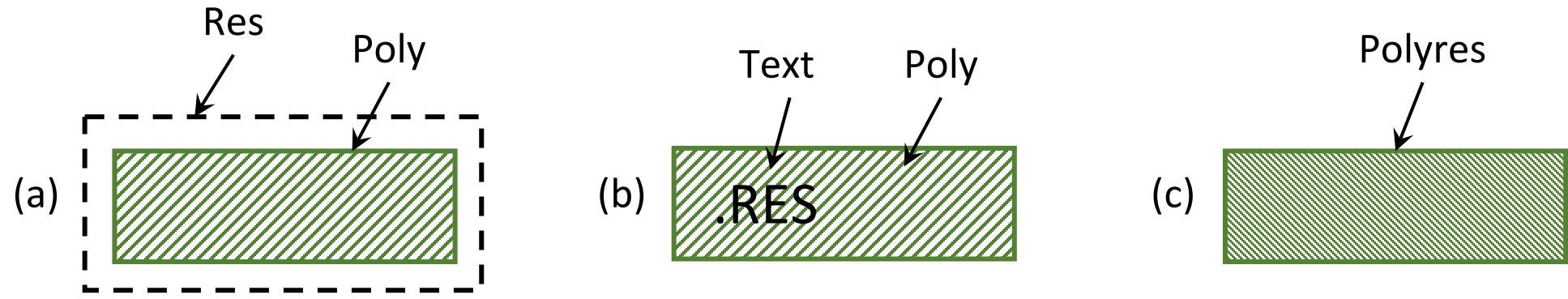




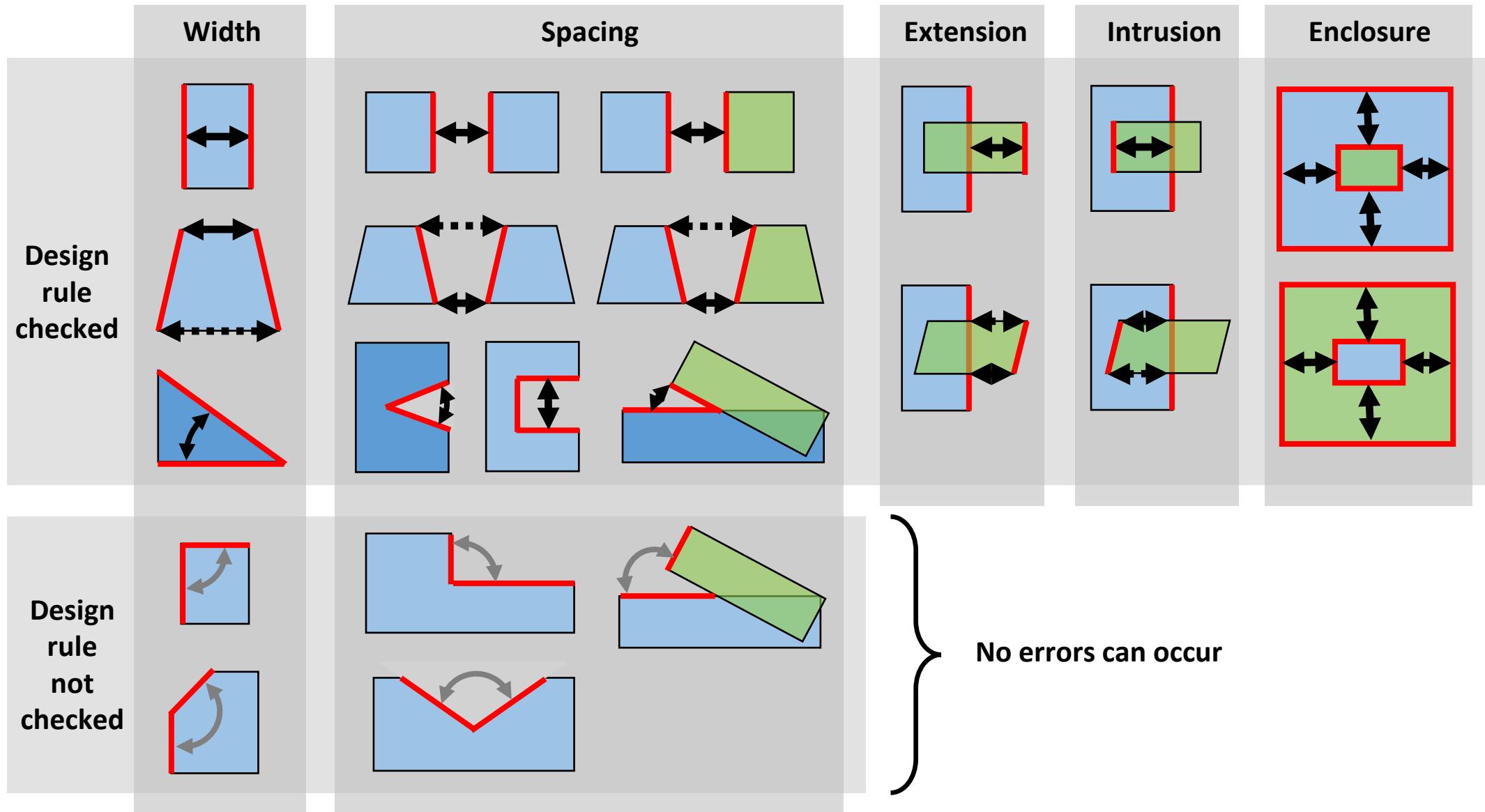


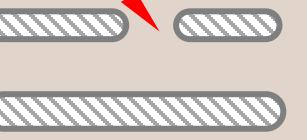
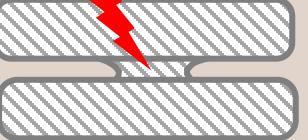




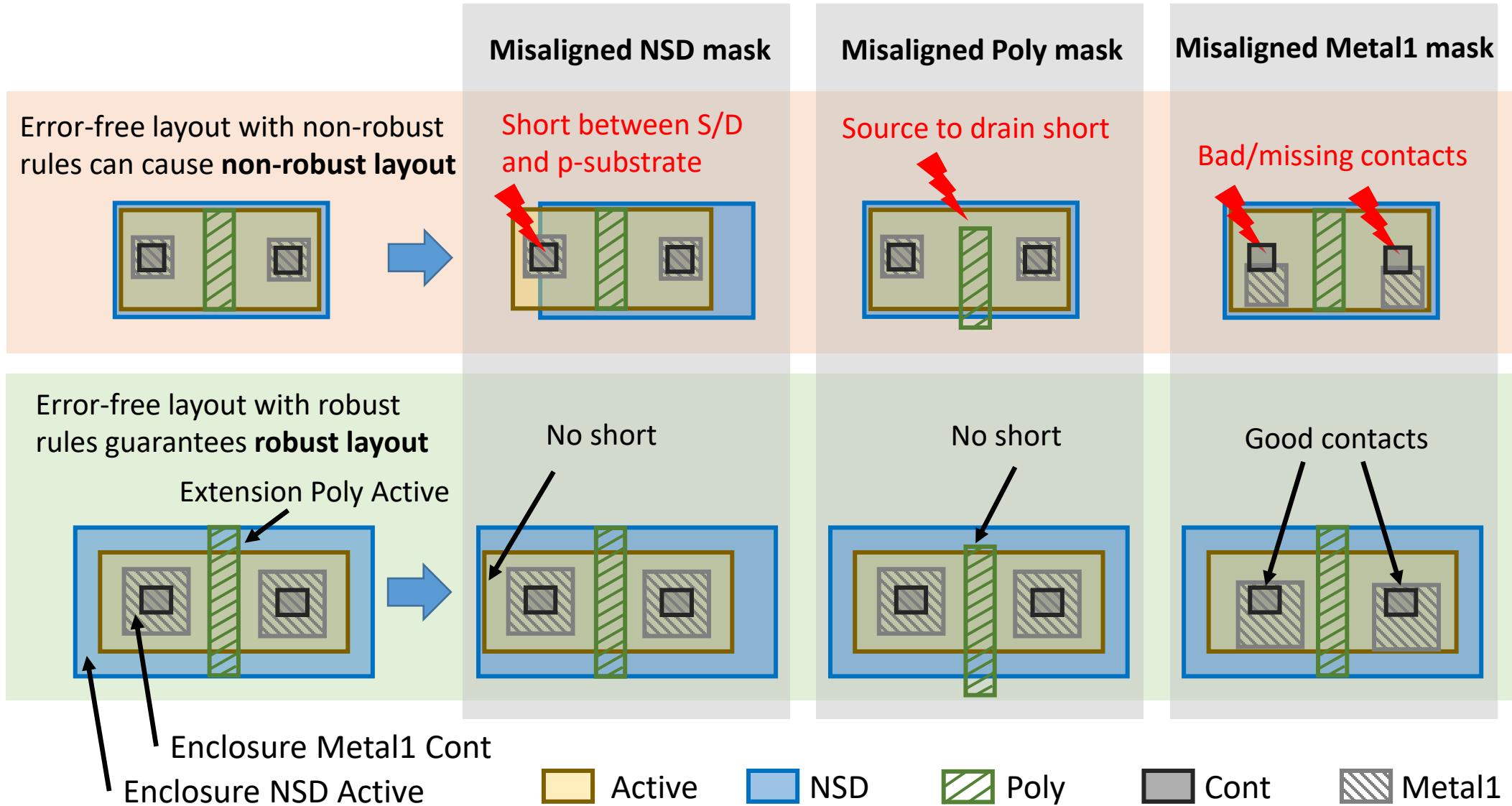


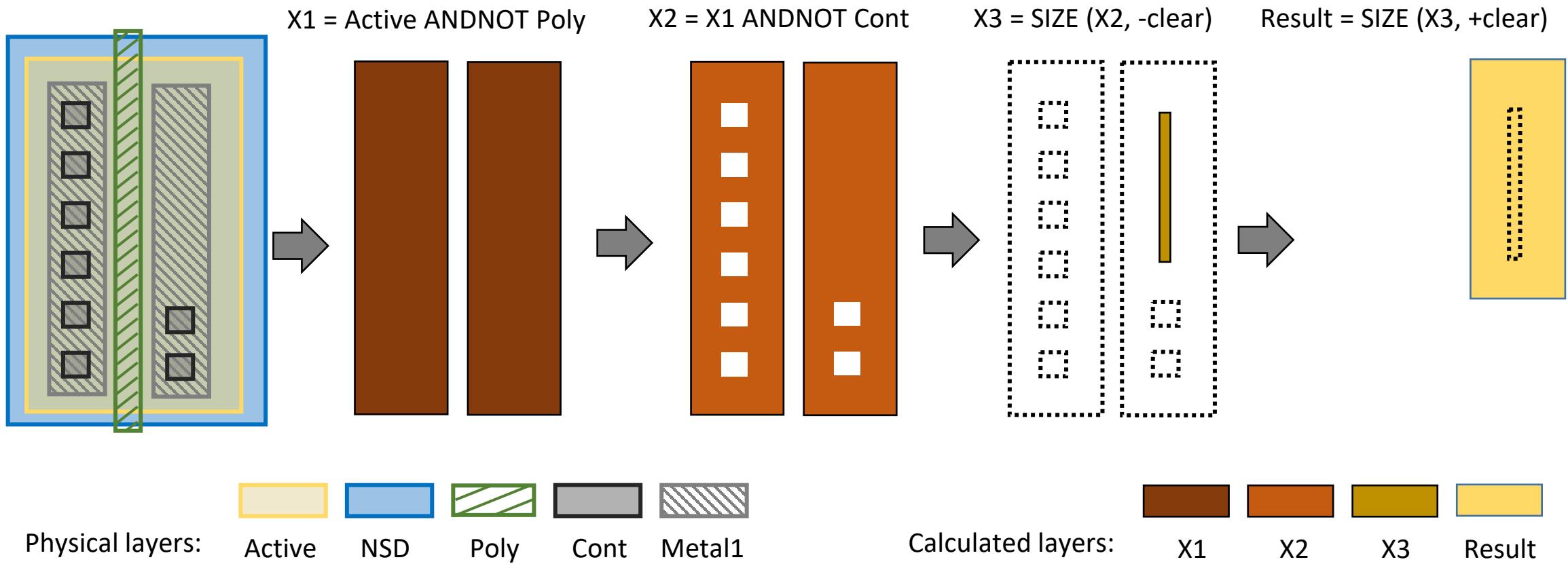
Design Rule	Relationship between edges	Number of shapes	Number of layers
Width	Inside / inside	1	1
Spacing	Outside / outside	(a) 1 or 2 (b) 2	(a) 1 (b) 2
Extension	Inside / outside	2	2
Intrusion	Inside / inside	2	2
Enclosure	Outside / inside	2	2

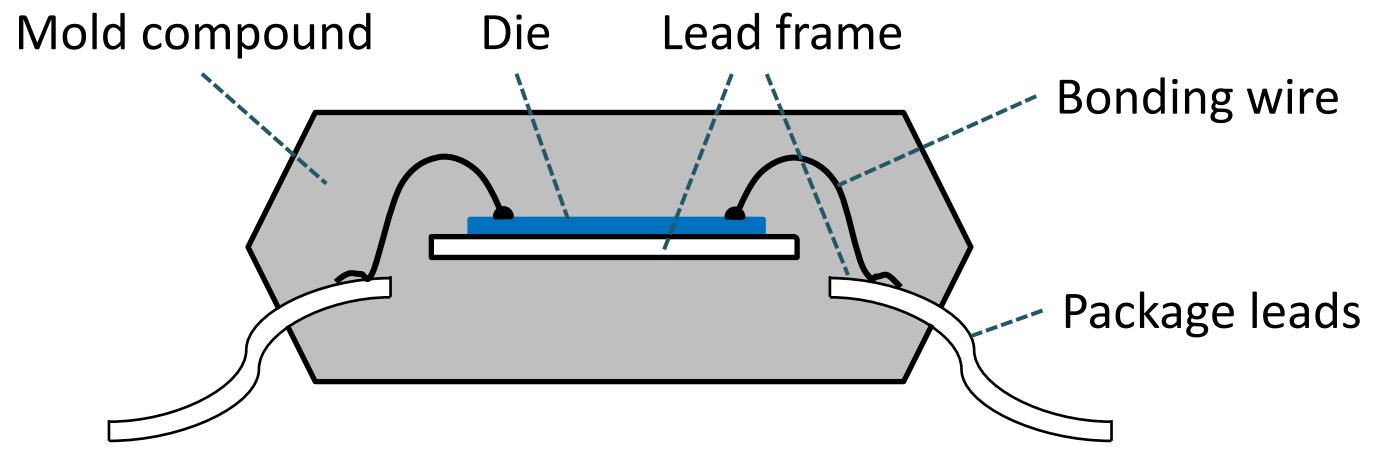


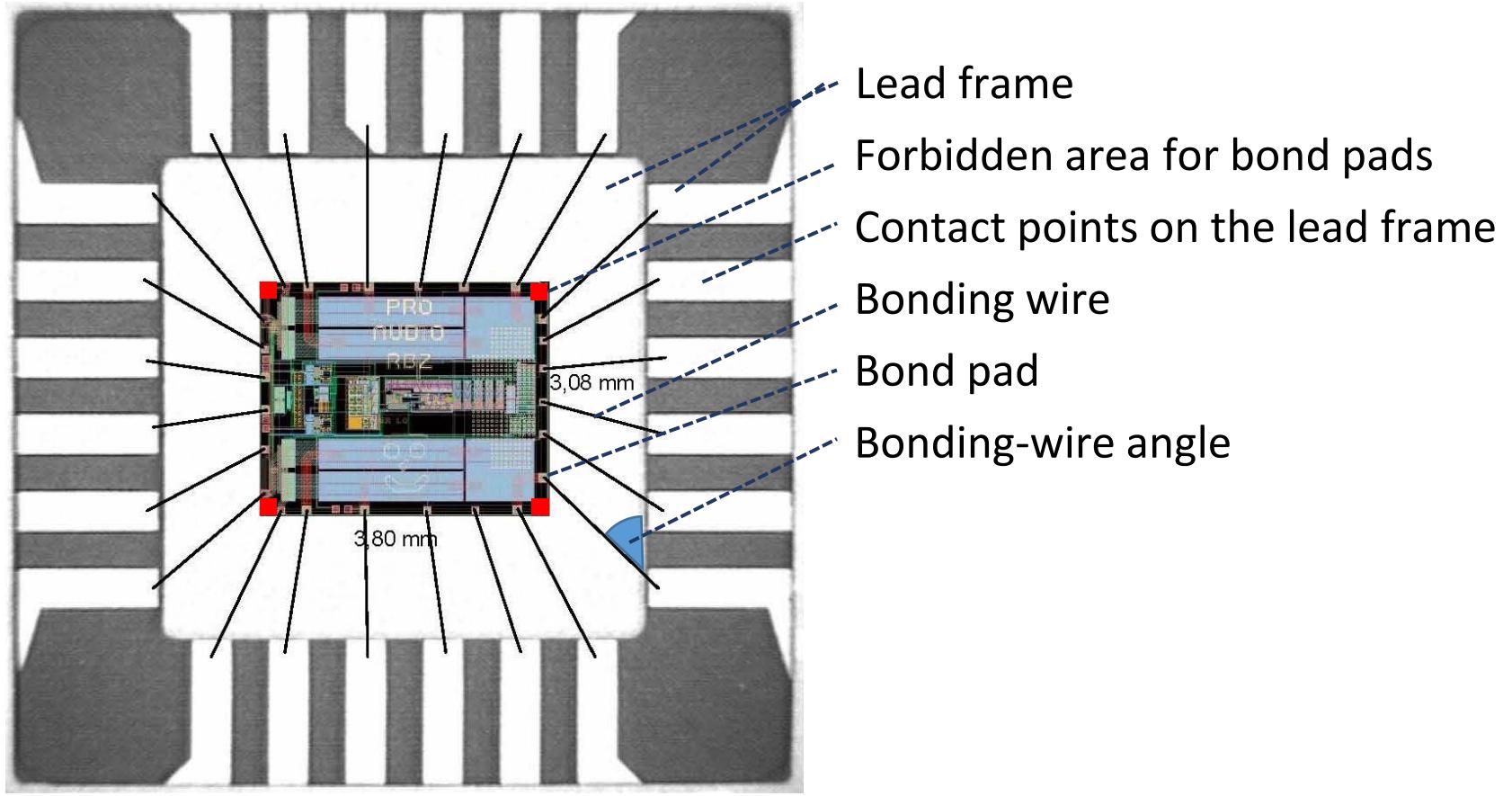
Error-free layout with non-robust rules can cause <b>non-robust layout</b>	Manufacturing tolerance ↓	Manufacturing tolerance ↑
<p>Minimum width</p> <p>Minimum spacing</p> 	<p>Break</p> 	<p>Short-circuit</p> 
<p>Error-free layout with robust rules guarantees <b>robust layout</b></p> <p>Minimum width</p> <p>Minimum spacing</p> 	<p>No break</p> 	<p>No short-circuit</p> 

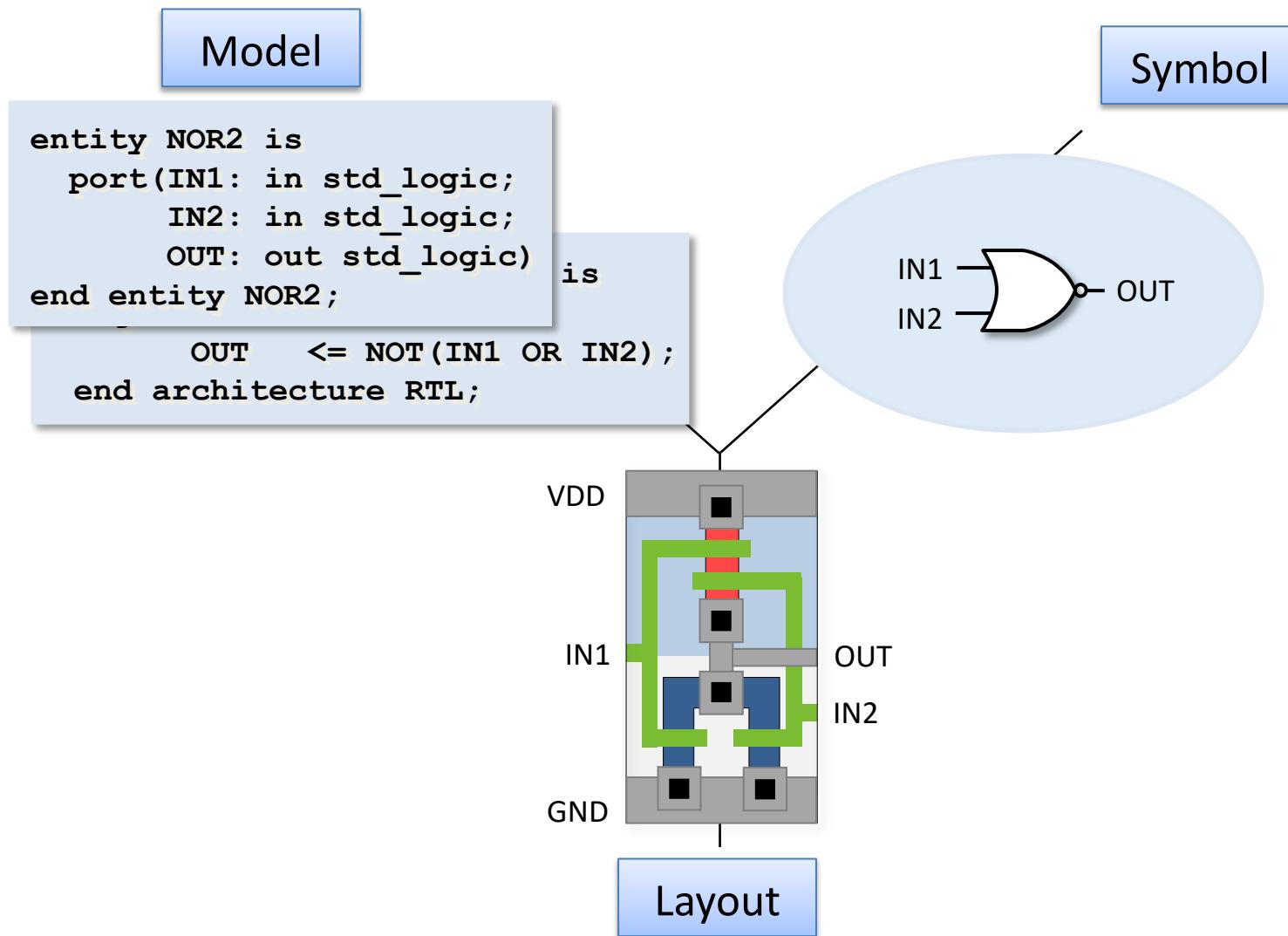
 Metal1

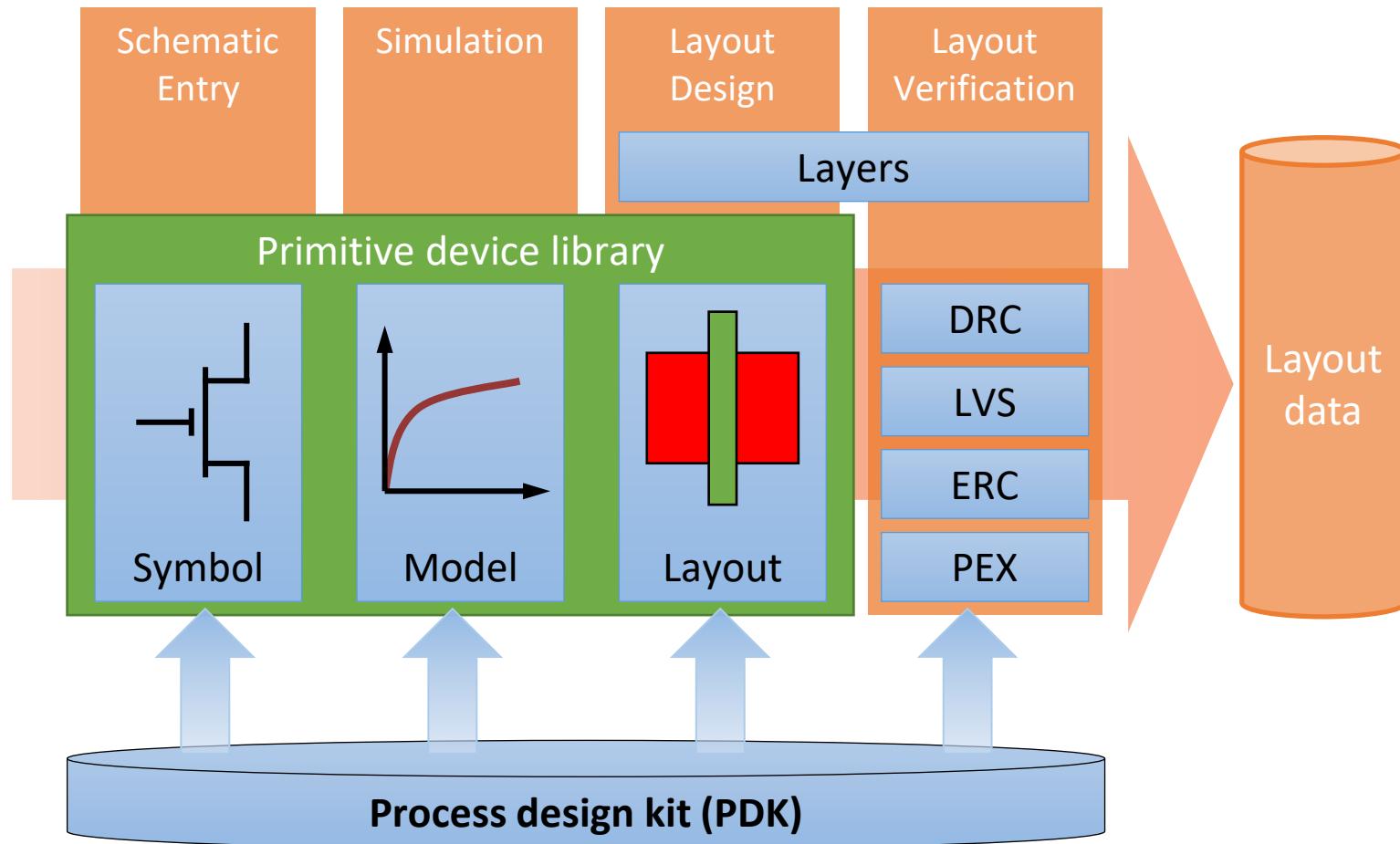


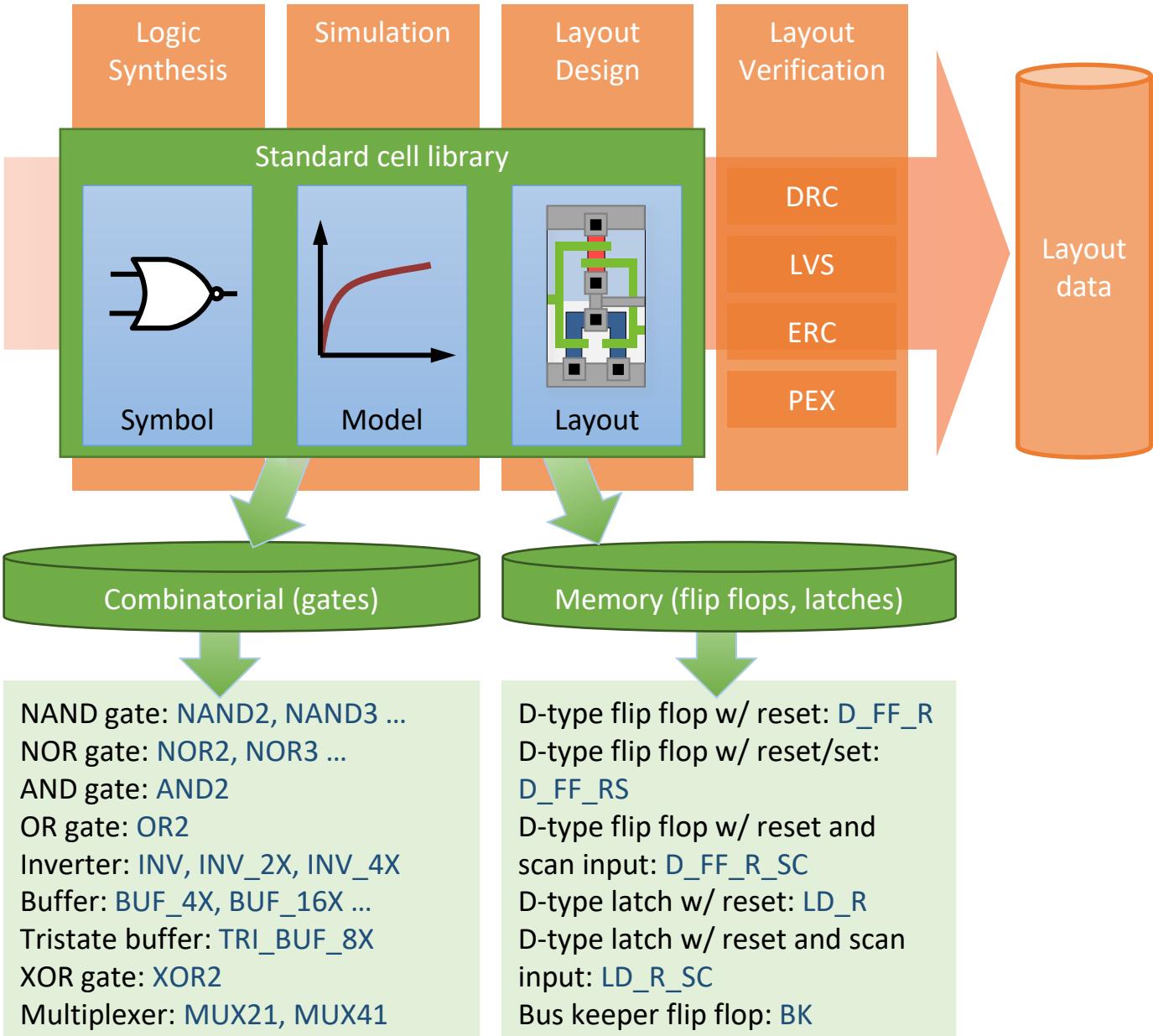


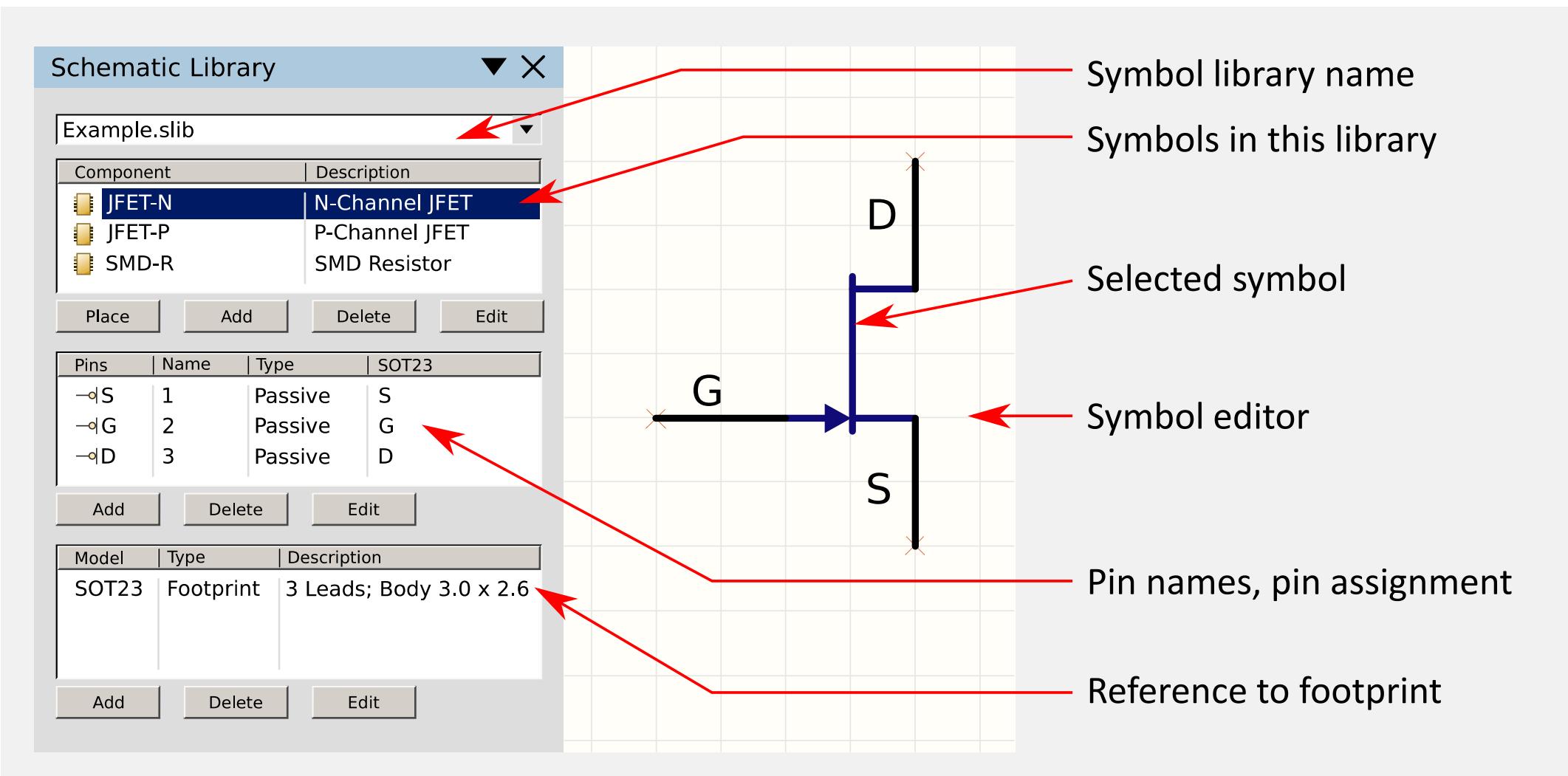


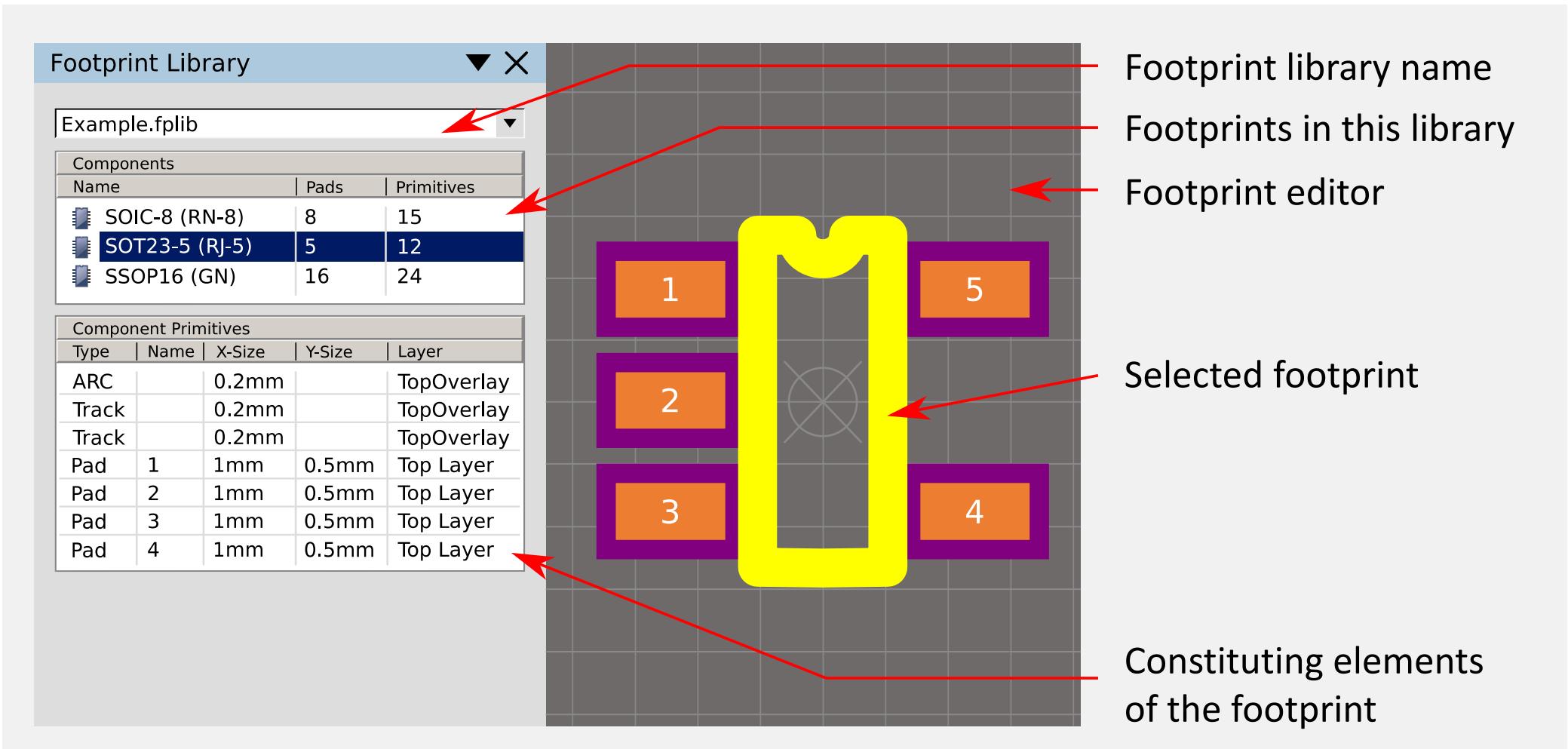












**Model Library**

▼ X

```
*****  
* Copyright (c) 2000-2012 Linear Technology Corporation. *  
* All rights reserved.  
*****  
  
.model 1N4001 D  
+Is=14.11n N=1.984 Rs=33.89m Ikf=94.81  
+Xti=3 Eg=1.11 Cjo=25.89p M=.44  
+Vj=.3245 Fc=.5 Bv=75 Ibv=10u Tt=5.7u  
+Iave=1 Vpk=50 mfg=GI type=silicon
```

Model name

Model category (diode)

Device specific parameter set

