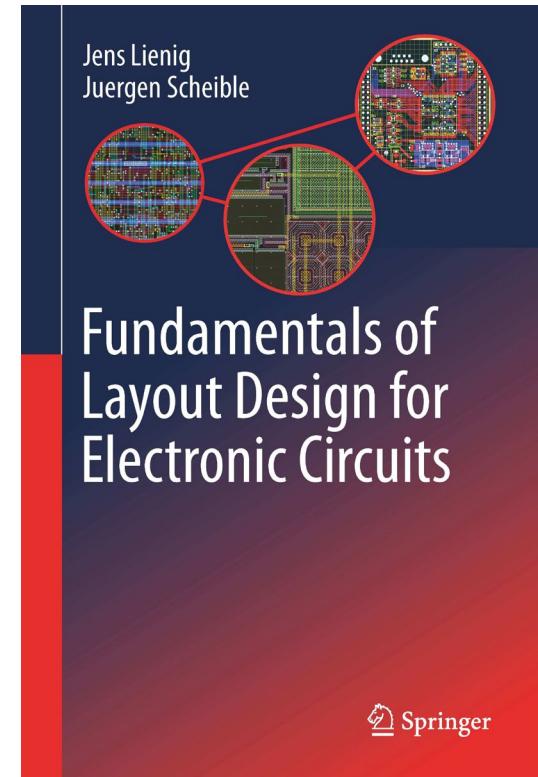


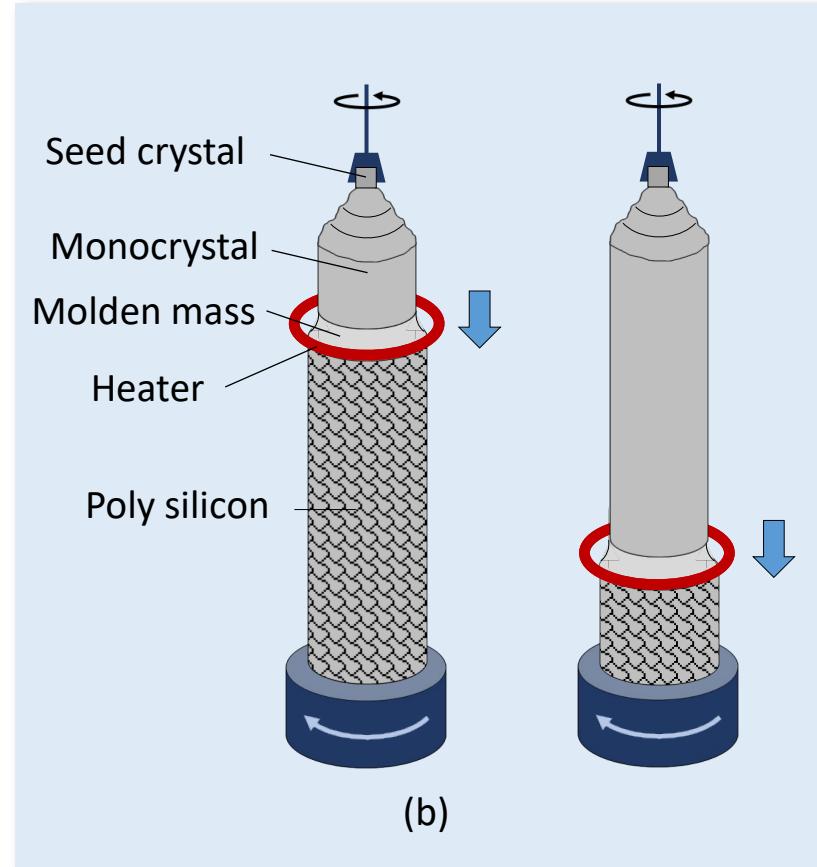
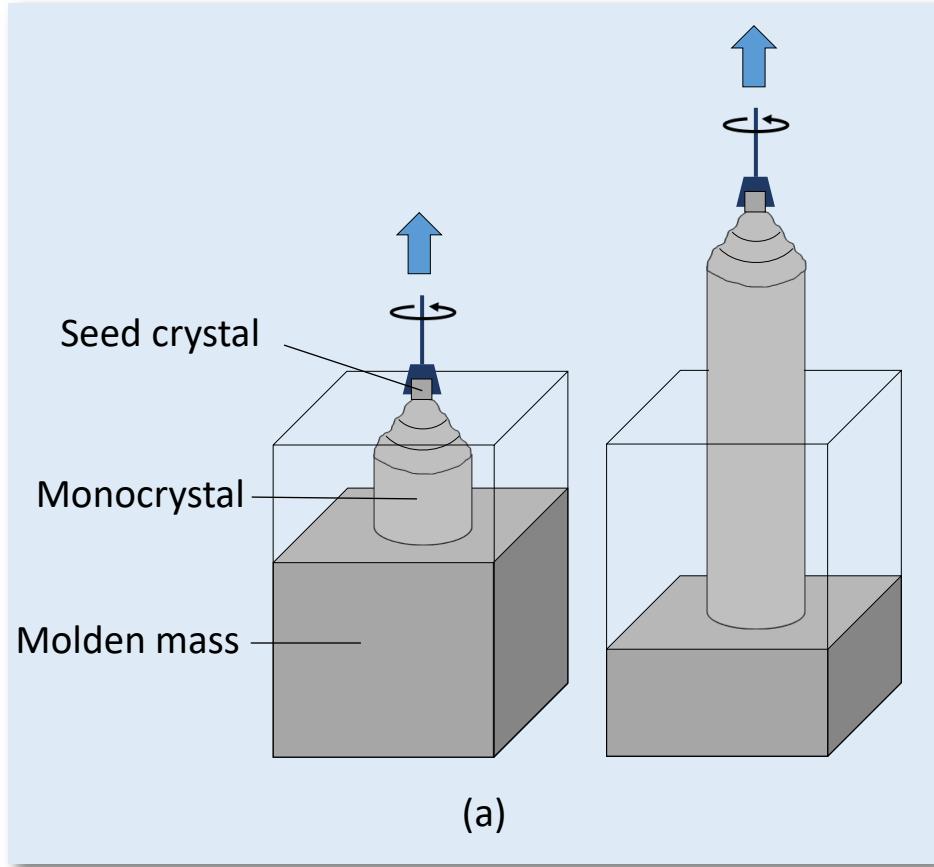
Chapter 2: Technology Know-How: From Silicon to Devices

- 2.1 Fundamentals of IC Fabrication
- 2.2 Base Material Silicon
- 2.3 Photolithography
- 2.4 Imaging Errors
- 2.5 Applying and Structuring Oxide Layers
- 2.6 Doping
- 2.7 Growing and Structuring Silicon Layers
- 2.8 Metallization
- 2.9 CMOS Standard Process



Chapter 2: Technology Know-How: From Silicon to Devices

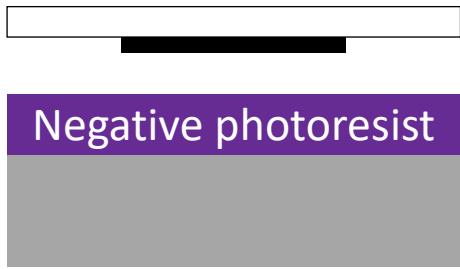
2.1	Fundamentals of IC Fabrication		
2.2	Base Material Silicon		
2.3	Photolithography	2.7	Growing and Structuring Silicon Layers
	2.3.1 Fundamentals		2.7.1 Homoepitaxy
	2.3.2 Photoresist		2.7.2 Heteroepitaxy and Polysilicon
	2.3.3 Photomasks and Exposure		2.7.3 Reference to Physical Design
	2.3.4 Alignment and Alignment Masks	2.8	Metallization
	2.3.5 Reference to Physical Design		2.8.1 Fundamentals
2.4	Imaging Errors		2.8.2 Metallization Structures Without Planarization
	2.4.1 Overlay Errors		2.8.3 Metallization Structures with Planarization
	2.4.2 Edge Shifts		2.8.4 Reference to Physical Design
	2.4.3 Diffraction Effects	2.9	CMOS Standard Process
	2.4.4 Reference to Physical Design		2.9.1 Fundamentals: The Field-Effect Transistor
2.5	Applying and Structuring Oxide Layers		2.9.2 Process Options
	2.5.1 Thermal Oxidation		2.9.3 FEOL: Creating Devices
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	2.5.3 Oxide Structuring by Etching		
	2.5.4 Local Oxidation		
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2.6	Doping		
	2.6.1 Background		
	2.6.2 Diffusion		
	2.6.3 Ion Implantation		
	2.6.4 Reference to Physical Design		



Adjust photomask

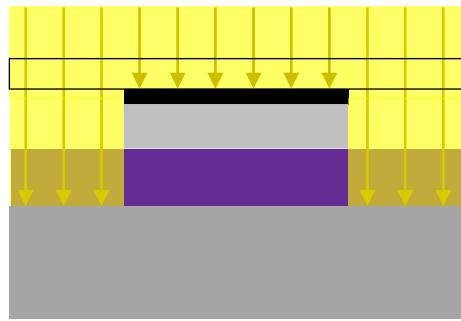
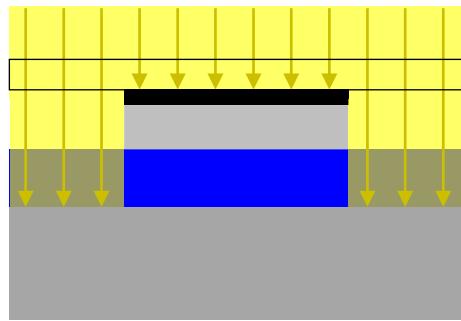


Positive photoresist

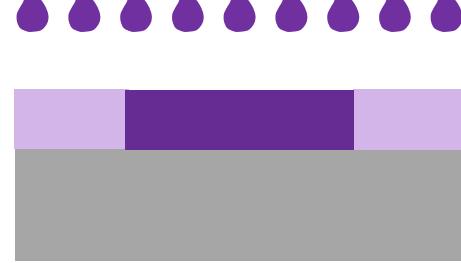
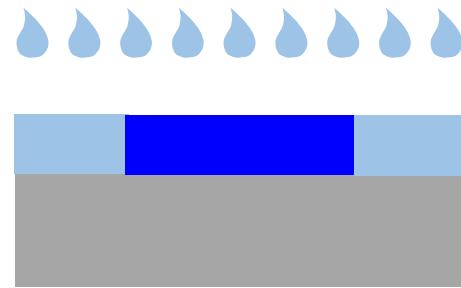


Negative photoresist

Exposure



Development



Developed photoresist

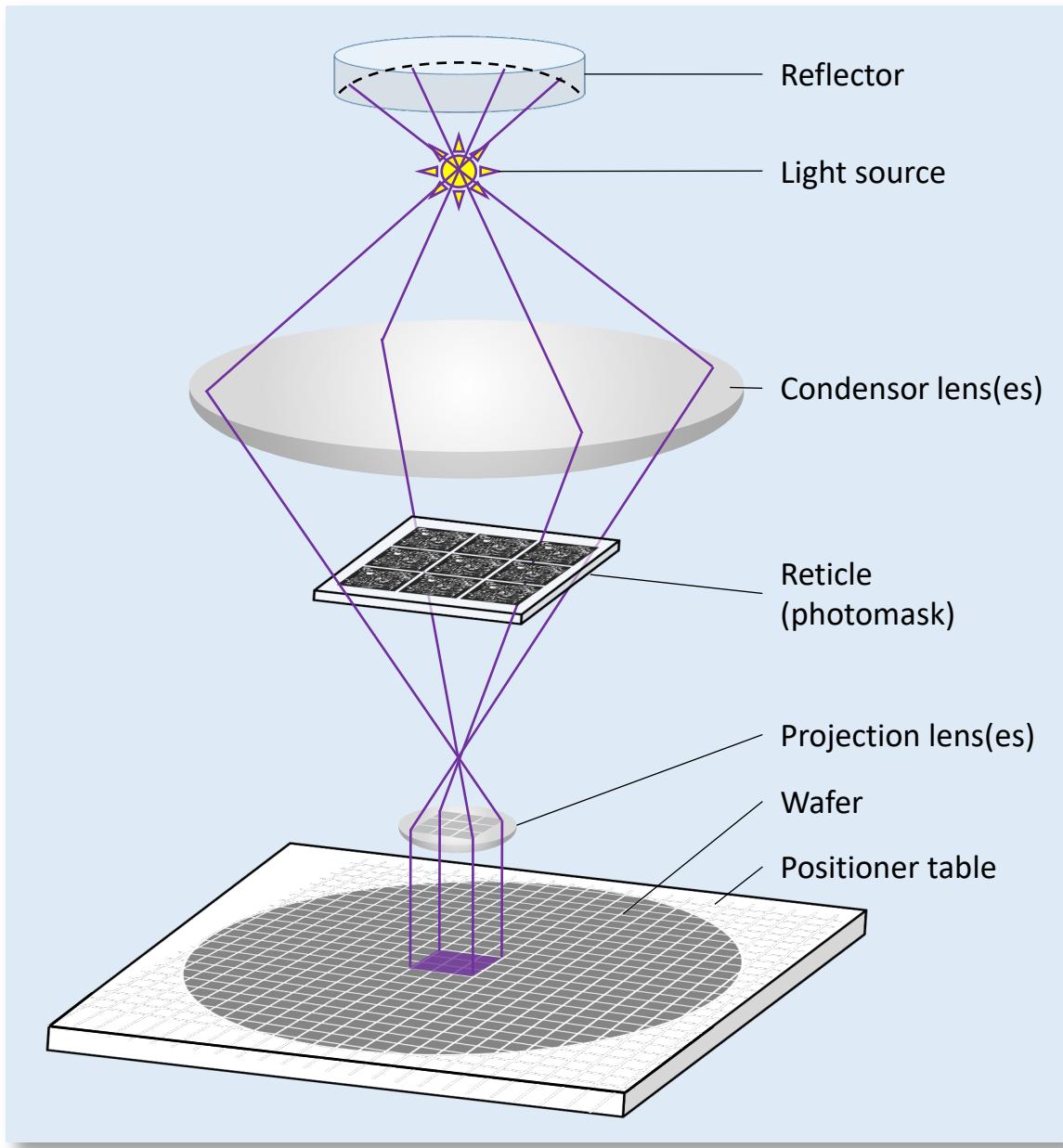


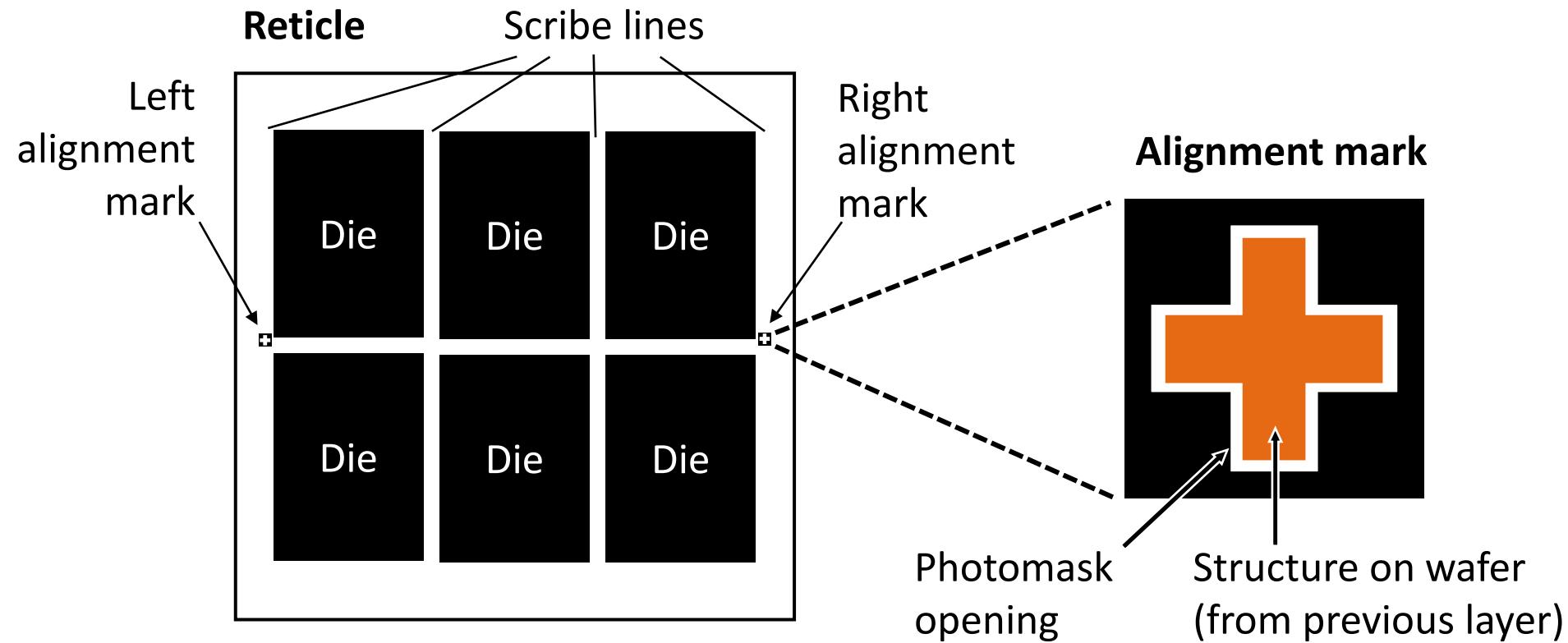
(a)

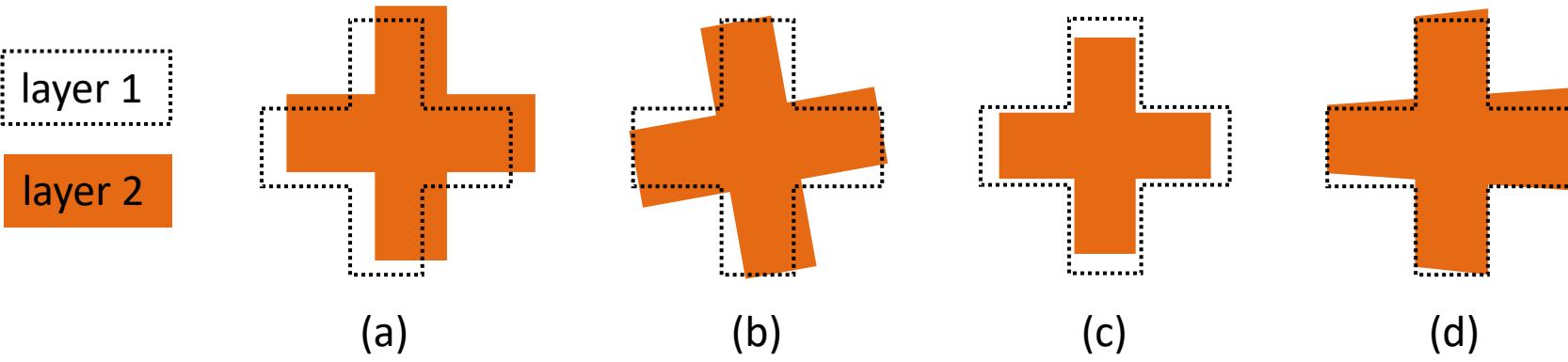
(b)

(c)

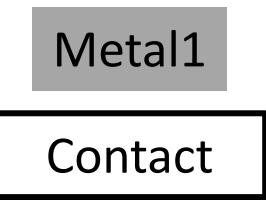
(d)





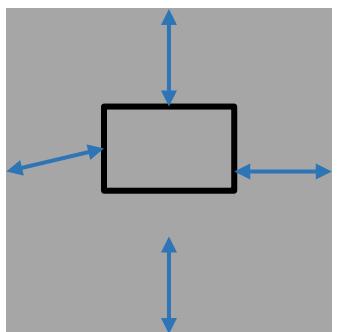


Layers



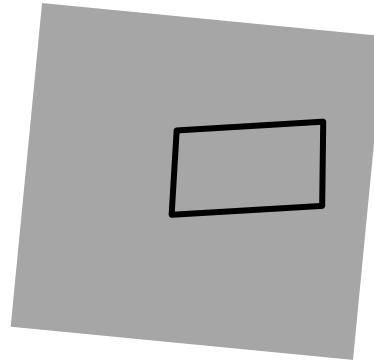
Design rule
Minimal enclosure
Metal1 vs. Contact

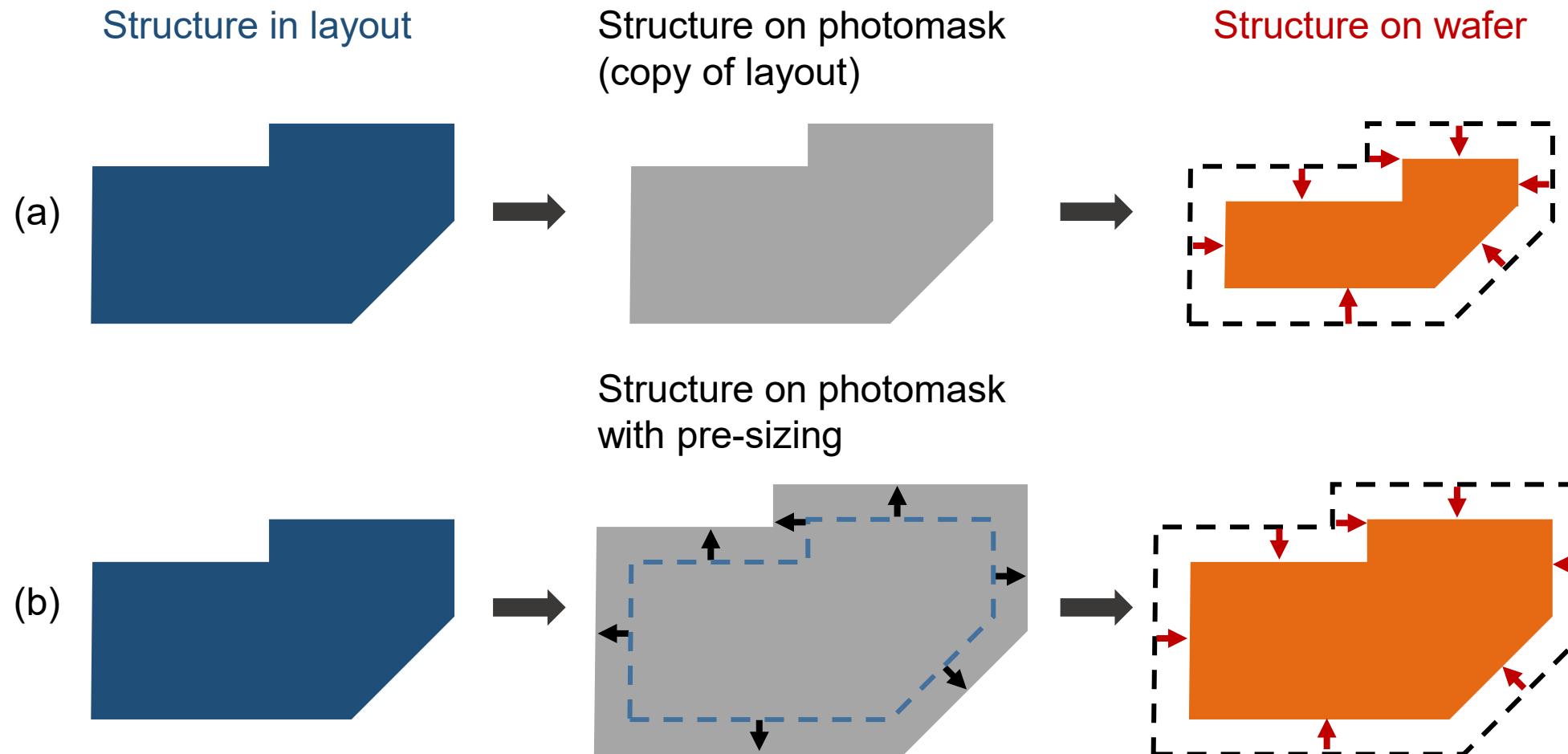
Layout structure



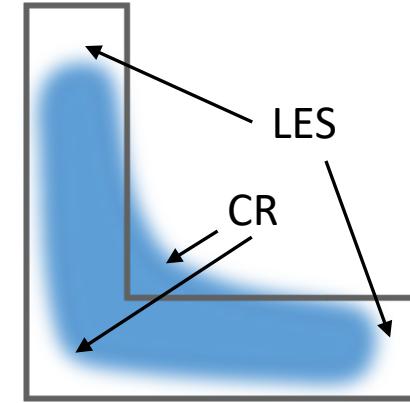
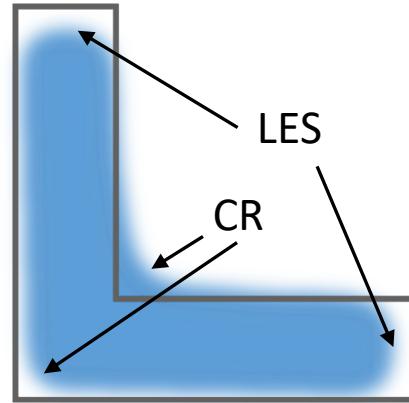
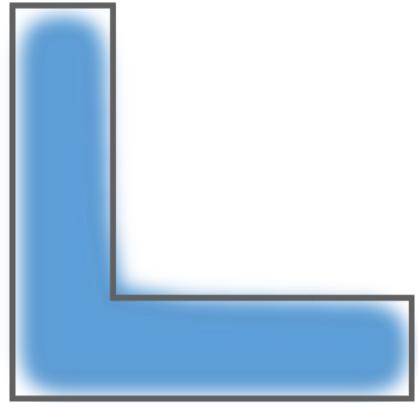
Structure on wafer

Overlay
error





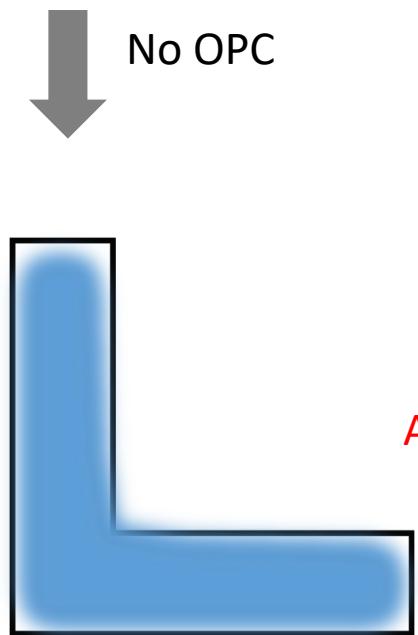
Decreasing ratio *structure size / wavelength*



Desired layout structure

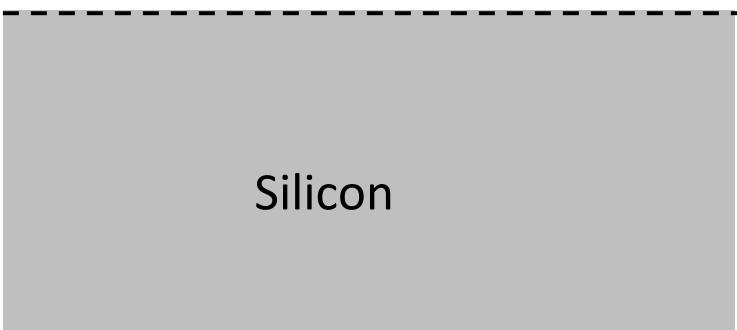
Structure in photoresist

Diffraction effects:
Line-end shortening (LES)
Corner rounding (CR)

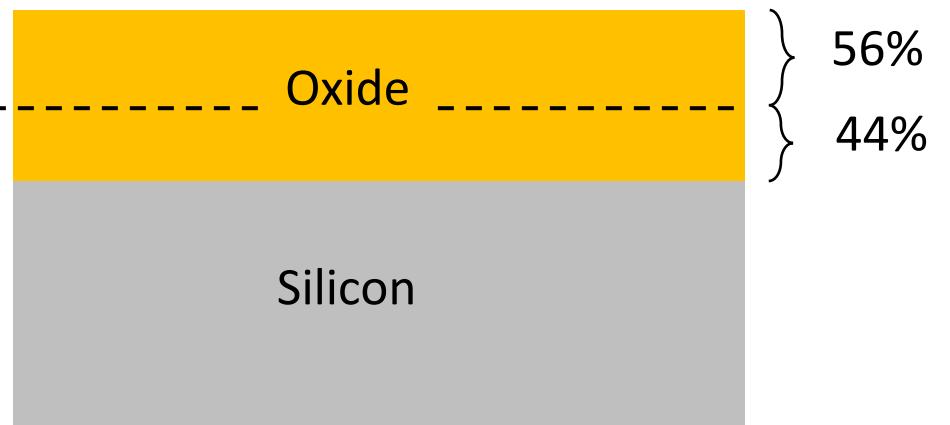


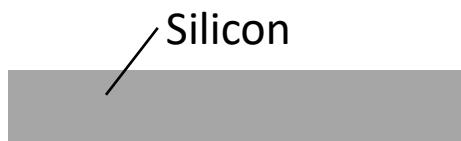
Optical proximity
correction (OPC)

Before thermal oxidation



After thermal oxidation





(a)



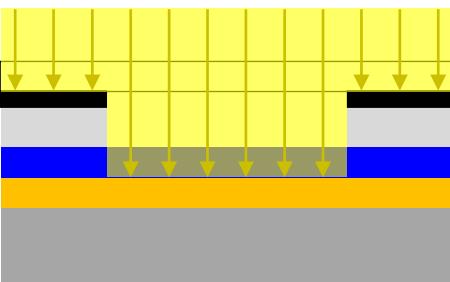
(b) Oxidation



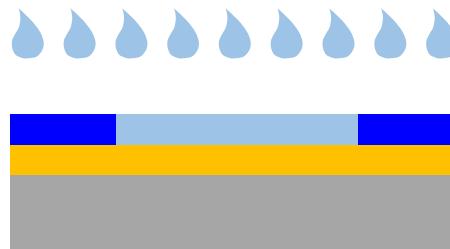
(c) Deposit photoresist



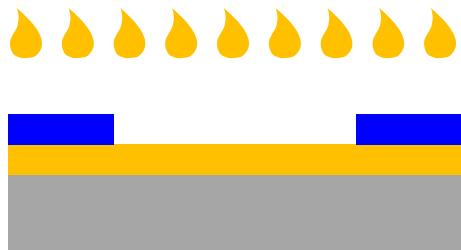
(d) Adjust photomask



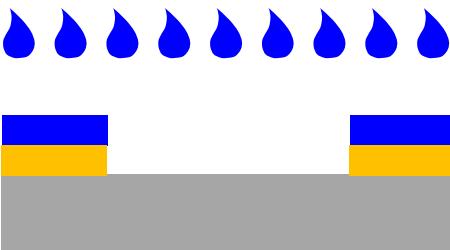
(e) Exposure



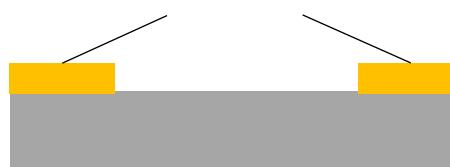
(f) Development



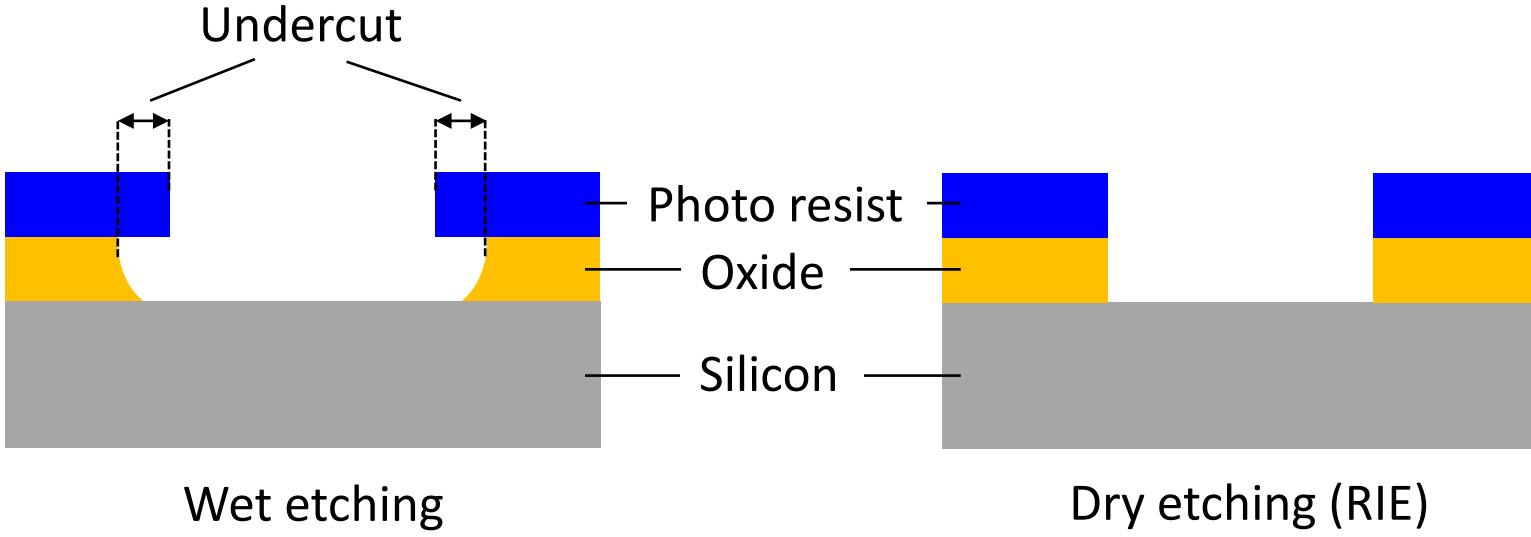
(g) Oxide etch

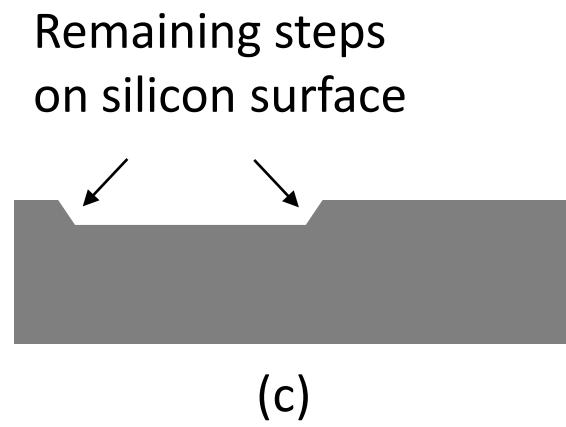
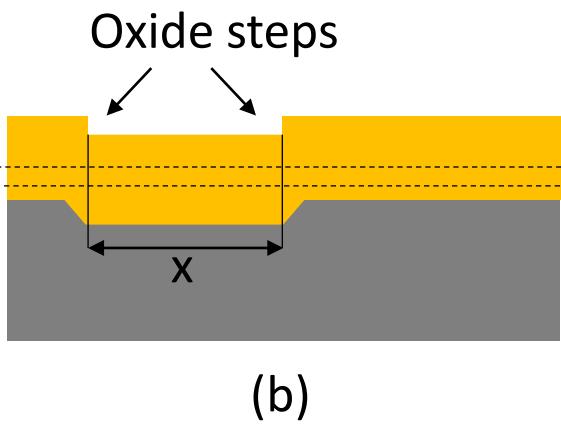
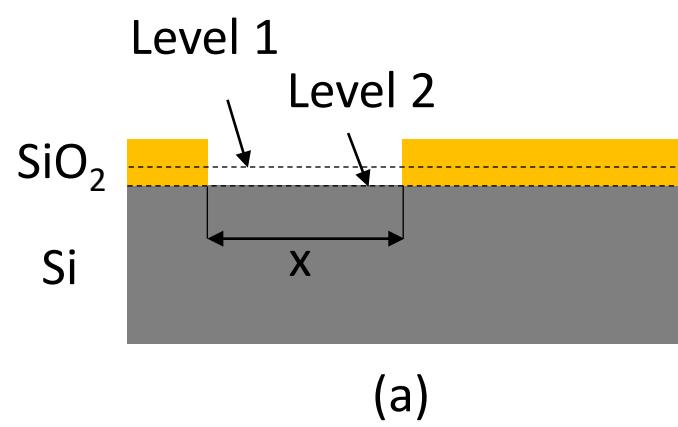


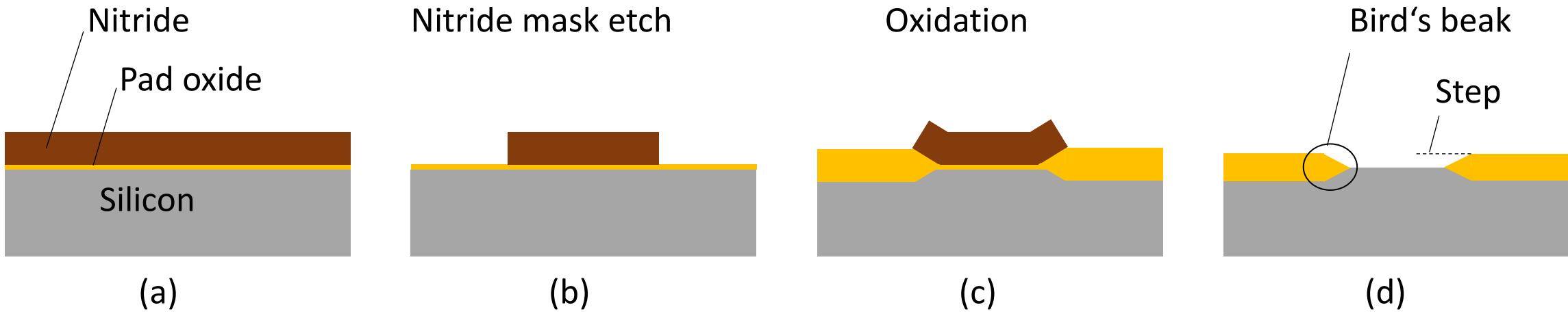
(h) Remove photoresist

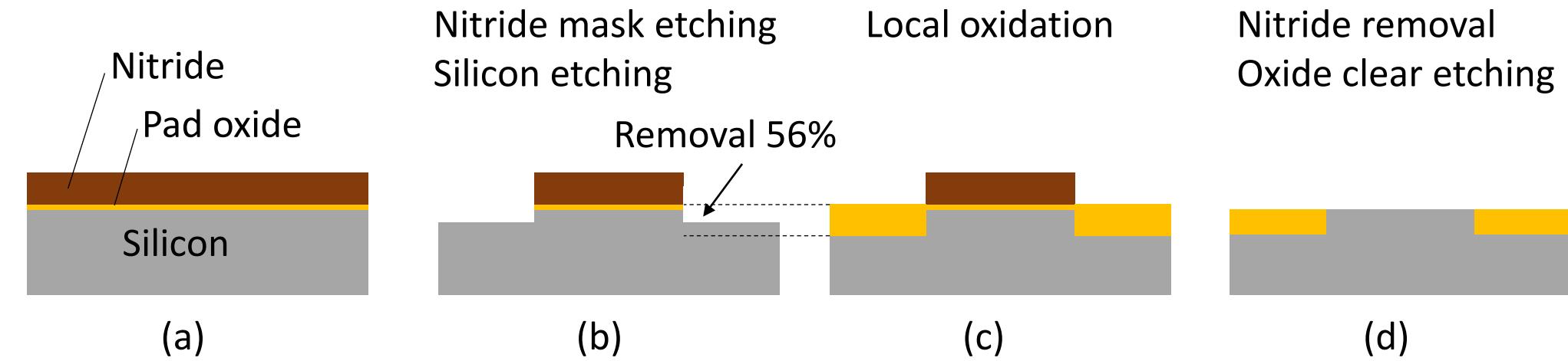


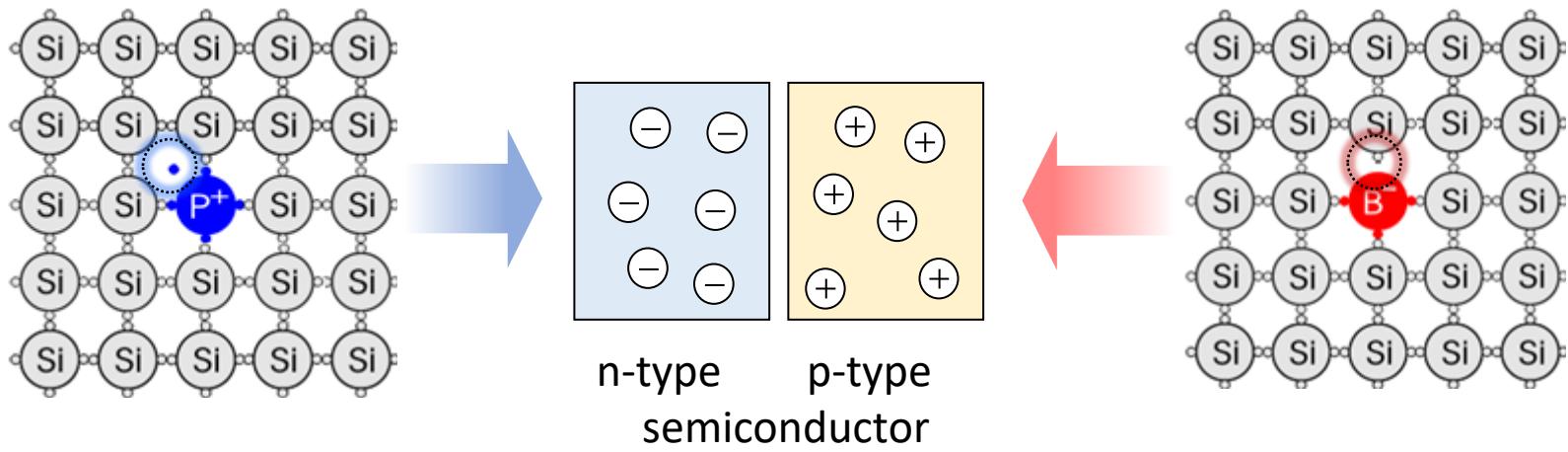
(i)

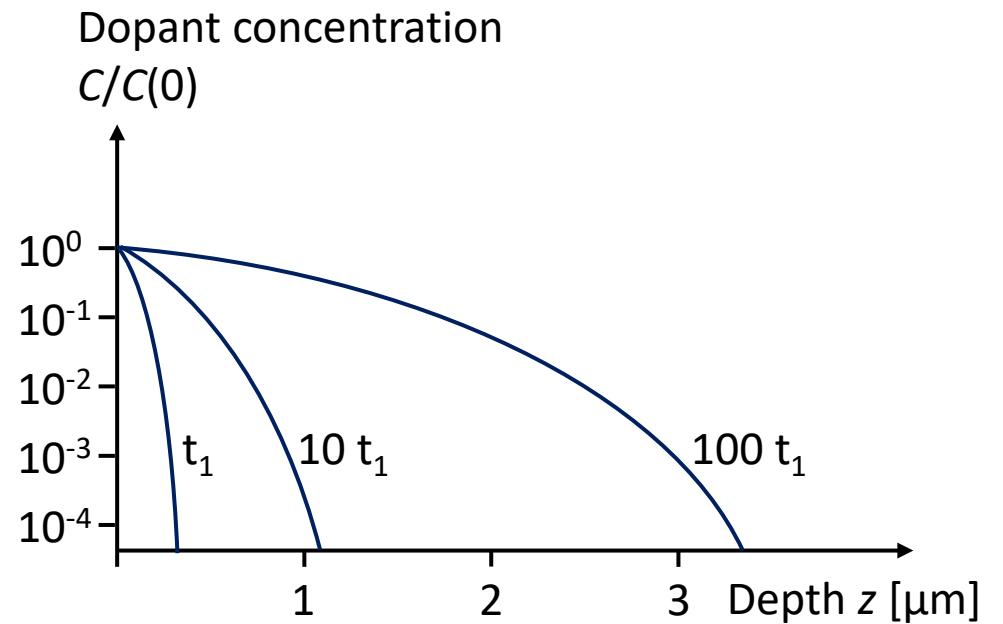
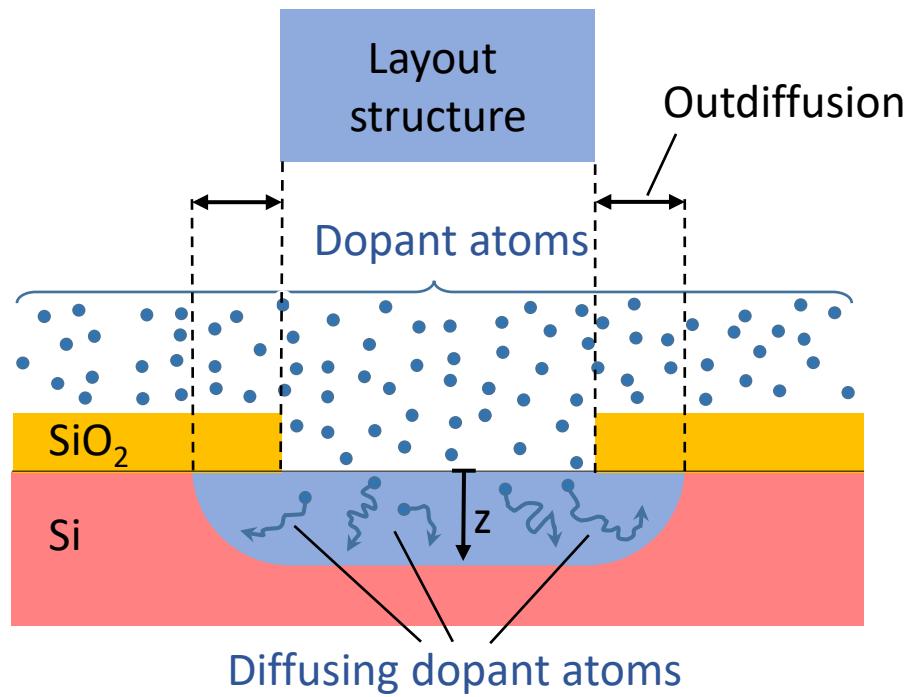


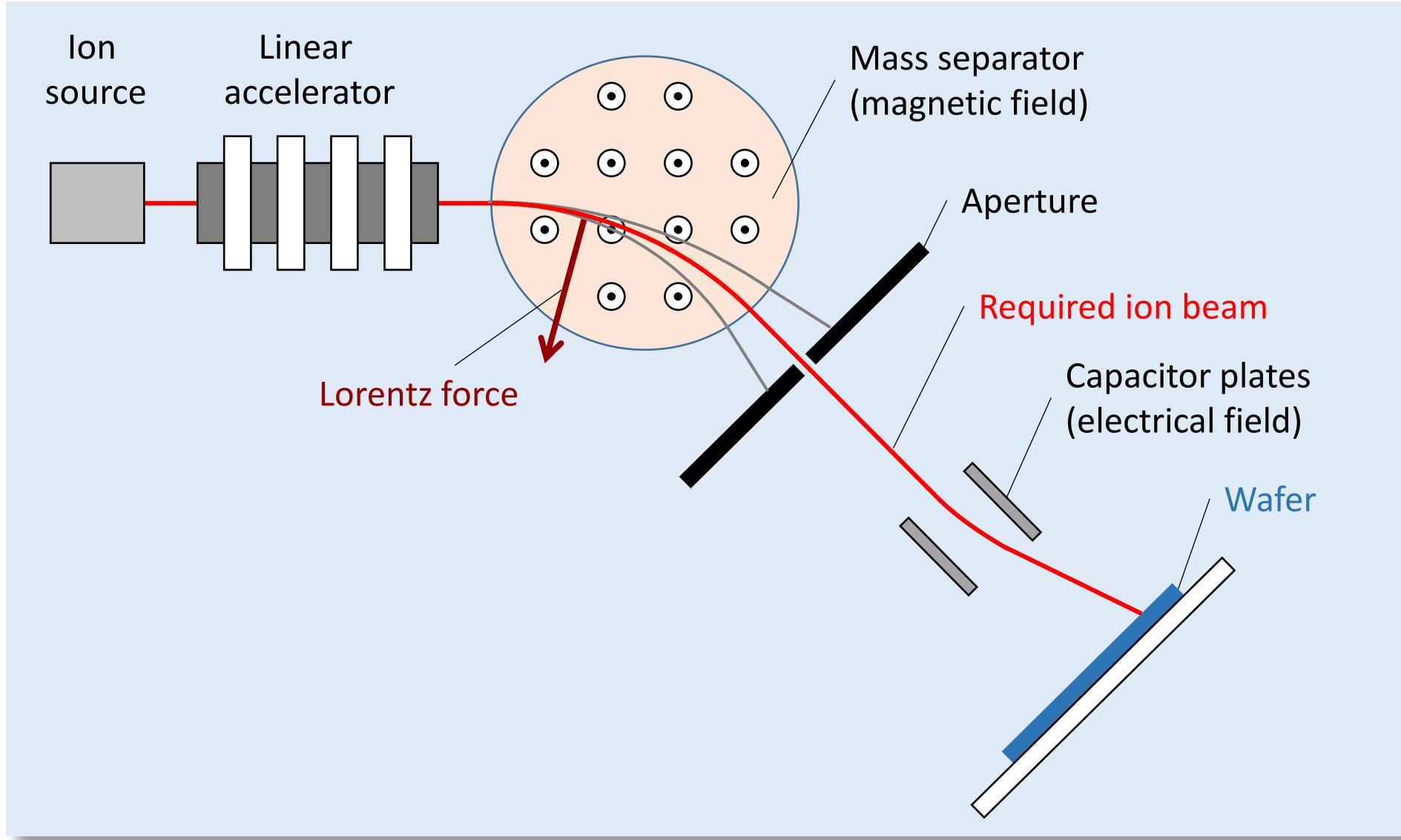


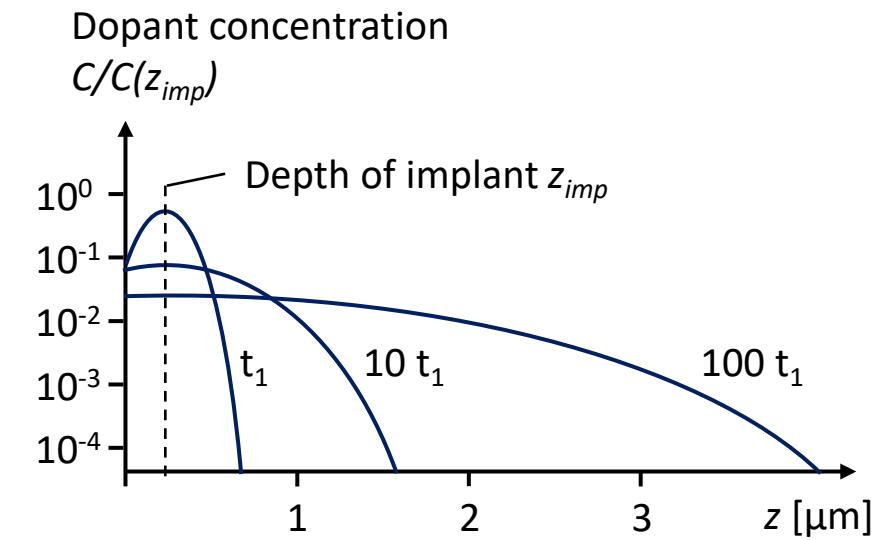
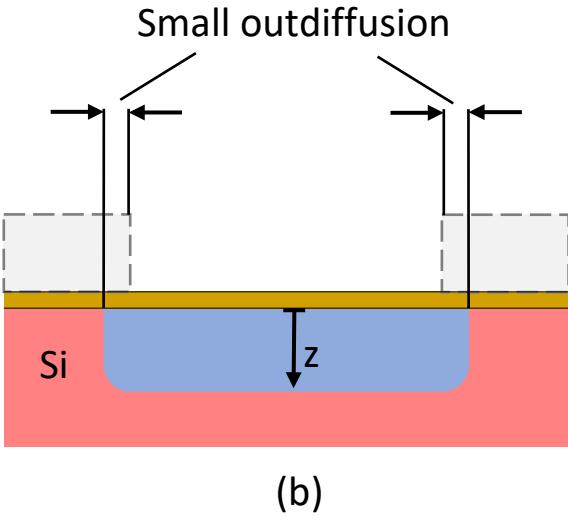
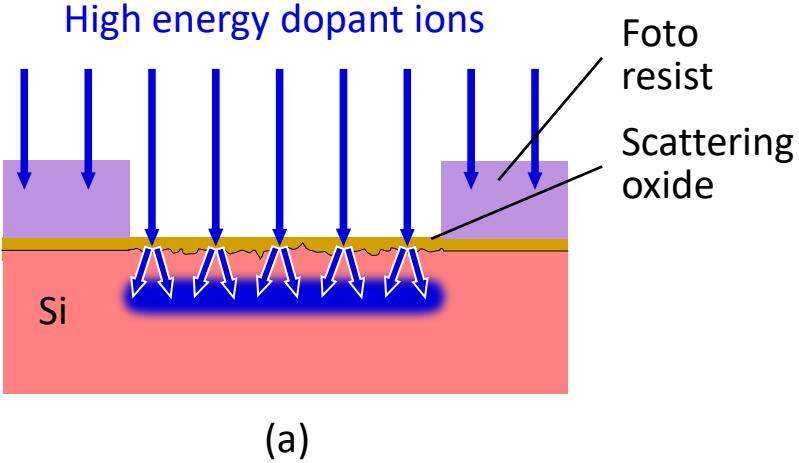


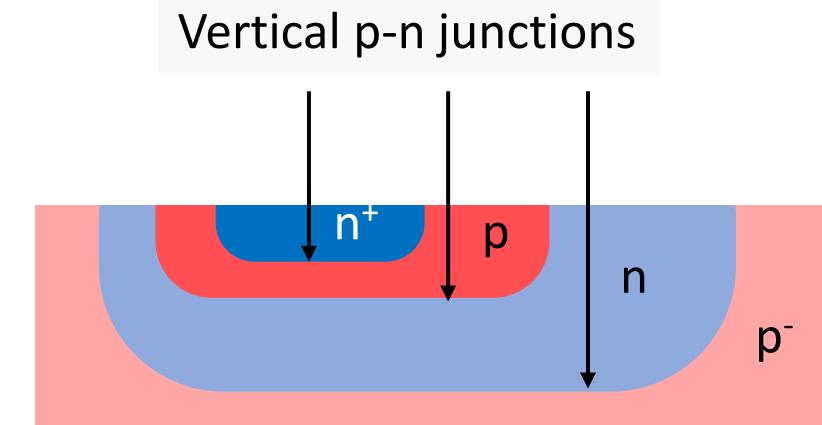




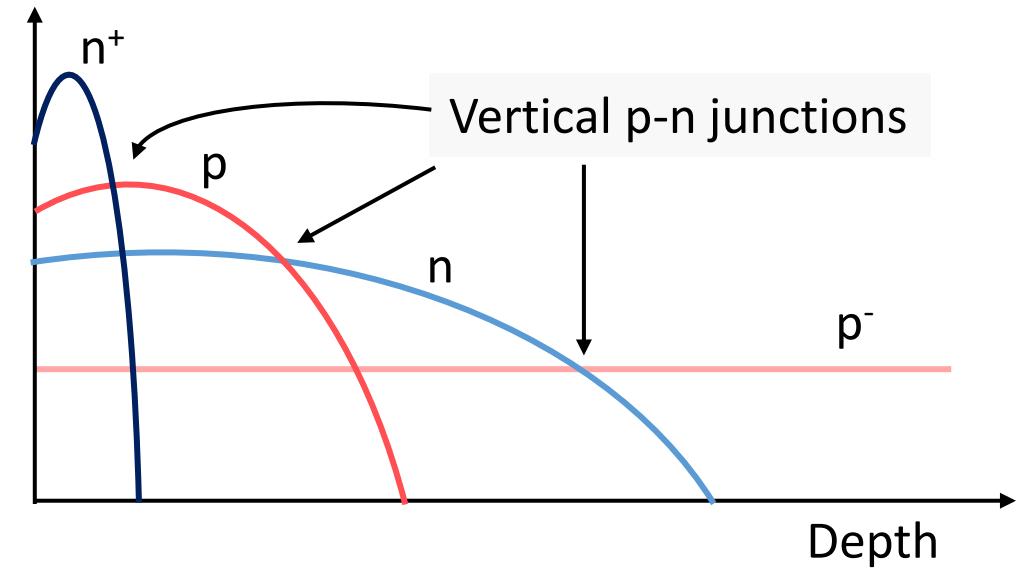


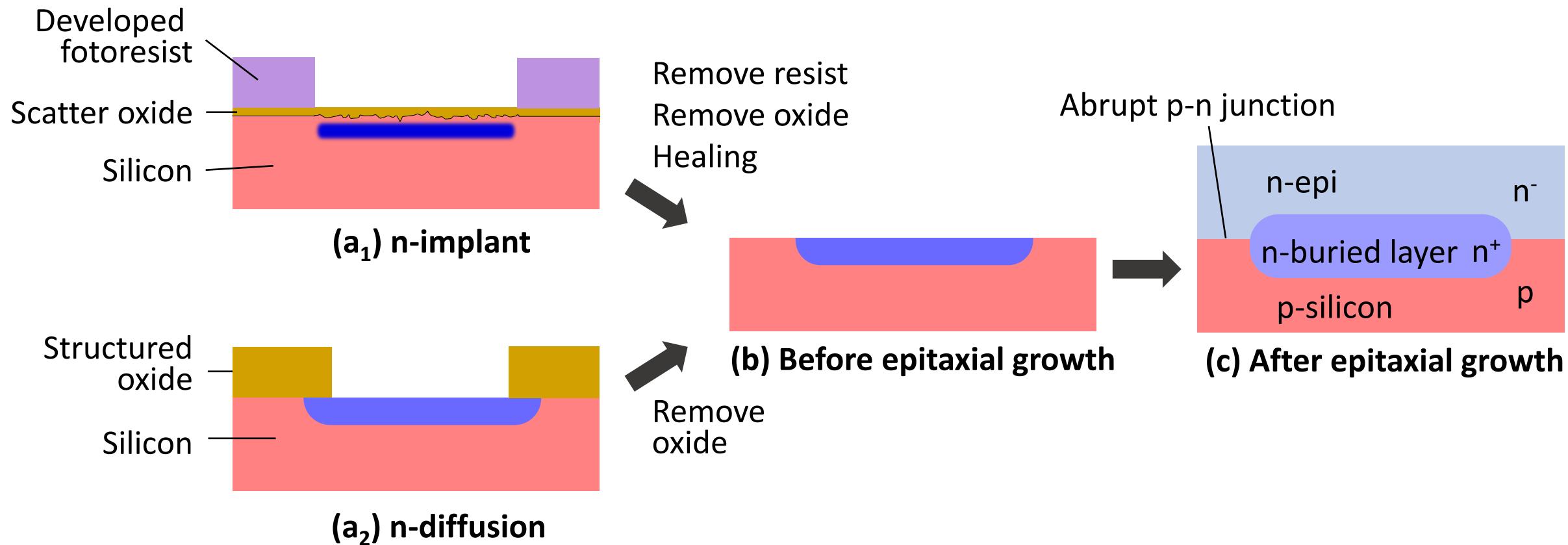


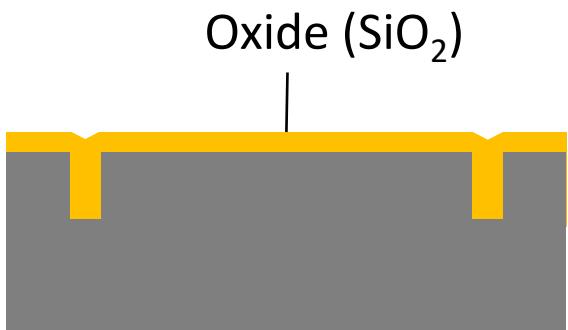
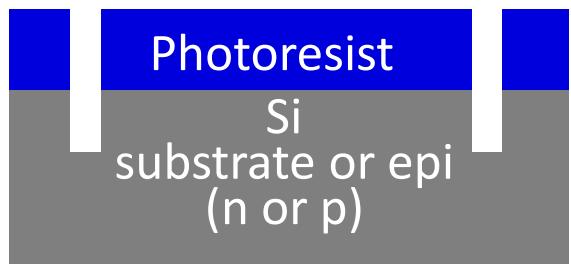




Dopant concentration (logarithmic)

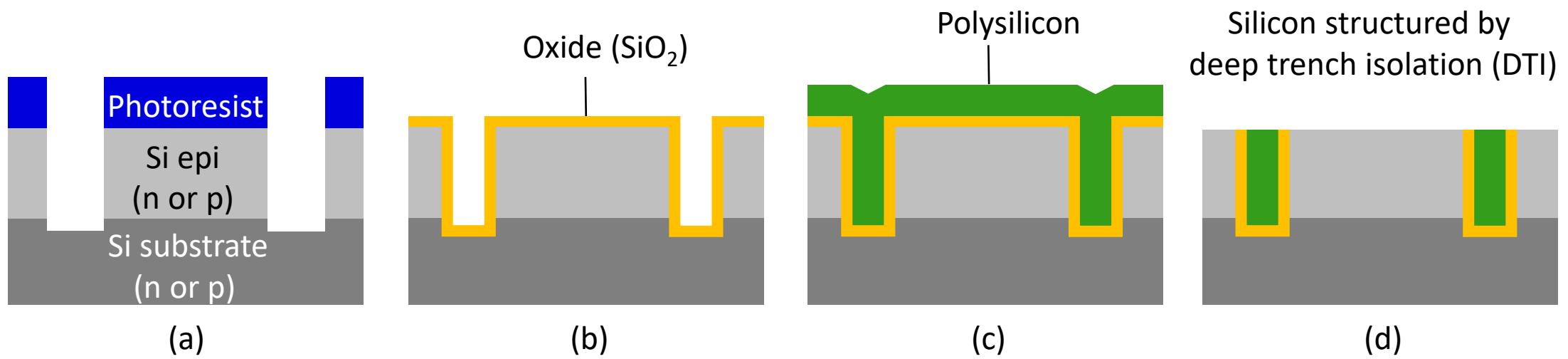


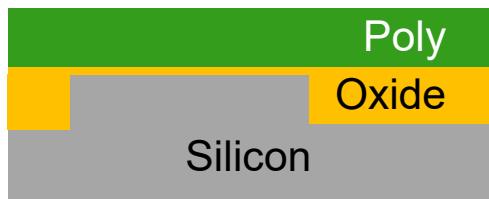




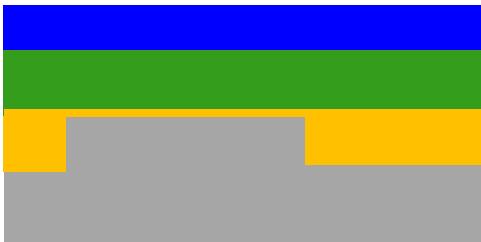
Silicon structured by
shallow trench isolation (STI)



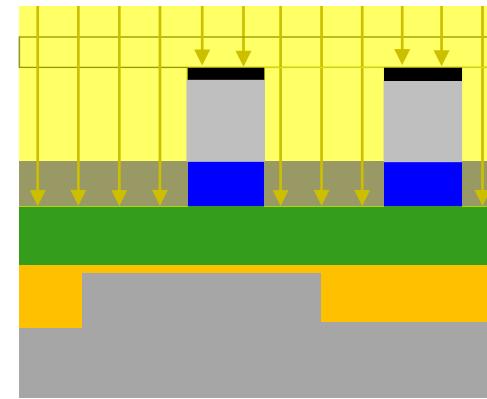




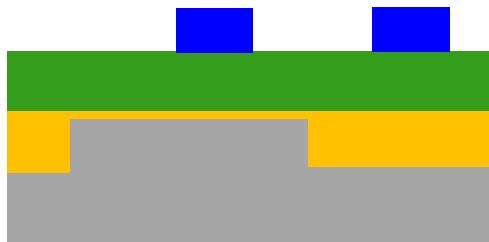
(a) Poly deposition



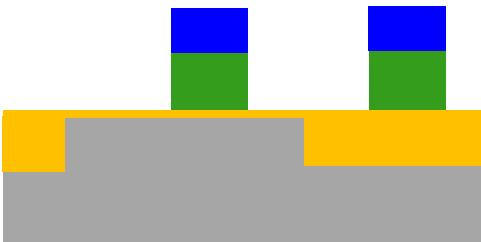
(b) Photoresist



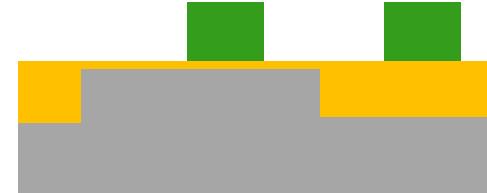
(c) Exposure



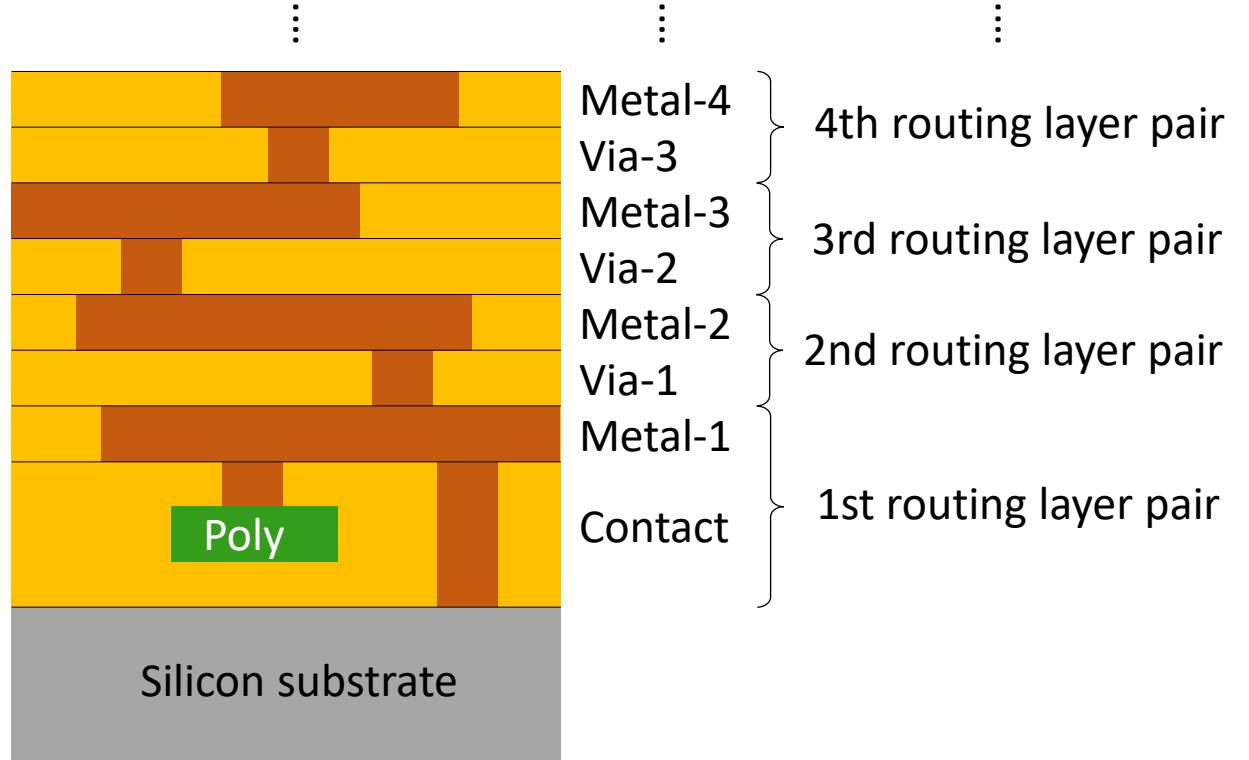
(d) Development

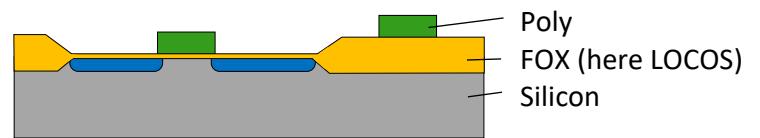


(e) Poly etch

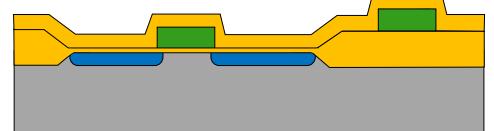


(f) Remove photoresist

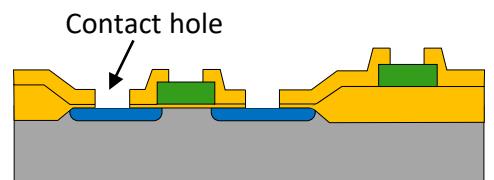




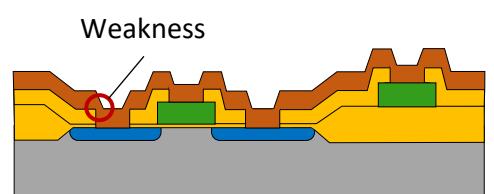
Initial state after FEOL



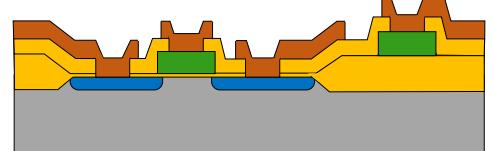
Step 1: 1st interlevel oxide deposit



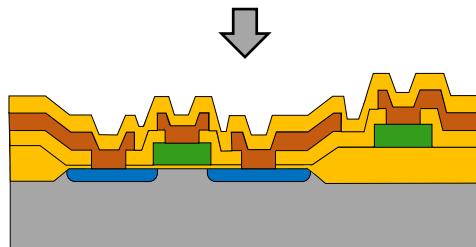
Step 2: contact hole etch



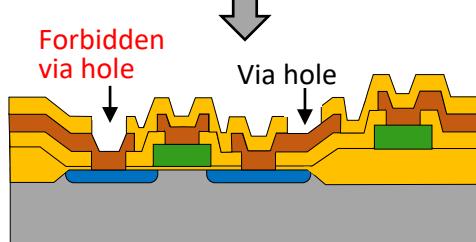
Step 3: metal 1 deposit



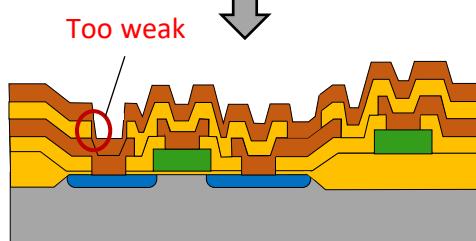
Step 4: metal 1 etch



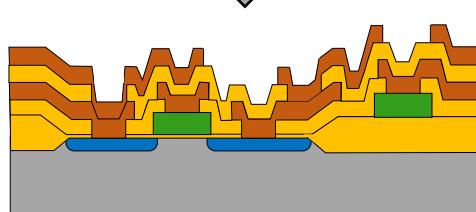
Step 5: 2nd interlevel oxide deposit



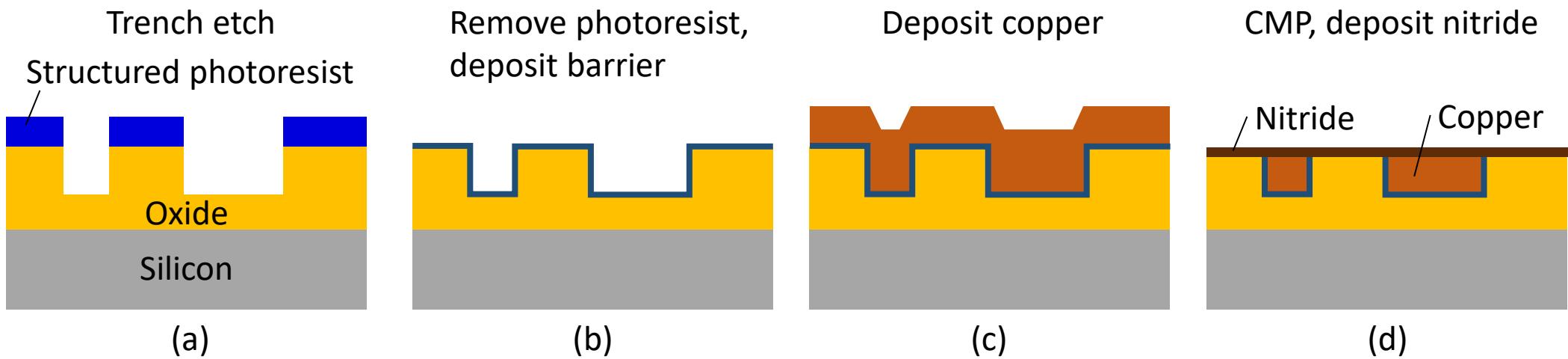
Step 6: via 1 hole etch

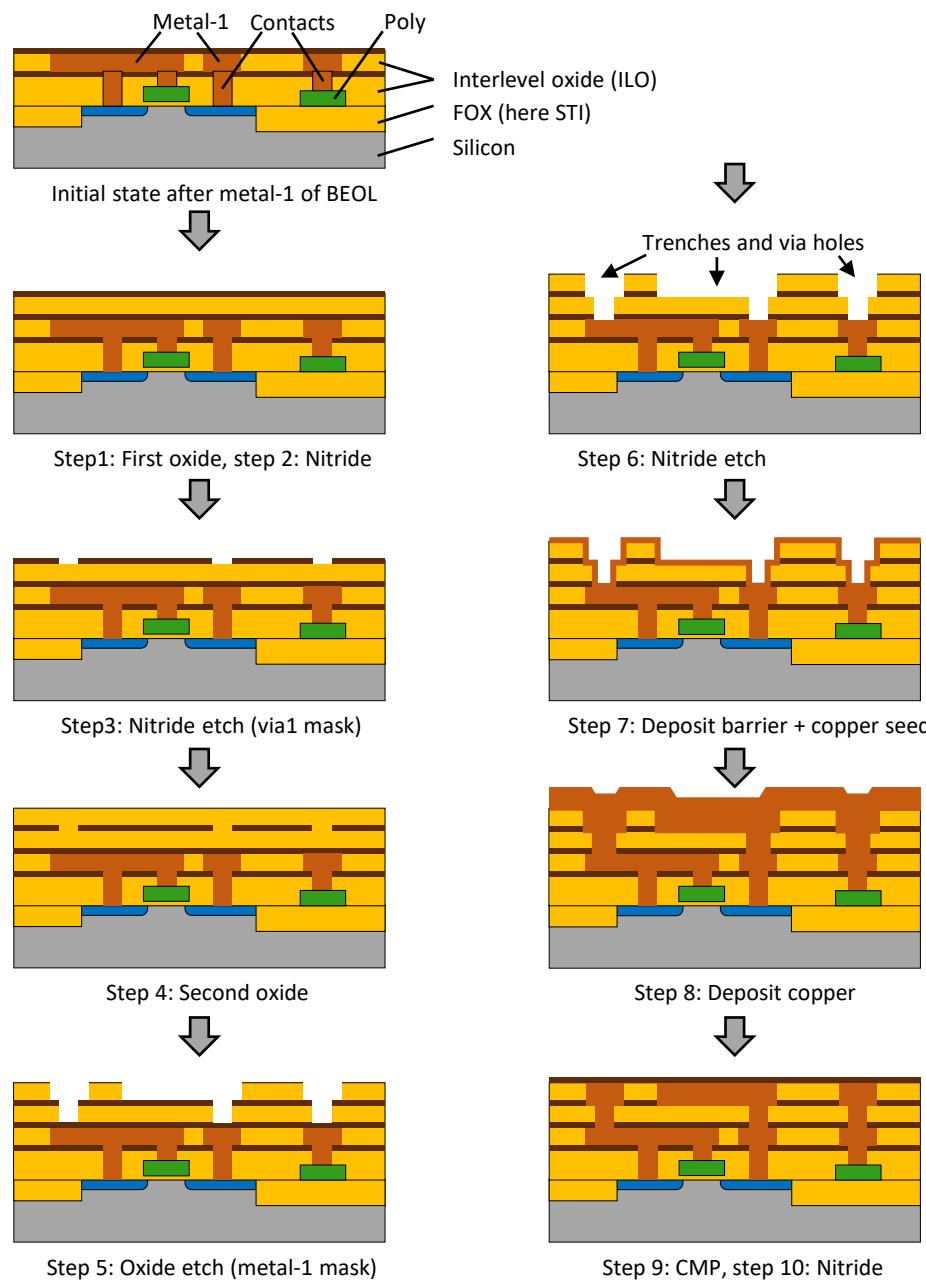


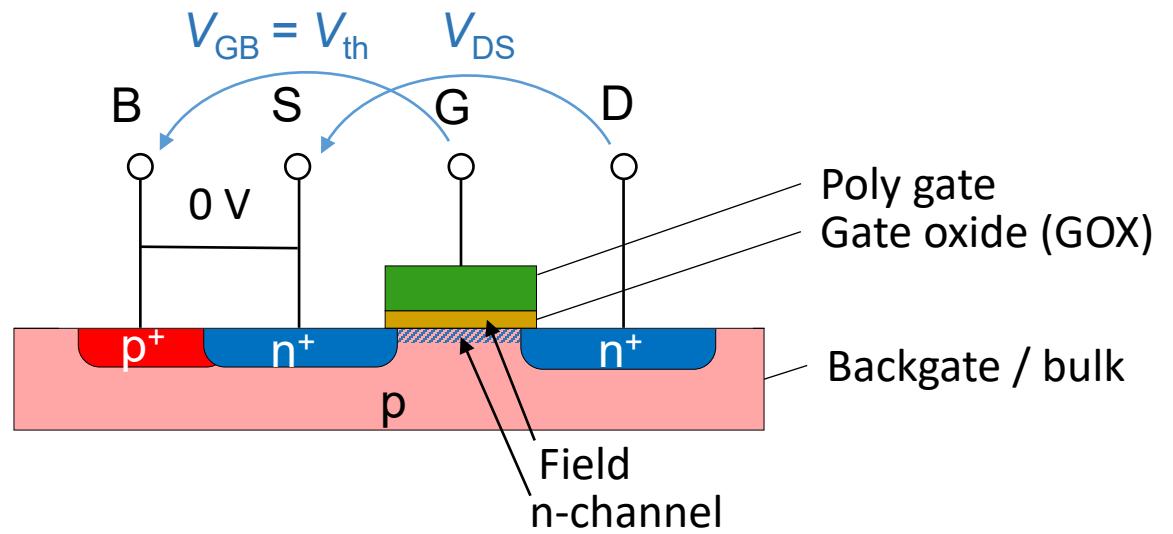
Step 7: metal 2 deposit

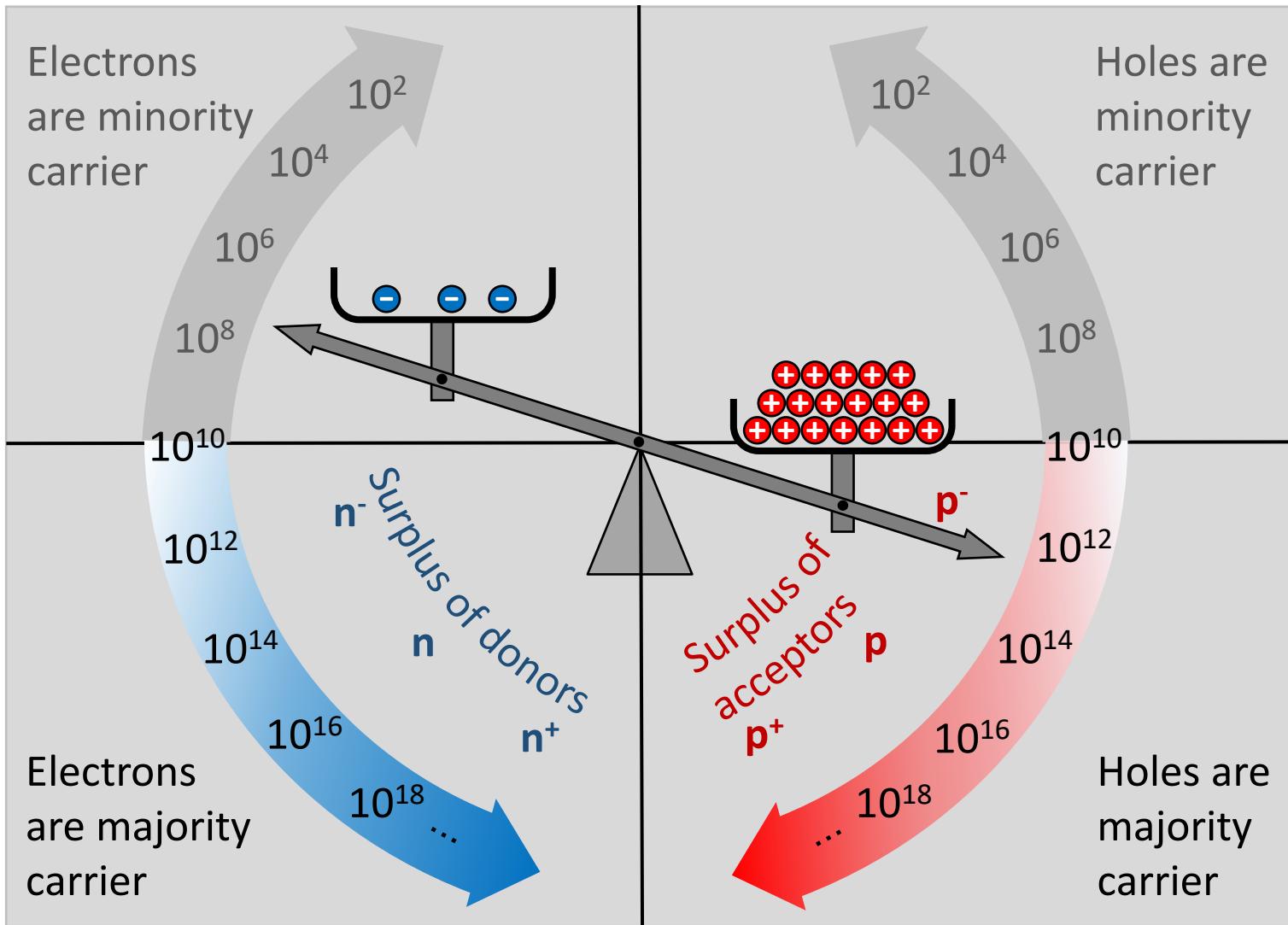


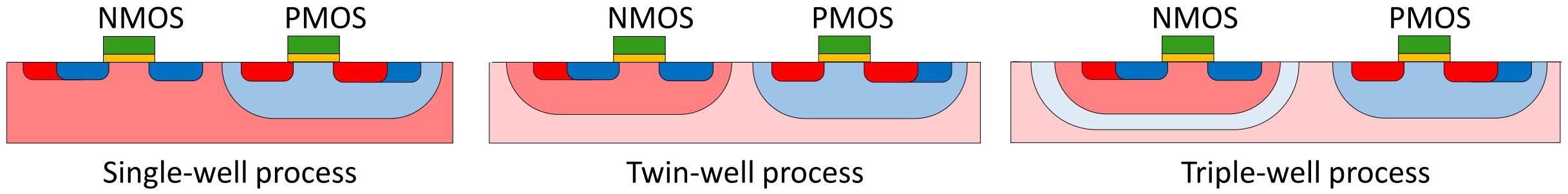
Step 8: metal 2 etch

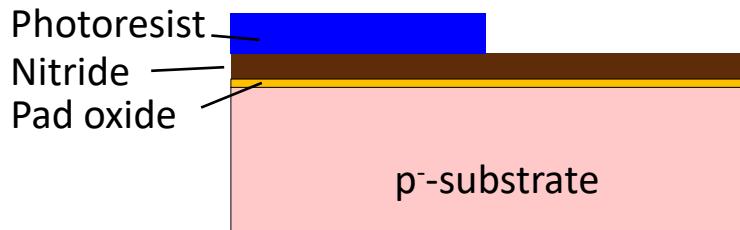




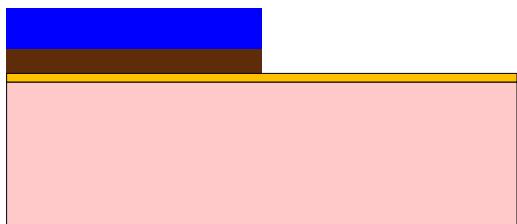




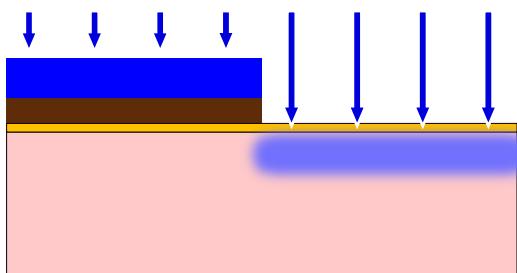




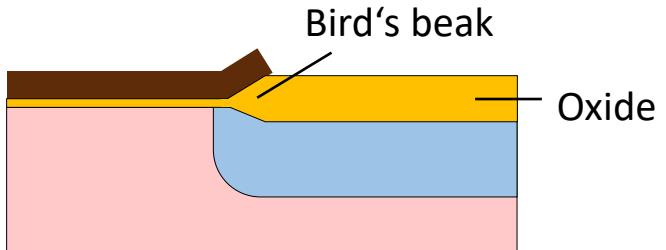
(a) Photolithography (mask Nwell)



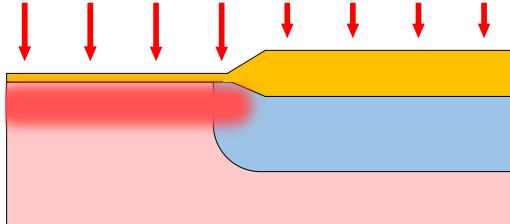
(b) Nitride etch



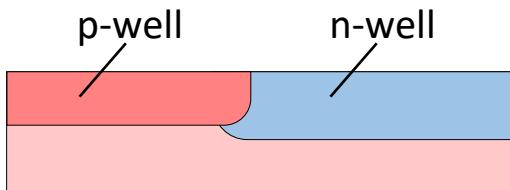
(c) n-implant



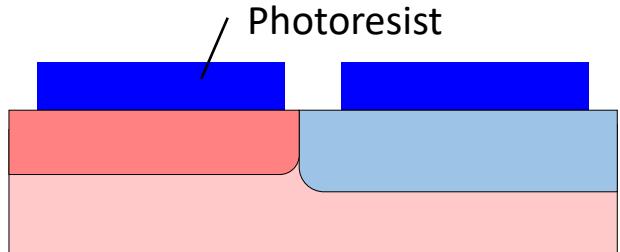
(d) Diffusion incl. LOCOS



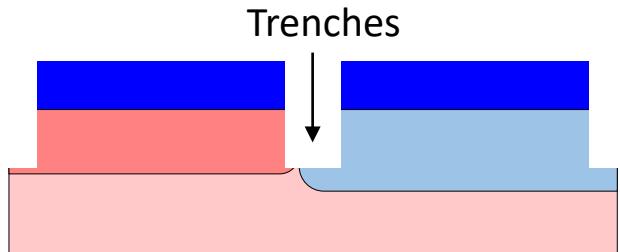
(e) p-implant (self-aligned)



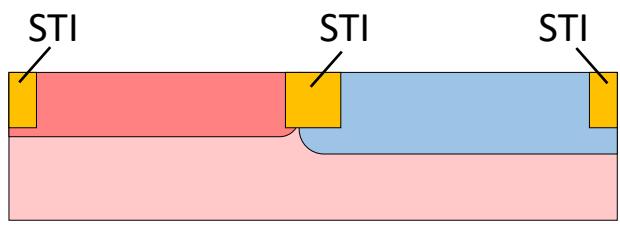
(f) Diffusion, CMP



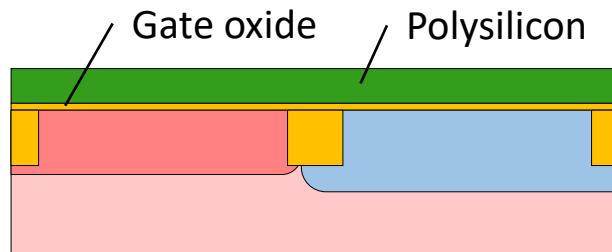
(a) Photolithography (mask STI)



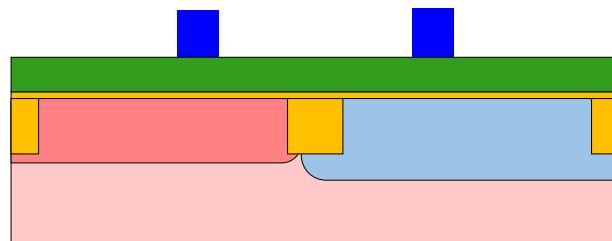
(b) Shallow trench etch



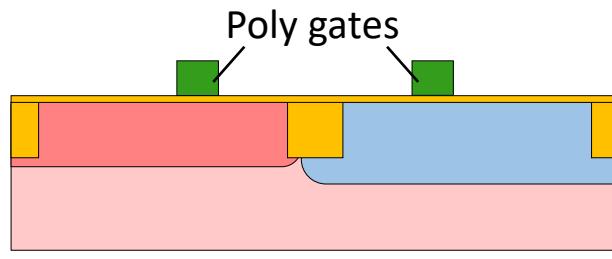
(c) Shallow trench oxidation, CMP



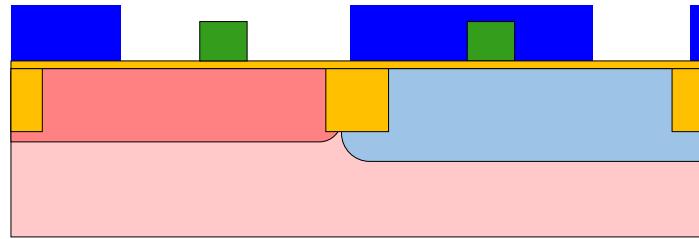
(d) Gate oxide, polysilicon deposit



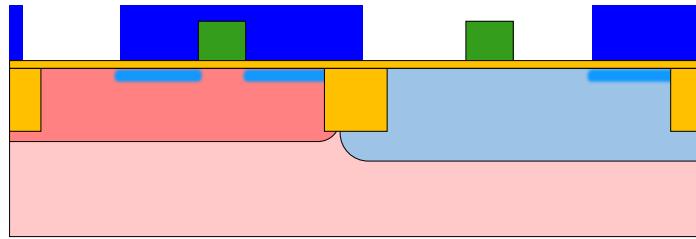
(e) Photolithography (mask Poly)



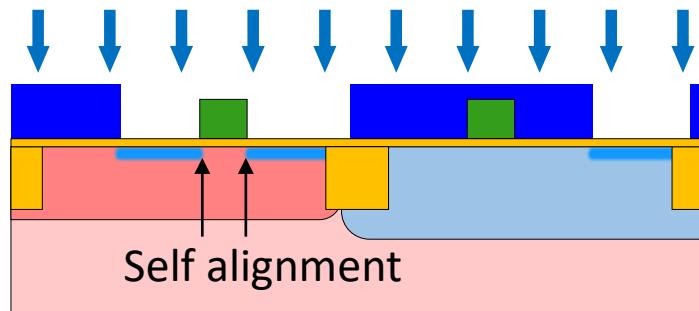
(f) Polysilicon etch



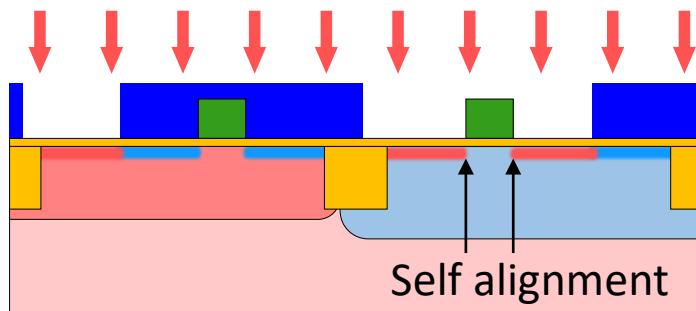
(a) Photolithography (mask NSD)



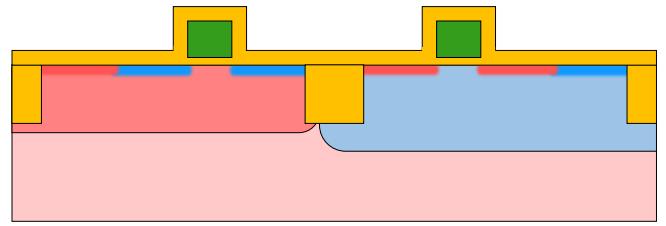
(c) Photolithography (mask PSD)



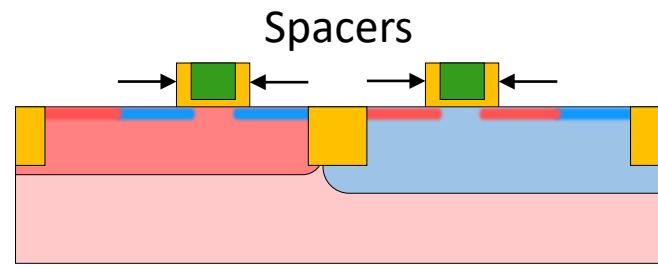
(b) n-implant (LDD)



(d) p-implant (LDD)



(a) Oxidation by CVD



(b) Oxide etch

