

5.5 Electromigration-Aware Design: Driven by Constraints

New challenges for IC design are appearing on the back of the ongoing trend in IC downscaling, i.e., structural miniaturization. Physical designs with ever-smaller feature sizes are subjected to an increasing number of more complex constraints due to these challenges. They are increasingly curtailing freedom in the design flow and are setting the boundaries of the ever-decreasing solution space. Hence, we are witnessing a slow, but steady evolution from a *constraint-correct* design flow to a *constraint-driven* one. With the latter, design algorithms and methodologies not only verify the correct implementation of constraints, but rather are governed by them.

One such challenge is EM. EM considerations are thus producing additional constraints in the design flow that are becoming the principal obstacles arising from progressive reductions in structure size. The resultant reduction in the available solution space for IC and routing design is illustrated in Fig. 5.3. Hence, a distinction must be made in the future between EM-robust and non-viable routing elements, whereby only EM-robust elements may be used for routing. Thus, constraint-driven routing is expected to predominate in future.

This book has examined the underlying EM-inhibiting effects and proposed guidelines for creating routing elements that are more EM robust. The prospective rules for the constraint-driven design in general and, in particular, constraint-driven routing techniques can be derived from the presented guidelines.

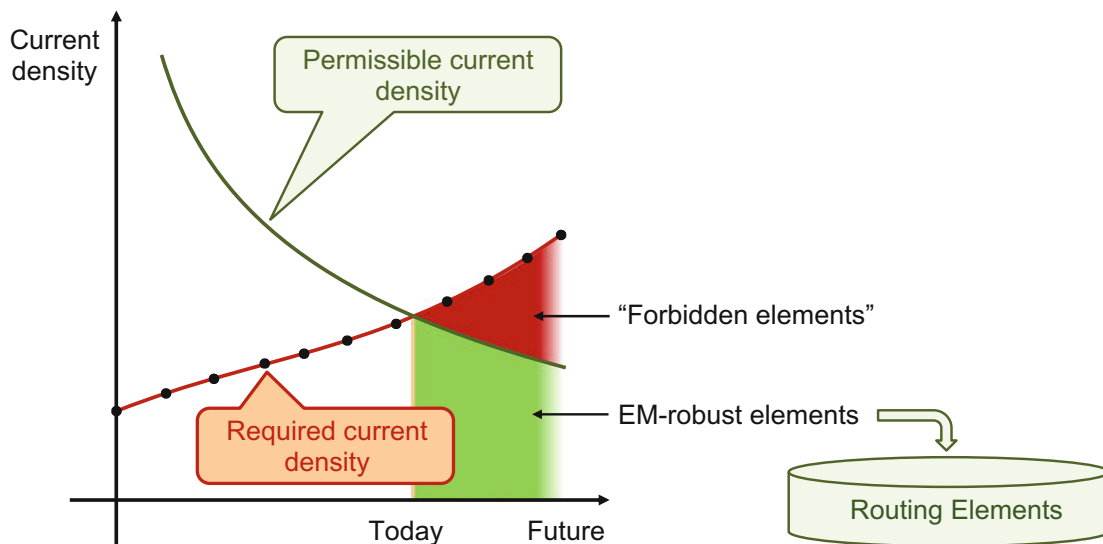


Fig. 5.3 Projected evolution of the routing solution space with falling current-density boundaries (green) and increasing required current densities (red, cf. Fig. 1.6 in Chap. 1). The solution space for the allowed routing elements will be increasingly curtailed; hence, today's constraint-correct routing evolves into constraint-driven routing where only EM-robust elements may be used (see Fig. 5.2 for the generation of the routing elements)

We expect that future, nanoscale design of reliable integrated circuits can only be achieved by applying the methodologies summarized in this final chapter and described in detail throughout this book.

References

- [ITR14] Int. Technology Roadmap for Semiconductors (ITRS), 2013 edn (2014). <http://www.itrs2.net/itrs-reports.html>. Last retrieved on 1 Jan 2018
- [ITR16] Int. Technology Roadmap for Semiconductors 2.0 (ITRS 2.0), 2015 edn (2016). <http://www.itrs2.net/itrs-reports.html>. Last retrieved on 1 Jan 2018