4.10 Summary

In this chapter, we examined different methodologies for mitigating EM in integrated electronic circuits. The use of the bamboo effect, length and reservoir effects, via configurations, self-healing, and the use of appropriate materials for conductors, dielectrics, and barriers are some of the issues we have examined.

The bamboo effect can greatly prolong the time to failure of an interconnect; it does, however, depend on numerous constraints. Before the effect can work in copper interconnects, the surface diffusion must be disabled, which requires specific materials. The focus in this regard is on very stable barrier layers that raise the activation energies to a high level. The interconnect resistance is increased as well in massively miniaturized technologies by means of wire slotting due to scattering effects. The benefits of the bamboo structure are thus largely eliminated by the negative thermal effects of self-heating.

The critical-length effects in combination with via effects (via-below and via-above configurations) and reservoir effects will soon become beneficial. Reliability can be greatly improved by controlling the wiring by using short segments where possible, and considering different boundary values for the product of current density and length. Reservoirs should be deployed in appropriate applications, as well.

Special care should be taken when arranging redundant vias or via arrays to avoid generating new EM flash points in the layout. Via arrays are required in the very EM-sensitive power supply nets. Hence, they are critical for the digital design flow. Specifically, one should optimize the via configurations also with regard to reservoirs between the vias to maximize the time to failure for small footprints. Reservoirs are particularly beneficial in power supply nets due to the constant direction of the current flow.

Frequency effects, that is, self-healing and skin effects, serve only to classify nets and allocate current-density boundary values. This is critical for the routing step and also for verification, as different current-density boundary values should be assigned for each net class. Valuable routing resources would be squandered by oversizing if a global boundary value was applied to the entire layout. The skin effect will not play a significant role in digital circuits now and in the near future, because frequencies will only increase very slowly compared to the scaling of the structural miniaturization. In the future, on the other hand, the skin effect will impact the reliability of analog high-frequency integrated circuits at frequencies of 45 GHz or higher [YZZ+11].

In this chapter, we also cast an eye beyond current methodologies and into the future. The main focus of present research is on the search for a new interconnect material, possibly CNTs. The current state of research shows that CNTs are potential candidates as a via and wire material. Further practice-oriented research is required, however, to integrate them in the manufacturing process for integrated circuits.

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