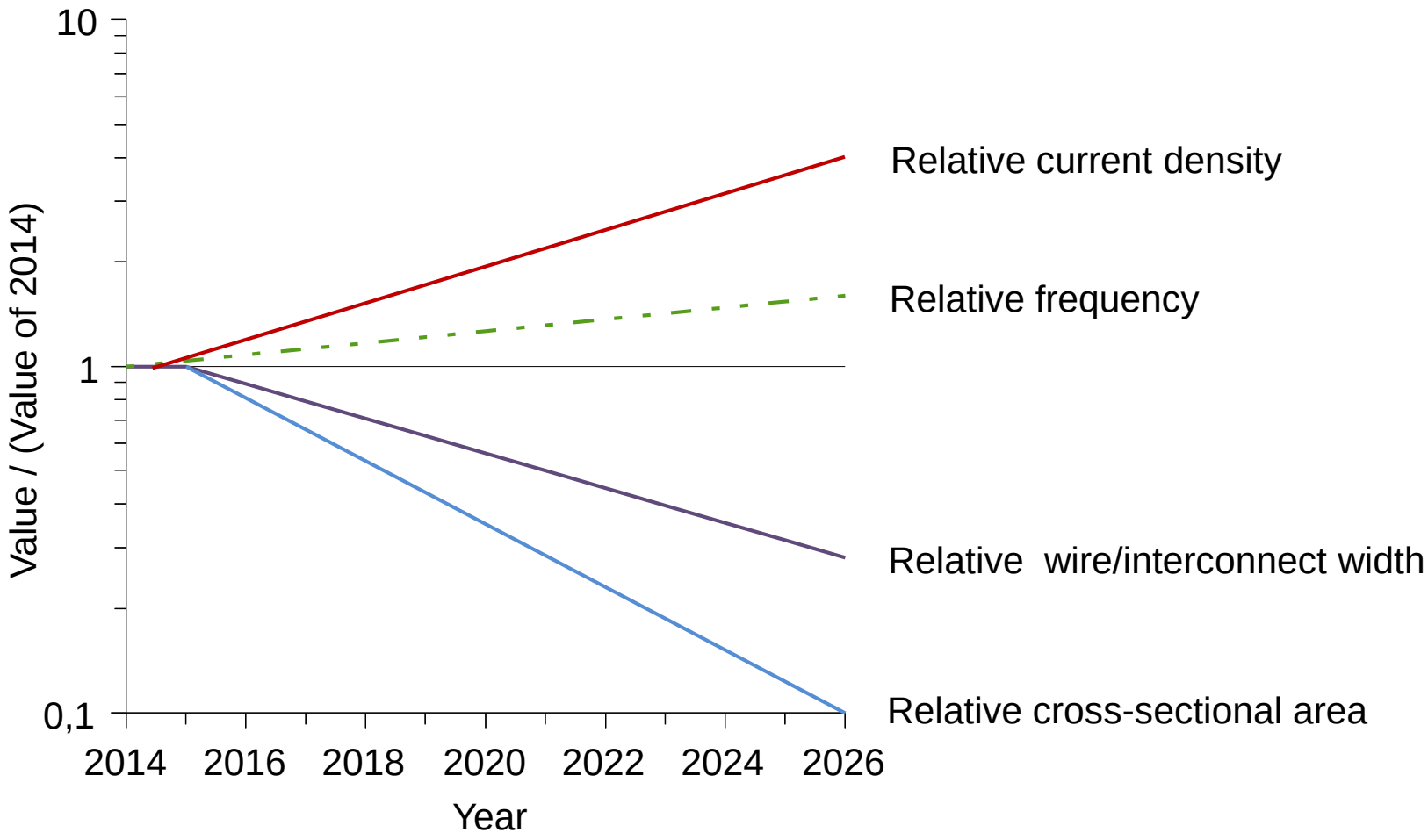
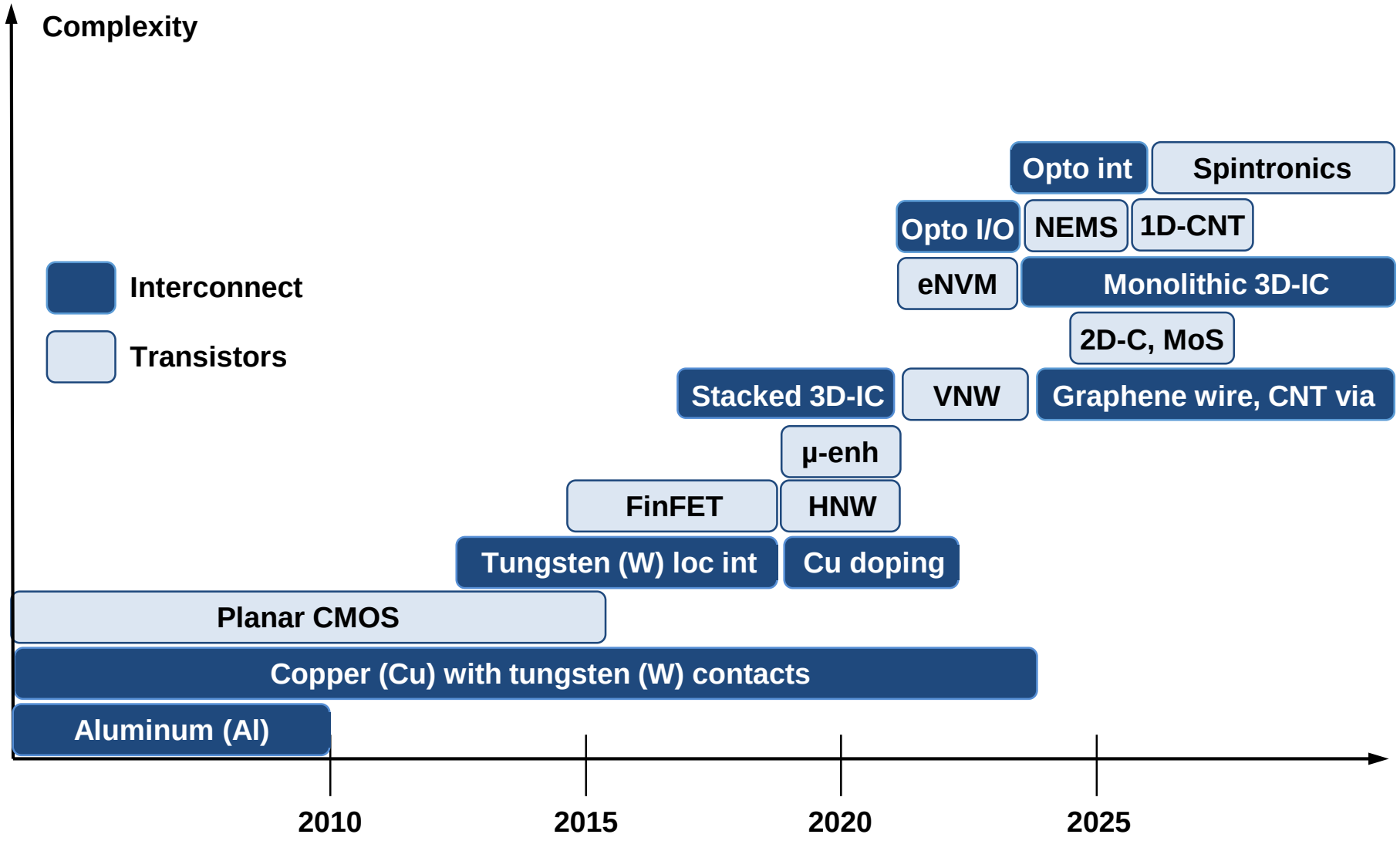
Year	2016	2018	2020	2022	2024	2026	2028
Gate length (nm)	15.34	12.78	10.65	8.87	7.39	6.16	5.13
On-chip clock frequency (GHz)	6.19	6.69	7.24	7.83	8.47	9.16	9.91
DC equivalent maximum current (µA, four gates)*	29.09	23.19	16.52	12.40	9.99	7.89	5.91
Metal 1 properties (Interconnect)							
Width – half-pitch (nm) (nm)	28.3	22.5	17.9	14.2	11.3	8.9	7.1
Aspect ratio	2.0	2.0	2.0	2.1	2.1	2.2	2.2
Height (nm)*	56.7	45.0	35.7	29.8	23.6	19.6	15.6
Cross-sectional area (nm^2)*	1607.2	1012.5	637.8	421.9	265.8	175.4	110.5
DC equivalent current densities (MA/cm^2)							
Maximum tolerable current density (w/o EM degradation)**	3.0	1.8	1.1	0.7	0.4	0.3	0.2
Maximum current density (beyond solutions are unknown)**	15.4	9.3	5.6	3.4	2.1	1.2	0.7
Required current density for driving four inverter gates	1.81	2.29	2.59	2.94	3.76	4.50	5.35
		EM to be expected			**Solutions unknown**		

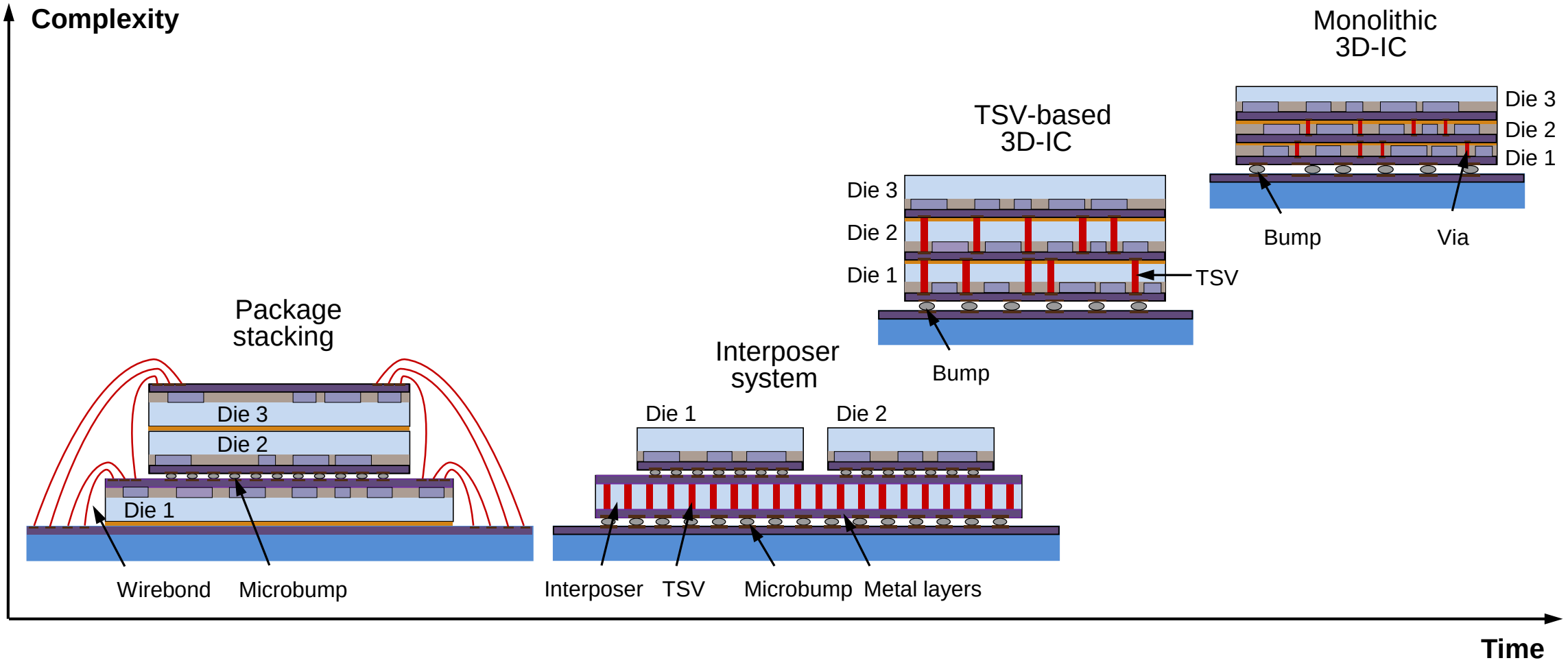
*) Calculated values, based on given width W, aspect ratio A/R, and current density J, calculated as follows: layer thickness $T = A/R \times W$, cross- sectional area $A = W \times T$ and current $I = J \times A$.

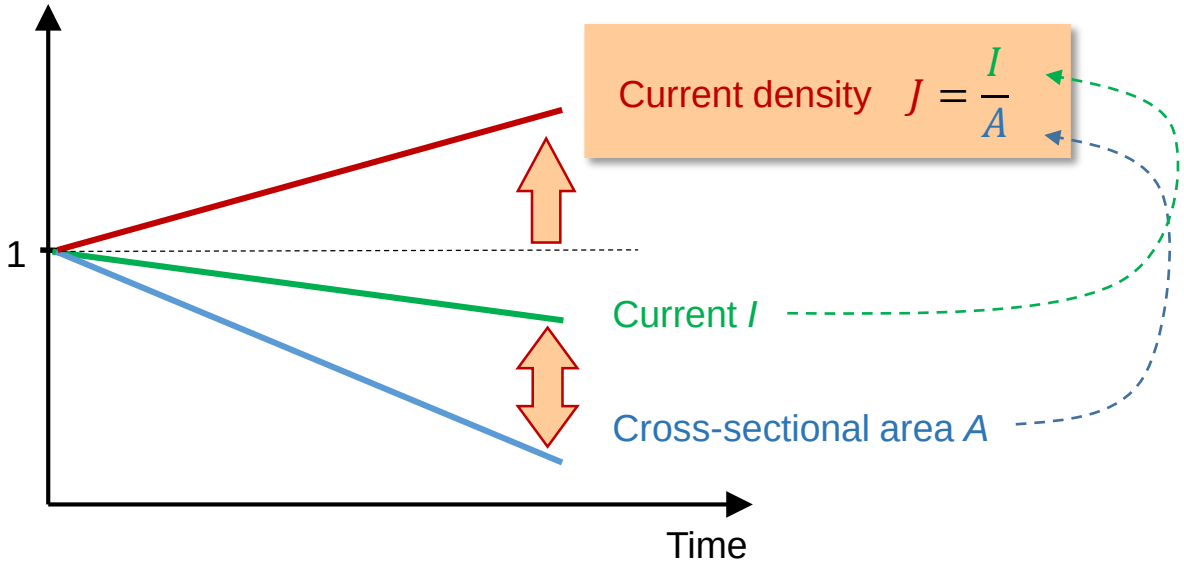
) Values taken from Fig. INTC9 [ITR14**]

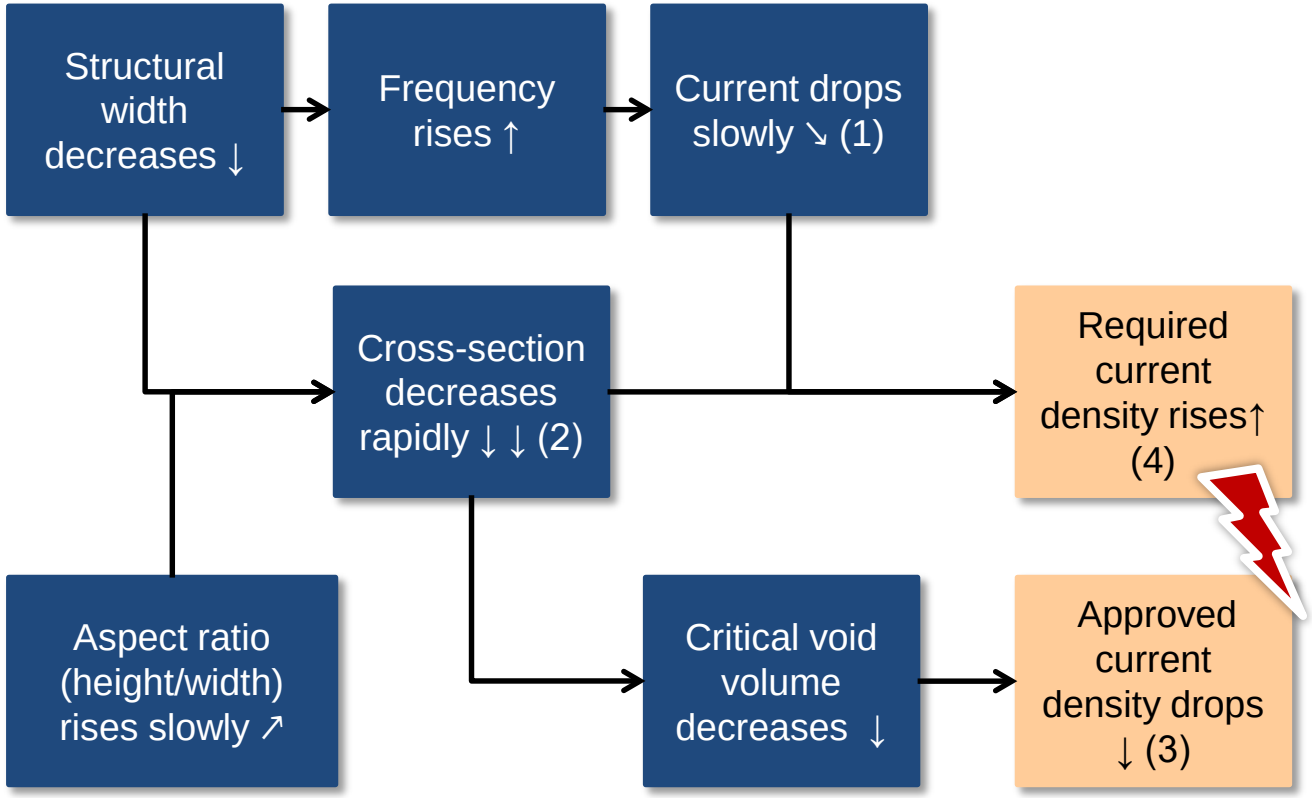
Remaining values from ITRS [**ITR14**]

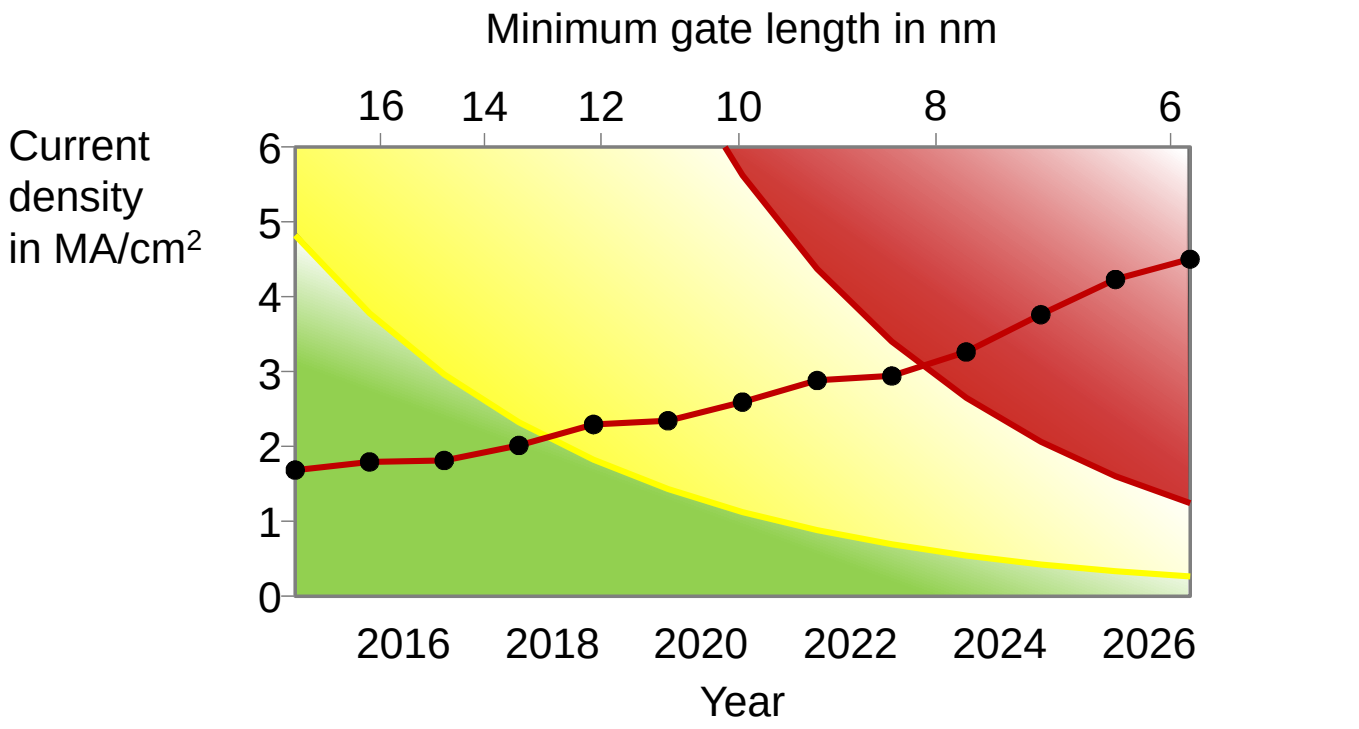

10
1
0,1
Value / (Value of 2014)
2014
2016
2018
2020
2022
2024
2026
Year
Relative current density
Relative frequency
Relative wire/interconnect width
Relative cross-sectional area


Complexity
Interconnect
Transistors
Opto int
Spintronics
Opto I/O
NEMS
1D-CNT
eNVM
Monolithic 3D-IC
2D-C, MoS
Stacked 3D-IC
VNW
Graphene wire, CNT via
μ-enh
FinFET
HNW
Tungsten (W) loc int
Cu doping
Planar CMOS
Copper (Cu) with tungsten (W) contacts
Aluminum (Al)
2010
2015
2020
2025


Complexity
Monolithic
3D-IC
Die 3
Die 2
Die 1
Bump
Via
TSV-based
3D-IC
Die 3
Die 2
Die 1
TSV
Bump
Package
stacking
Die 3
Die 2
Die 1
Wirebond
Microbump
Interposer
system
Die 1
Die 2
Interposer
TSV
Microbump
Metal layers
Time


Current density $J = \frac{I}{A}$
1
Current I
Cross-sectional area A
Time


Structural width decreases ↓
Frequency rises ↑
Current drops slowly ↘ (1)
Cross-section decreases rapidly ↓ ↓ (2)
Required current density rises↑ (4)
Aspect ratio (height/width) rises slowly ↗
Critical void volume decreases ↓
Approved current density drops ↓ (3)


Minimum gate length in nm
16
14
12
10
8
6
Current density in MA/cm²
6
5
4
3
2
1
0
2016
2018
2020
2022
2024
2026
Year
IC design without EM consideration
Manufacturable EM-robust solutions are known
Manufacturable EM-robust solutions are NOT known
Required current density for driving four inverter gates