1.5 Motivation and Structure of This Book

Integrated circuits have far greater reliability than circuits consisting of discrete components; this advantage is driving semiconductor scale reductions and associated investments in advanced technologies.

Unfortunately, increasingly small IC structures begin to have a significant negative impact on reliability, as the cross-sectional areas of the metallic interconnects in the IC are diminished in size. The problem arises because the required currents cannot be reduced to the same extent—even by reducing the supply voltages and gate capacitances.

To make matters worse, the maximum tolerable current densities are shrinking at the same time due to smaller structure sizes (see Fig. 1.5). As already mentioned, the reason for this is that small voids and other material defects, which could have been tolerated in earlier technology nodes, cause increasingly dramatic damage or side effects to the wires with shrinking metal structures. Thus, maximum tolerable current densities will have to decrease to maintain the required interconnect reliability. As a result, technological roadmaps, such as the ITRS, have indicated that all minimum-sized interconnects will be increasingly EM-affected, potentially limiting any further downscaling of wire sizes.

Furthermore, the total length of interconnect per IC will continue to increase. As a consequence, reliability requirements per length unit of the wires need to *increase* in order to *maintain* overall IC reliability. This accepted wisdom is contradicted by the future *decrease* in interconnect reliability due to electromigration—as noted above.

Measures to handle electromigration, such as current-dependent routing or the adaptation of the track width in highly loaded interconnects, are *de rigueur* today for designing analog integrated circuits. As a result of structural miniaturization, digital integrated circuits are now also affected by the problem of increasing current densities and accompanying EM. Typical measures, such as increasing the interconnect width, common in analog circuit design, cannot be deployed in these much more complex digital circuits. Such measures would work against the reduction in structure size and prevent further scaling. New approaches are therefore required to avoid EM damage in digital circuits, as a result of falling semiconductor scale.

Fundamentals of Electromigration-Aware Integrated Circuit Design
Jens Lienig, Susann Rothe, Matthias Thiele
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This book presents measures for layout design for avoiding damage caused by EM in both digital and analog ICs. We determine parameters for every measure so that the usability and suitability of a specific measure can be determined as a function of the technology used. Approved current densities can thus be increased at the critical places by means of local layout modifications. The aim essentially is to avoid exceeding approved current densities by enlarging reliability limits. This book provides the reader with the necessary knowledge to overcome such design challenges.

Furthermore, we show how novel physics-based EM models can help overcoming design challenges by giving more precise lifetime estimations and providing guidance where to apply EM countermeasures. Replacing current density as the decisive parameter for EM verification is an important step to avoid unnecessarily high safety margins and, thus, prevent overdesign.

It is particularly important that the proposed measures are applied at the physical-design stage, and especially for the routing step. The reason for this is that good interconnect routing allows the optimal utilization of measures for promoting EM robustness. Interventions at a later stage in the design process, typically involving layout modifications, are much less effective, because fewer modification options are available at this later stage. On the other hand, currents cannot be precisely specified before the layout is generated, as a physical network topology is needed to provide detailed current knowledge.

The fundamental physical problem of EM will be examined to the core in Chap. 2, as this knowledge is a requisite for adopting appropriate countermeasures. After first explaining the physical causes of EM, we introduce influencing factors arising from the specific circuit technology, the environment, and the design. We then investigate detailed EM mechanisms with regard to circuit materials, frequencies, and mechanical stresses. IC designers must be especially aware of thermal and stress migration; both are introduced and described in their interaction with EM.

Chapter 2 also outlines the principles of a migration analysis through simulation. This honors the importance of finite element modeling (using the finite element method, FEM) in EM analysis and enables the reader to develop and apply similar modeling and simulation techniques. We show simulation techniques for both conventional current density-based EM assessments and novel physics-based approaches.

Chapter 3 presents options for modifying the present design methodology to encompass EM prevention. Analog and digital designs are considered separately in this context as the respective measures differ for both. Understanding that knowledge of the currents flowing in interconnects is a fundamental requisite for an EM-aware design flow, we will discuss the different types of currents encountered and show how sensible current values can be determined.

In conventional models, the key parameter for EM prevention is the maximum permissible boundary value of the current density in the wires. This parameter is, however, dependent on the intended use of the IC, which is why so-called mission

profiles are created to determine such values. Chapter 3 describes how robust current-density boundary values (limits) can be determined, using application and reliability specifications.

Fundamental procedures for current-density verification are examined as well. Methods for eliminating problems, identified during current-density verification, by means of layout adjustment are presented. Finally, we put forward a number of approaches for increasing current-density boundary values, based on our assessment of current technological trends.

Moreover, it is shown how physics-based modeling can be used to further improve EM verification. The focus is on both immortality and lifetime checks. Both challenges and possibilities are discussed to demonstrate which obstacles remain to be overcome and what are the benefits physics-based EM modeling offers for the design of reliable ICs.

While Chap. 3 outlined options to address EM in today's physical design of electronic circuits, Chap. 4 describes in detail the EM-inhibiting effects that these options are based on. The goal of this chapter is to summarize the state of the art in EM-mitigating effects. This knowledge is presented such that a circuit designer can use it to increase EM limits with the overall goal of reducing the negative impact of EM on the circuit's reliability. We will show how EM-induced hydrostatic stress can be reduced by means of local layout modifications (thus, allowing increased current densities). Detailed application advice concludes each presented measure. We also consider material-related options to reduce EM, such as surface passivation.

In Chap. 5, we summarize our findings, make proposals for further EM-aware integrated circuit design, and present the future outlook in this field, along with expected developments in micro- and nanoelectronics.

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