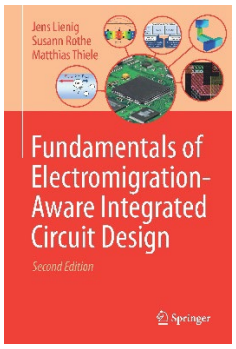

Fundamentals of Electromigration-Aware Integrated Circuit Design
Jens Lienig, Susann Rothe, Matthias Thiele
2025 (2nd edition), 164 pages, Springer Cham

ISBN 978-3-031-80022-1, eBook ISBN 978-3-031-80023-8
DOI 10.1007/978-3-031-80023-8

Notes and Sources of Figures in the Book

Fig. 1.1

The trajectories are directly derived from ITRS, 2013 edition; the cross-section area was calculated by

$$A = W^2 \cdot AR$$

with area *A*, width *W* and aspect ratio *AR*.

Fig. 2.15

The two curves are based on ITRS 2013 edition values: M1 halfpitch and clock frequency. Skin depth is calculated by Eq. (2.9) on p. 32 (Chap. 2).

Fig. 4.3

Width (halfpitch) is from ITRS 2013 edition, bamboo structure lengths (constant values) from [HRT01] and [HOG+12].

Fig. 4.12

Blech lengths are calculated from ITRS 2013 edition current density values, mean segment lengths are calculated from interconnect lengths on metal layers 1 through 6 and transistor density. (Transistor density has been taken from ITRS 2012 update. This value was supposed to be moved to the “Design” table in the 2013 edition, which was never published.)

Fig. 4.15

Blech lengths are calculated from ITRS 2013 edition current density values, while a lower Blech product *jL* is assumed for via above, mean segment lengths are calculated from interconnect lengths on metal layers 1 through 6 and transistor density. (Transistor density has been taken from ITRS 2012 update.)

Fig. 4.19

Blech lengths are calculated from ITRS 2013 edition current density values, while a double allowed Blech product jL is assumed for reservoirs, mean segment lengths are calculated from interconnect lengths on metal layers 1 through 6 and transistor density. (Transistor density has been taken from ITRS 2012 update.)

Sources

The following ITRS tables where used, with the applied values marked in green.

ITRS 2013:

Table INTC2 MPU Interconnect Technology Requirements

Grey cells indicate the requirements projected only for the years indicated.

Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
DRAM ½ Pitch (nm) (contacted)	28	26	24	22	20	18	17	15	14	13	12	11	10	9,2	8,4	7,7
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	40,0	31,8	31,8	28,3	25,3	22,5	20,0	17,9	15,9	14,2	12,6	11,3	10,0	8,9	8,0	7,1
MPU Physical Gate Length (nm)	20,2	18,4	16,8	15,3	14,0	12,8	11,7	10,65	9,72	8,87	8,10	7,39	6,75	6,16	5,62	5,13
Number of metal levels (includes ground planes and passive devices)	13	13	13	13	14	14	14	14	15	15	15	15	16	16	16	16
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	2.500	3.143	3.143	3.528	3.960	4.444	4.989	5.600	6.285	7.055	7.919	8.889	9.977	11.199	12.571	14.110
J_{max} (MA/cm^2) – intermediate wire (at 105°C) [7]	1,50	1,68	1,79	1,81	2,01	2,29	2,34	2,59	2,88	2,94	3,26	3,76	4,23	4,50	4,91	5,35
Interlevel metal insulator – effective dielectric constant (?)	2.55-3.00	2.55-3.00	2.55-3.00	2.40-2.78	2.40-2.78	2.40-2.78	2.15-2.46	2.15-2.47	2.15-2.48	1.88-2.28	1.88-2.28	1.88-2.28	1.65-2.09	1.65-2.09	1.65-2.09	1.40-1.90
Interlevel metal insulator –bulk dielectric constant (?)	2.30-2.60	2.30-2.61	2.30-2.60	2.20-2.55	2.20-2.55	2.20-2.55	2.00-2.40	2.00-2.40	2.00-2.40	1.80--2.20	1.80--2.20	1.80--2.20	1.60-2.00	1.60-2.00	1.60-2.00	1.40-1.80
Copper diffusion barrier and etch stop – bulk dielectric constant (?)	3.00-3.50	3.00-3.50	3.00-3.50	2.60-3.00	2.60-3.00	2.60-3.00	2.40-2.60	2.40-2.60	2.40-2.60	2.10-2.40	2.10-2.40	2.10-2.40	2.00-2.22	2.00-2.22	2.00-2.22	1.80-2.02
METAL 1																
Metal 1 wiring pitch (nm)	80	64	64	57	51	45	40	36	32	28	25	23	20	18	16	14
Metal 1 A/R (for Cu)	1,9	1,9	1,9	2,0	2,0	2,0	2,0	2,0	2,1	2,1	2,1	2,1	2,2	2,2	2,2	2,2
Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]	2,4	2,1	1,9	1,7	1,5	1,3	1,2	1,1	1,0	0,9	0,8	0,7	0,6	0,5	0,4	0,3
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	7,6	6,0	6,0	5,7	5,1	4,5	4,0	3,6	3,3	3,0	2,7	2,4	2,2	2,0	1,8	1,6
Conductor effective resistivity (µ?-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	4,03	4,62	4,51	4,77	5,08	5,41	5,85	6,35	6,84	7,43	8,07	8,75	9,38	10,10	10,81	11,41
Capacitance per unit length for M1 wires (pF/cm) - assumed PMD $?_{eff}$ = 4.2 [6]	1.8-2.0	1.8-2.0	1.8-2.0	1.8-2.0	1.8-2.0	1.8-2.0	1.6-1.8	1.6-1.8	1.7-1.8	1.5-1.7	1.5-1.7	1.5-1.7	1.4-1.7	1.4-1.7	1.4-1.7	1.4-1.7
Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below [8]. (Average C used from above)	7.804	10.525	15.145	17.941	24.021	33.460	44.784	58.192	74.884	84.852	154.678	170.570	215.789	312.877	399.000	535.000
Coupling ratio of M1 wire victim with an adjacent M1 wire aggressor [9]	33,1	33,1	33,1	33,9	33,9	33,9	33,4	33,4	34,4	33,4	33,9	33,9	34,2	34,2	34,4	34,4

INTERMEDIATE WIRES																
Intermediate wiring pitch (nm)	80	64	64	57	51	45	40	36	32	28	25	23	20	18	16	14
Intermediate wiring dual damascene A/R (Cu wire)***	1,9	1,9	1,9	2,0	2,0	2,0	2,0	2,0	2,1	2,1	2,1	2,1	2,2	2,2	2,2	2,3
Intermediate wiring dual damascene A/R (Cu via)***	1,7	1,7	1,7	1,8	1,8	1,8	1,8	1,8	1,9	1,9	1,9	1,9	1,9	1,9	1,9	1,9
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	2,4	2,1	1,9	1,7	1,5	1,3	1,2	1,1	1,0	0,9	0,8	0,7	0,6	0,5	0,4	0,3
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	7,6	6,0	6,0	5,7	5,1	4,5	4,0	3,6	3,3	3,0	2,7	2,4	2,2	2,0	1,8	1,6
Conductor effective resistivity (µ?-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	4,03	4,62	4,51	4,77	5,08	5,41	5,85	6,35	6,84	7,43	8,07	8,75	9,38	10,10	10,81	11,41
Capacitance per unit length for intermediate wires (pF/cm) - assumed PMD $?_{eff}$ = 4.2 [6]	1.6-1.9	1.6-1.9	1.6-1.9	1.5-1.8	1.5-1.8	1.5-1.8	1.4-1.6	1.4-1.6	1.4-1.6	1.2-1.5	1.2-1.5	1.2-1.5	1.1-1.4	1.1-1.4	1.1-1.4	1.1-1.4
Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below [8]	7.067	9.532	13.716	15.958	21.366	29.761	38.400	49.933	64.552	68.032	128.739	141.966	174.607	253.166	310.000	405.000
Coupling ratio of Intermediate wire victim with an adjacent Intermediate wire aggressor [9]	34,1	34,1	34,1	35,2	35,2	35,2	35,2	35,2	36,3	36,3	36,3	36,3	36,6	36,6	36,6	36,6
Semi-global wire pitch (nm) (ASIC only) [2x of Metal 1]	160	127	127	113	101	90	80	71	64	57	51	45	40	36	32	28

Table ORTC1 2013 ORTC Technology Trend Targets–2013-2020

Year of Production ["Risk Start" Production; followed by HVM]	2013	2014	2015	2016	2017	2018	2019	2020
Logic Industry "Node Name" Labeling (nm) [based on 0.71x reduction per "Node Name" (extended on 2yr pace from 2013)	"16/14"		"10"		"7"		"5"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2] (nm)	40	31.8	31.8	28.3	25.3	22.5	20.0	17.9
FinFET Fin Half-pitch (new) =.75 Mx (nm)	30.0	23.9	23.9	21.3	18.9	16.9	15.0	13.4
FinFET Fin Width (nm)	6.4	5.8	5.3	4.9	4.4	4.1	3.7	3.4
Flash ½ Pitch (nm) (un-contacted Poly)(f) [2D]	18	17	15	14.2	13.0	11.9	11.9	11.9
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	16-32	16-32	16-32	16-32	16-32	32-64	32-64	48-96
Flash 3D Layer half-pitch targetts (nm)	64nm	54nm	54nm	45nm	45nm	32nm	30nm	29nm
Flash Generation Bits/chip targets (independent of 2D or 3D) (SLC/MLC)	64G /128G	128G /256G	128G /256G	256G /512G	256G / 512G	256G / 512G	512G / 1T	512G / 1T
DRAM Generation Bits/chip targets	4G	8G	8G	8G	8G	16G	16G	16G
DRAM ½ Pitch (nm) (contacted)	28	26	24	22	20	18	17	15
SRAM Cell (6-transistor) Area factor	60	60	60	60	60	60	60	60
Logic Gate (4-transistor) Area factor	155	155	155	155	155	155	155	155
MPU/ASIC High Perf 6t SRAM Cell Area [60f2] (μm^2)	0.096	0.061	0.061	0.048	0.038	0.030	0.024	0.019
MPU/ASIC HighPerf 4t NAND Gate Size [155f2] (um2)	0.248	0.157	0.157	0.125	0.099	0.078	0.062	0.049
MPU/ASIC HighPerf 4t NAND Gate Density (K gates/mm2)	4.03E+03	6.37E+03	6.37E+03	8.03E+03	1.01E+04	1.27E+04	1.61E+04	2.02E+04
MPU High-Performance Printed Gate Length (GLpr) (nm)	28	25	22	19.8	17.7	15.7	14.0	12.5
MPU High-Performance Physical Gate Length (GLph) (nm)	20.2	18.4	16.8	15.3	14.0	12.8	11.7	10.65
ASIC/Low Standby Power Physical Gate Length (nm)	23.0	21.0	19.2	17.5	16.0	14.6	13.3	12.1
MPU High-Performance Etch Ratio GLpr/GLph	1.39	1.36	1.32	1.29	1.26	1.23	1.20	1.17
Power Supply Voltage (V)								
Vdd (V)	0.86	0.85	0.83	0.81	0.80	0.78	0.77	0.75
Intrinsic Transistor Frequency [1/(CV/I)] (1/psec)								
Bulk	1.04	1.14	1.20	1.27	1.33			
SOI	1.13	1.23	1.28	1.29	1.44	1.48	1.59	1.74
MugFET (MG)			1.53	1.63	1.75	1.84	1.97	2.00
8% TREND NEED DRIVER - FOR REFERENCE ONLY	1.00	1.08	1.17	1.26	1.36	1.47	1.59	1.71
On-chip local clock (Ghz)	5.50	5.72	5.95	6.19	6.44	6.69	6.96	7.24
Maximum number wiring levels	13	13	13	13	14	14	14	14
450mm Production Risk Starts (1Kwspm)				2016				
450mm Production High Volume Manufacturing (100Kwspm)						2018		

Table ORTC1 2013 ORTC Technology Trend Targets–2020-2028

Year of Production ["Risk Start" Production; followed by HVM]	2020	2021	2022	2023	2024	2025	2026	2027	2028
Logic Industry "Node Name" Labeling (nm) [based on 0.71x reduction per "Node Name" (extended on 2yr pace from 2013)		"3.5"		"2.5"		"1.8"		"1.3"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2] (nm)	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1
FinFET Fin Half-pitch (new) =.75 Mx (nm)	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6.0	5.3
FinFET Fin Width (nm)	3.4	3.1	2.8	2.6	2.3	2.1	2.0	1.8	1.6
Flash ½ Pitch (nm) (un-contacted Poly)(f) [2D]	11.9	11.9	11.9	11.9	11.9	11.9	11.9	11.9	11.9
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	48-96	48-96	64-128	64-128	96-192	96-192	96-192	192-384	192-384
Flash 3D Layer half-pitch targetts (nm)	29nm	28nm	27nm	27nm	26nm	25nm	24nm	23nm	22nm
Flash Generation Bits/chip targets (independent of 2D or 3D) (SLC/MLC)	512G / 1T	512G / 1T	1T / 2T	1T / 2T	2T /4T	2T / 4T	2T / 4T	4T /8T	4T /8T
DRAM Generation Bits/chip targets	16G	32G	32G	32G	32G	32G	32G	32G	32G
DRAM ½ Pitch (nm) (contacted)	15	14	13	12	11	10	9.2	8.4	7.7
SRAM Cell (6-transistor) Area factor	60	60	60	60	60	60	60	60	60
Logic Gate (4-transistor) Area factor	155	155	155	155	155	155	155	155	155
MPU/ASIC High Perf 6t SRAM Cell Area [60f2] (μm^2)	0.019	0.015	0.012	0.010	0.008	0.006	0.005	0.004	0.003
MPU/ASIC HighPerf 4t NAND Gate Size [155f2] (um2)	0.049	0.039	0.031	0.025	0.020	0.016	0.012	0.010	0.008
MPU/ASIC HighPerf 4t NAND Gate Density (K gates/mm2)	2.02E+04	2.55E+04	3.21E+04	4.05E+04	5.10E+04	6.42E+04	8.09E+04	1.02E+05	1.28E+05
MPU High-Performance Printed Gate Length (GLpr) (nm)	12.5	11.1	9.91	8.83	7.86	7.01	6.24	5.62	5.13
MPU High-Performance Physical Gate Length (GLph) (nm)	10.65	9.72	8.87	8.10	7.39	6.75	6.16	5.62	5.13
ASIC/Low Standby Power Physical Gate Length (nm)	12.1	11.1	10.1	9.24	8.43	7.70	7.03	6.42	5.86
MPU High-Performance Etch Ratio GLpr/GLph	1.17	1.14	1.12	1.09	1.06	1.04	1.01	1.00	1.00
Power Supply Voltage (V)									
Vdd (V)	0.75	0.74	0.72	0.71	0.69	0.68	0.66	0.65	0.64
Intrinsic Transistor Frequency [1/(CV/I)] (1/psec)									
Bulk									
SOI	1.74								
MugFET (MG)	2.00	2.10	2.16	2.29	2.22	2.24	2.32	2.35	2.36
8% TREND NEED DRIVER - FOR REFERENCE ONLY	1.71	1.85	2.00	2.16	2.33	2.52	2.72	2.94	3.17
On-chip local clock (Ghz)	7.24	7.53	7.83	8.14	8.47	8.81	9.16	9.53	9.91
Maximum number wiring levels	14	15	15	15	15	16	16	17.00	17.00
450mm Production Risk Starts (1Kwspm)									
450mm Production High Volume Manufacturing (100Kwspm)									

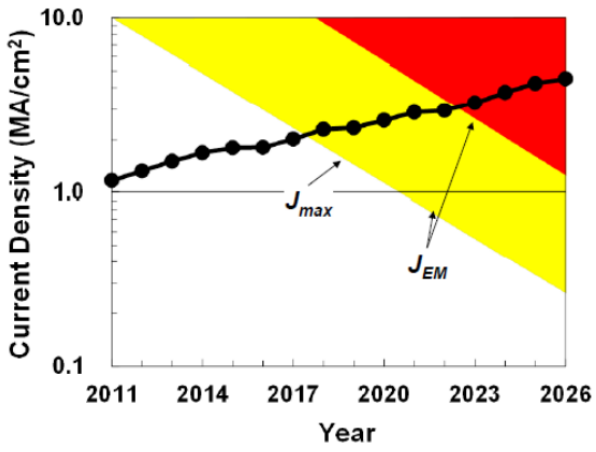

Figure INTC9 Evolution of Jmax (from device requirement) and JEM (from targeted lifetime)

ITRS 2012 Update (Data not available in ITRS 2013):

Table ORTC-2C MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model--MPU Model unchanged from the 2009 and 2010 roadmap editions, but extended to 2026

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14,2	13,0	11,9	10,9	10,0	8,9	8,0	8,0	8,0	8,0	8,0
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20,0	17,9	15,9	14,2	12,6	11,3	10,0	8,9	8,0	7,1	6,3
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18,9	16,9	15,0	13,4	11,9	10,6	9,5	8,4	7,5	6,7	6,0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19,8	17,7	15,7	14,0	12,5	11,1	9,9	8,8	7,9	6,79	5,87
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15,3	14,0	12,8	11,7	10,6	9,7	8,9	8,1	7,4	6,6	5,9
SRAM Cell (6-transistor) Area factor ++	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60,0	60,0
Logic Gate (4-transistor) Area factor ++	175	175	175	175	175	175	175	175	175	175	175	175	175	175	175,0	175,0
SRAM Cell (6-transistor) Area efficiency ++	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63	0,63
Logic Gate (4-transistor) Area efficiency ++	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50	0,50
SRAM Cell (6-transistor) Area (μm^2) ++	0,09	0,061	0,043	0,034	0,027	0,021	0,017	0,014	0,011	0,009	0,007	0,005	0,004	0,0034	0,0027	0,0021
SRAM Cell (6-transistor) Area w/overhead (μm^2) ++	0,137	0,097	0,069	0,055	0,043	0,034	0,027	0,022	0,017	0,014	0,011	0,0086	0,0068	0,0054	0,0043	0,0062
Logic Gate (4-transistor) Area (um2) ++	0,25	0,18	0,13	0,10	0,079	0,063	0,050	0,039	0,031	0,025	0,020	0,016	0,012	0,010	0,0078	0,0062
Logic Gate (4-transistor) Area w/overhead (μm^2) ++	0,50	0,35	0,25	0,20	0,16	0,13	0,10	0,079	0,063	0,050	0,039	0,031	0,025	0,020	0,0157	0,0124
Transistor density SRAM (Mtransistors/cm^2)	4.365	6.173	8.730	10.999	13.858	17.459	21.997	27.715	34.919	43.995	55.430	69.838	87.990	110.860	139.675	175.980
Transistor density logic (Mtransistors/cm^2)	798	1.129	1.596	2.011	2.534	3.193	4.022	5.068	6.385	8.045	10.136	12.770	16.090	20.272	25.541	32.179
*Generation at introduction **	p13c	p13c	p16c	p16c	p16c	p19c	p19c	p19c	p22c	p22c	p22c	p25c	p25c	p25c	p28c	p28c
Functions per chip at introduction (million transistors [Mtransistors])	3092	3092	6184	6184	6184	12368	12368	12368	24736	24736	24736	49471	49471	49471	98.942	98.942
Chip size at introduction (mm^2) ‡	280	222	280	222	176	280	222	176	280	222	176	280	222	176	280	222
OH % of Total Chip Area	27,9%	35,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%	42,8%
Logic Core+SRAM (Without OH Average Density (Mt/cm2)	1532	2166	3063	3859	4862	6126	7718	9725	12252	15437	19449	24505	30874	38899	49.009	61.748
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	1104	1391	1753	2209	2783	3506	4417	5565	7012	8834	11130	14023	17668	22261	28.047	35.336
*Generation at production **	p11c	p11c	p13c	p13c	p13c	p16c	p16c	p16c	p19c	p19c	p19c	p22c	p22c	p22c	p25c	p25c
Functions per chip at production (million transistors [Mtransistors])	1546	1546	3092	3092	3092	6184	6184	6184	12368	12368	12368	24736	24736	24736	49.471	49.471
Chip size at production (mm^2) §§	140	99	140	111	88	140	111	88	140	111	88	140	111	88	111	88
OH % of Total Chip Area	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%	27,9%
Logic Core+SRAM (Without OH Average Density (Mt/cm2)	1532	2166	3063	3859	4862	6126	7718	9725	12252	15437	19449	24505	30874	38899	49.009	49.009
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	1104	1562	2209	2783	3506	4417	5565	7012	8834	11130	14023	17668	22261	28047	35.336	35.336

ITRS 2015

Table INTC2 MPU Interconnect Technology Requirements

Grey cells indicate the requirements projected only for the years indicated.

Year of Production	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
DRAM ½ Pitch (nm) (contacted)	24	22	20	18	17	15	14	13	12	11	10	9	8	8		
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	26	18	18	12	12	9	9	6	6	6	6	6	6	6	6	6
MPU Physical Gate Length (nm)	16,8	15,3	14,0	12,8	11,7	10,65	9,72	8,87	8,10	7,39	6,75	6,16	5,62	5,13		
Number of metal levels (includes ground planes and passive devices)	10	11	11	12	12	13	13	15	15	17	17	19	19	21	21	21
Total interconnect length (m/cm2) – Metal 1 and five intermediate levels, active wiring only [1]	3.846	5.556	5.556	8.333	8.333	11.111	11.111	16.667	16.667	16.667	16.667	16.667	16.667	16.667	16.667	16.667
Interlevel metal insulator – effective dielectric constant (κ)	2.55-3.00	2.40-2.78	2.40-2.78	2.15-2.46	2.15-2.46	2.15-2.46	2.15-2.46	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28	1.88-2.28
Interlevel metal insulator –bulk dielectric constant (κ)	2,55	2.40-2.55/ 1.0	2.40-2.55/ 1.0	2.40-2.55/ 1.0	2.40-2.55/ 1.0	2.40-2.55/ 1.0	2.40-2.55/ 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0	2.00–2.55 / 1.0
Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	3.00-3.50	2.60-3.00	2.60-3.00	2.40-2.60	2.40-2.60	2.40-2.60	2.40-2.60	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40	2.10-2.40
METAL 1, INTERMEDIATE WIRES																
Metal 1 wiring pitch (nm)	52	36	36	24	24	18	18	12	12	12	12	12	12	12	12	12
Metal 1 A/R (for Cu)	1,9	2,0	2,0	2,1	2,1	2,1	2,1	2,2	2,2	2,2	2,2	2,2	2,2	2,2	2,2	2,2
Barrier/cladding thickness (for Cu Metal 1 wiring) (nm)	1,9	1,3	1,3	1,0	1,0	0,8	0,8	0,6	0,6	0,6	0,6	0,6	0,6	0,6	0,6	0,6
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	4,9	3,6	3,6	2,5	2,5	1,9	1,9	1,3	1,3	1,3	1,3	1,3	1,3	1,3	1,3	1,3
Conductor effective resistivity (µΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below [2]	5,1	6,4	6,4	8,4	8,4	10,4	10,4	12,9	12,9	12,9	12,9	12,9	12,9	12,9	12,9	12,9

**(Maximum and Minimum are divided into separate rows for easier calculation.*

***Higher and Lower values are divided into separate rows for easier calculation.*

****Wire and Via are divided into separate rows for easier calculation.*

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

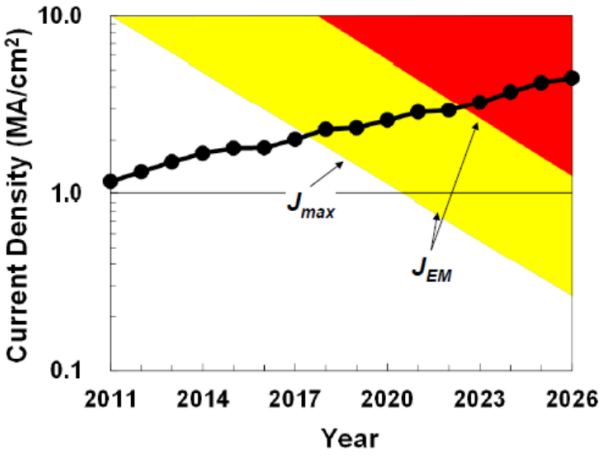

Figure INTC6 Evolution of Jmax (from device requirement) and JEM (from targeted lifetime)

IRDS 2022, "More Moore"

The following information from IRDS 2022[1] was used for the updated predictions (2nd edition) regarding device technology, interconnect and barrier materials, electromigration, and clock frequencies:

[1] *International Roadmap for Devices and Systems (IRDS)*, 2022 Edition, 2022. https://irds.ieee.org/editions/2022, last retrieved on Jan. 1, 2025

Table MM-11 Area, Power, and Performance Scaling of SoC

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
LOGIC TECHNOLOGY INTEGRATION CAPACITY						
Number of stacked tiers (1)	1	1	1	2	4	6
NAND2-eq gate count (Mgates/mm2)	21	29	39	81	171	284
L3 cache SRAM density (Mbits/mm2)	27	27	41	87	191	286
CPU thruput scaling target - node-to-node	1.70	1.70	1.70	1.70	1.70	1.70
#GPU cores in SoC - based on integration capacity	36	49	66	136	286	477
#CPU cores in SoC - based on thruput target, #CPUxfmax	12	20	33	55	92	155
#MAC units in SoC - based on integration capacity	8192	11038	14980	30966	65191	108652
Analog + IO scaling	1.00	0.85	0.72	0.61	0.52	0.44
SoC footprint scaling	1.00	0.85	0.61	0.33	0.19	0.14
POWER AND PERFORMANCE SCALING FACTORS						
HP frequency improvement	1.00	1.03	1.06	1.08	1.09	1.10
HP block power at iso frequency	1.00	0.83	0.78	0.59	0.50	0.48
HD block power at iso frequency	1.00	0.81	0.72	0.56	0.50	0.49
HP power at fmax	1.00	0.80	0.74	0.55	0.46	0.44
Power density at fmax	1.00	1.03	1.20	2.29	4.85	7.99
CPU clock frequency (GHz)	3.18	3.28	3.36	3.42	3.47	3.50
CPU clock frequency at constant power density (GHz)	3.18	3.17	2.79	1.49	0.71	0.44
CPU throughput at fmax (TFLOPS/sec)	0.31	0.52	0.88	1.50	2.55	4.33
CPU throughput at constant power density (TFLOPS/sec)	0.31	0.50	0.73	0.65	0.53	0.54

4.5.4. Reliability—Electromigration

An effective scaling model has been established in the earlier editions of roadmap where it assumes that the void is located at the cathode end of the interconnect wire containing a single via with a drift velocity dominated by interfacial diffusion. The model predicts that lifetime scales with w*h/j, where w is the linewidth (or the via diameter), h the interconnect thickness, and j the current density. Whereas the geometrical model predicts that the lifetime decreases by half for each new generation, it can also be affected by small process variations of the interconnect dimensions. Jmax (maximum equivalent DC current density) and JEM (DC current density at the electromigration limit) are limited by the interconnect geometry scaling. Jmax increases with scaling due to reduction in the interconnect cross-section and increase in the maximum operating frequency. The practical solutions to overcome the lifetime decrease in the narrow linewidths have been discussed actively over the past years. Recent studies show an increasingly important role of grain structure in contributing to the drift velocity and thus the EM reliability beyond the 45nm node. Process solutions with Cu alloys seed layer (e.g., Al or Mn) have shown to be an optimum approach to increase the lifetime. Other approaches are the insertion of a thin metal layer (e.g., CoWP or CVD Co) between the Cu trench and the dielectric SiCN barrier and the usage of the short length effect. The short length effect has effectively been used to extend the current carrying capability of conductor lines and has dominated the current density design rule for interconnects.

Table MM-13 Interconnect Roadmap for Scaling

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
INTERCONNECT TECHNOLOGY						
Number of Mx layers	2	2	2	2	2	2
Number of >P40 and <P720 layers	12	12	13	14	14	14
Number of P720 layers	2	2	2	2	2	2
Number of wiring layers - M1+Mx+ >P40	17	17	18	19	19	19
Mx - tight-pitch interconnect resistance (Ohms/um)	300	475	920	1450	1450	1450
Mx - tight-pitch interconnect capacitance (aF/um)	270	270	270	270	270	270
Vx - tight-pitch interconnect via resistance (Ohms/via)	50.0	53.0	38.0	64.0	64.0	64.0
MP80 - 80nm pitch interconnect resistance (Ohms/um)	13.3	13.3	13.3	13.3	13.3	13.3
MP80 - 80nm pitch interconnect capacitance (aF/um)	198	198	198	198	198	198
VP80 - 80nm pitch interconnect via resistance (Ohms/via)	5.0	5.0	5.0	5.0	5.0	5.0
Aspect ratio - M0, M1, Mx, MP80, MP720	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5
Power rail layer	M0	Buried Rail	Buried Rail	Buried Rail	Buried Rail	Buried Rail
Power rail material	Co, W, Ru	W, Ru	W, Ru	W, Ru	W, Ru	W, Ru
Metallization - M0	Co, W, Ru	Co, W, Ru	Co, W, Ru	Co, W, Ru	Co, W, Ru	Co, W, Ru
Barrier - M0	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC
Metallization - M1, Mx	Cu	Cu, Co, Ru	Cu, Co, Ru	Cu, Co, Ru	Cu, Co, Ru	Cu, Co, Ru
Barrier metal - M1,Mx	1.5nm TaNCo	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC
Di-electrics k value - M0,M1,Mx	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)
Metallization - >MP40	Cu	Cu	Cu	Cu	Cu	Cu
Di-electrics k value - >MP40	SiCOH (2.40-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)